An Adaptive Path Delay Fault Diagnosis Methodology

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Abstract

A framework to adaptively perform delay fault diagnosis is introduced. We propose a methodology to perform diagnosis taking into account the effect of test vector on the propagation delay along a path. An ATPG capable of generating test vectors that cannot be invalidated due to process variations in the submicron technology is used for diagnosis purposes. The proposed framework also has the ability to generate tests that can take of care delay faults induced by noise. Experimental results on the ISCAS'85 benchmarks shows the effectiveness of the proposed technique.

1 Introduction

With the advent of deep-submicron technology, testing the performance of an integrated circuit (IC) has become a difficult task. Even small process variations can cause a fault in the circuit. Therefore before mass production of the IC, a small number (first silicon) is produced to perform the various tests and check for the performance of the IC. The check is performed by applying test vectors and comparing the expected output to the sampled output. In this paper, without loss of generality, a slow-fast test application methodology on the combinational component of the digital synchronous circuit is assumed. The concepts presented in this paper can be extended with trivial modifications to handle at-speed test application methodology. Assuming that the chip is functionally correct, i.e., the chip produces the correct output if given enough time, any fault observed at the output is the result of one or more delay faults in the circuit under diagnosis(CUD). The process of locating input-output paths in the chip that caused the delay fault is termed as *delay fault diagnosis*. In this paper we use the path delay fault model (PDF) for delay fault diagnosis.

One of drawbacks with the PDF model is the implicit assumption that all test vectors excite the same delay through a path. We refer to this as *pattern independent path delay fault* or *conventional path delay fault model*. Such an assumption is optimistic for delay diagnosis. This has been noted in [10] also. Test generation techniques like [5] propose methods to excite a large propagation delay through the path under consideration. Techniques like [8, 9] implicitly use the delay independent PDF model for diagnosing delay faults which may lead to identifying an erroneous set of PDFs as faulty. Hence it is mandatory for a delay fault diagnosis approach to consider the pattern dependent delay defects for diagnosis purposes. [11] proposed such a framework for diagnosing transition faults. However the transition fault model does not accurately describe the distributed delay defects like the PDF model. The approach presented in [11] cannot be directly extended for the PDF model. It also works under the assumption that no noise exists in the circuit under diagnosis. Such an assumption is not valid for submicron technologies.

In this paper we present an approach which can use the pattern dependent PDF model for delay diagnosis and also take into consideration the effect of noise on the temporal behavior of the circuit under diagnosis. The proposed approach differentiates between errors introduced by the pre-layout processes and the post-layout processes. Errors introduced by design errors, intra-chip process variations, etc., are classified as pre-layout errors. The errors introduced by noise (like crosstalk, ground bounce, etc.,) and manufacturing defects (like bridging) are considered as post-layout errors. The inter-chip variations are not considered here because the proposed diagnosis is performed on the first silicon.

Diagnosis frameworks like [3, 8, 9] perform delay diagnosis (using conventional PDF model) using on cause-effect analysis. In cause-effect analysis methods, a set of input vector pairs that is provided is applied to the circuit under test and the output of the applied test is compared against the expected output. This information is used to prune the set of possible faults in an attempt to locate the fault. One of the key concepts in cause-effect diagnosis is that, *f*aults that

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are not sensitized cannot be diagnosed. Hence any cause-effect based diagnosis approach does not guarantee to detect all possible delay faults in the circuit under diagnosis and the diagnostic resolution depends on the initial test set.

A straight forward approach for diagnosing delay faults is to test each PDF by itself and not exciting any other fault together by the same test. Such an approach is not always feasible and, furthermore, not practical due to the number of faults that can exist in a circuit. Hence it starts diagnosing delay faults using a test set that is compact and targets a large set of faults for each single test vector. However with such a test set, it is extremely difficult to identify the faulty PDF from the set of suspected faults corresponding to a single failing test. An appropriate solution to this problem is to adaptively generate additional tests to improve the diagnostic resolution gradually. Techniques like [4, 12] propose adaptive test generation for diagnosis, however still fail to take into account the effect of pattern dependence on the excitation of delays through a PDF. Here we propose a framework that is capable of adaptively generating tests for diagnosing PDFs by taking into consideration the effect of pattern dependence on the propagation delay and also the effect of noise on the PDFs.

Section 2 defines the problem studied and reviews the traditional delay fault diagnosis methodology. Section 3 introduces the proposed pattern dependent delay diagnosis framework and the need for adaptive test generation to improve diagnostic resolution. It describes conditions whose satisfaction guarantees improved resolution. Section 4 proposes a hybrid ATPG technique that attempts to satisfy constraints formulated in Section 3 using both boolean functions and a PODEM based approach to generate effective test vectors. Experimental results and conclusion are provided in Sections 5 and 6, respectively.

2 Preliminaries

The problem of delay fault diagnosis is defined as the process of identifying the potential set of PDFs that causes observable delay faults for a given initial test set $\mathcal{T}$. An adaptive diagnosis process generates additional test vectors to further improve the diagnostic resolution. In the proposed framework, we also try to differentiate between the potential causes of error, either as pre-layout error or post-layout error. This distinction helps in fixing the errors more accurately.

Consider a test set $\mathcal{T}$. For each input vector pair $t \in \mathcal{T}$ for which the expected and observed output transition and output logical state is the same is termed as a passing test. Each t for which the expected and observed output transition or logical state differ is termed as a *failing test*. The set of all passing tests $\mathcal{T}_p$ (respectively failing tests $\mathcal{T}_f$) is termed as a *passing set*(respectively *failing set*). The set of all PDFs tested by the passing set and is guaranteed to be fault free is termed as a *fault free set* $\mathcal{F}$. The set of all PDFs tested by the failing set that could explain for the error observed is termed as a *suspect set* $\mathcal{S}$.

A *fault free PDF* is defined as a PDF that is tested by a given passing test and is guaranteed to be fault free. A collection of such PDFs form the *fault free set*. Several PDFs in the suspect set may be fault-free. Based on the PDFs in the fault free and suspect set, such PDFs in the suspect are shown to be fault free, thus reducing the search space of the potential fault.

Let circuit $\mathcal{C}$ be the circuit under diagnosis. Let $\mathcal{T}_p$ and $\mathcal{T}_f$ be the passing set and failing set of test vectors, respectively. The problem of pattern independent delay diagnosis [8, 9] is defined to identify the minimum subset of $\mathcal{S}$ formed by the set of PDFs sensitized by $\mathcal{T}_f$. An outline of the caused-effect diagnosis procedure [8, 9] is described by Algorithm 1.

Algorithm 1 Diagnosis($\mathcal{C}, \mathcal{T}_p, \mathcal{T}_f$)

Require: $\mathcal{C}, \mathcal{T}_p, \mathcal{T}_f$
1: Identify the fault free set $\mathcal{F}$, tested by robust tests in $\mathcal{T}_p$
2: Identify the suspect set $\mathcal{S}$, tested by all tests in $\mathcal{T}_p$
3: **for all** s such that $s \in \mathcal{S}$ **do**
4: **if** s is a single PDF and is present in $\mathcal{F}$ **then**
5: Remove s from $\mathcal{S}$
6: **else if** s is a multiple PDF and a subset of s is present in $\mathcal{F}$ **then**
7: Remove s from $\mathcal{S}$
8: **end if**
9: **end for**
10: Return $\mathcal{S}$

If a single PDF s is in both $\mathcal{S}$ and $\mathcal{F}$ then it is guaranteed under the conventional PDF model to be fault free and is hence eliminated from $\mathcal{S}$. If a multiple PDF s in $\mathcal{S}$ has a subfault in $\mathcal{F}$ then it is guaranteed under the conventional PDF model to be fault free and is hence eliminated from $\mathcal{S}$. This is because a delay fault in a multiple PDF cannot be observed unless all of the subfaults that constitutes the multiple PDF also has an observable delay fault [12]. In [8, 9] Procedure Diagnosis has been implemented non-enumeratively using novel algorithms on appropriate data structures. Implementation details are ommitted here.

Some PDFs sensitized by a passing test vector may not be indeed fault free if the conventional PDF model is used, and thus result to an erroneous resolution. There are several cases where the resolution is overly pessimistic.

Under the conventional model, there are several cases where a delay fault can be masked. A non-robust test inherently has this property. Consider two robustly sensitized PDFs that are sensitized by the same failing pattern and share the same sub-path from some internal gate g to a pri-

mary output. The PDF with the earliest arriving transition to a non-controlling value at g is also masked under this pattern applicant. In fact, all but one (robustly or non-robustly) sensitized PDFs to some common output will be masked under any applied failing pattern.

The proposed pattern dependent PDF method refines the diagnostic resolution by considering the above cases. It uses typical delays which can model inter-chip process variations and other pre-layout errors in first silicon. However, post-layout errors cannot be easily modeled and one cannot rely on simple fault simulation arguments to identify the masked PDFs by failing patterns. A more sophisticated method is required. The method proposed in Section 3 presents necessary conditions that allow for correct and effective improvements in the diagnostic resolution under non-modeled post-layout errors.

3 Pattern Dependent Delay Fault Diagnosis

Let p be a PDF and p^{t_i} be the pattern dependent version of p corresponding to the test t_i. Let $\mathcal{K}^p$ represent the set of all tests that can sensitize p. Let $d_p^{t_i}$ be the propagation delay of p corresponding to test $t_i \in \mathcal{K}^p$ using typical delay values that model pre-layout errors. For each $t_i \in \mathcal{K}^p$, techniques like [5, 10] can be used to sort p^{t_i} based on $d_p^{t_i}$. Let p^{t_i} and p^{t_j} be two different pattern dependent versions of the PDF p.

The input is a test set $\mathcal{T}$. By definition, cause-effect diagnosis does not apply to faults that are never sensitized by $\mathcal{T}$. Thus, adaptive diagnosis is needed to be performed to classify a PDF p as either faulty or fault free (for the given test set $\mathcal{T}$) if it satisfies any one of the following two conditions:

1. The PDF p is present both in $\mathcal{F}$ and in $\mathcal{S}$.
2. The PDF p is present only in $\mathcal{S}$.

In the following, when we refer to noise induced delay, we consider delay defects induced by crosstalk. However the concepts presented here are directly extendable to delay defects induced by other sources like ground bounce, high resistance bridging, etc. Four different classifications are given when a PDF p is present both in $\mathcal{F}$ and $\mathcal{S}$. We also note the properties that a diagnostic test vector needs to possess to classify p as either faulty or fault free. The four different classifications are presented below.

- **Case A**: If p^{t_i} is in $\mathcal{F}$ and p^{t_j} in $\mathcal{S}$ and $d_p^{t_i} > d_p^{t_j}$, p^{t_j} has a propagation delay lesser than p^{t_i}. It is expected that p^{t_j} is delay fault free because p^{t_i} is fault free. Hence the delay fault that is observed for PDF p sensitized by the test vector t_j can be attributed to noise induced delay. However it is also possible that delay fault on p due to t_i has been masked by signal speed-up on p due to noise.
- **Case B**: If p^{t_i} is in $\mathcal{S}$ and p^{t_j} in $\mathcal{F}$ and $d_p^{t_i} > d_p^{t_j}$, p^{t_j} has a propagation delay lesser than p^{t_i}. It is either possible that p^{t_j} is fault free or that the delay fault in p due to t_j has been masked due to pattern dependence or by signal speed-up on p due to noise.
- **Case C**: If p^{t_i} is in $\mathcal{F}$ and p^{t_j} in $\mathcal{S}$ and $d_p^{t_i} < d_p^{t_j}$, p^{t_i} has a propagation delay lesser than p^{t_j}. It is either possible that p^{t_i} is fault free or that the delay fault in p due to t_i has been masked due to pattern dependence or by signal speed-up on p due to noise.
- **Case D**: If p^{t_i} is in $\mathcal{S}$ and p^{t_j} in $\mathcal{F}$ and $d_p^{t_i} < d_p^{t_j}$, p^{t_i} has a propagation delay lesser than p^{t_j}. It is expected that p^{t_i} is delay fault free because p^{t_j} is fault free. Hence the delay fault that is observed for PDF p sensitized by the test vector t_i can be attributed to noise induced delay. However it is also possible that delay fault on p due to t_j has been masked by signal speed-up on p due to noise.

Clearly, cases A and D are equivalent conditions and similarly do cases B and C. Thus, for simplicitly we address cases A and B.

In the following, conditions are described under which additional tests can be generated in order to correctly improve the diagnostic resolution. The approach generates an additional test for p when available both in $\mathcal{F}$ and $\mathcal{S}$ in order to ensure the status of the p in $\mathcal{F}$. A distinction is made according to either case A or B.

- **Case A**: The new test set must clarify whether a PDF p in the suspect set is masked when applying pattern t_i due to signal speed-up or that a delay fault exists in p when applying t_j. This is accomplished by generating a single additional test vector t_k using the timed ATPG framework presented in Section 4. The new test vector t_k must satisfy that $d_p^{t_k} \geq d_p^{t_i} > d_p^{t_j}$. In addition, the timed ATPG must ensure that the signals at the off-inputs do not arrive later than the on-inputs and that no delay is introduced in p due to noise.
- **Case B**: The new test set must clarify if p^{t_j} is fault free or its delay has been masked by noise or due to pattern t_j. In this case, the new test vector t_k needs to satisfy the condition that $d_p^{t_k} > d_p^{t_j}$. The timed must also ensure that the signals at the off-inputs do not arrive later than the on-inputs, and that no delay is introduced on p due to noise. If there exists a t_k and is a passing test then p^{t_j} is fault free and p^{t_i} can be eliminated from $\mathcal{S}$.

If a pattern dependent version of p is present in $\mathcal{F}$ and in $\mathcal{S}$, the delay correctness of p cannot be verified. A PDF p can be deemed as fault free only after all the conditions

described above have been met. If a test t_k does not exist then p is eliminated from $\mathcal{F}$ and is not used to eliminate any PDFs from $\mathcal{S}$ in order to prove a pattern dependent version of p in $\mathcal{F}$ as fault free. Once this correctness is ascertained, then all the conditions proposed in [8, 9] can also be used for improving the diagnostic resolution. As explained in the previous section, the methods in [8, 9] can lead to erroneous resolution if used in a stand-alone manner.

Purely following the rules of cause-effect analysis will not yield in a high diagnostic resolution because the result totally depends on the characteristics and coverage of the passing and failing test set $\mathcal{T}_p$ and $\mathcal{T}_f$, respectively. [4] proposed an approach to incrementally generate test vectors for gate delay fault diagnosis based on $\mathcal{F}$ and $\mathcal{S}$ so that additional fault free PDFs from $\mathcal{S}$ can be eliminated thereby improving the diagnostic resolution.

As described earlier, not all PDFs in $\mathcal{S}$ are necessarily faulty. Some of the fault free PDFs may be included in $\mathcal{S}$ due to the process of sensitization of more than a single fault by a test vector in $\mathcal{T}_f$. A new test set $\mathcal{T}_n$ is adaptively generated to improve the diagnostic resolution. It is however noted here that such an adaptive test generation process is guided by conditions mentioned above. Any PDFs that are added in $\mathcal{F}$ must satisfy them to ensure that they are indeed fault free. We describe the proposed approach using Algorithm 2.

Algorithm 2 Adaptive Diagnosis($\mathcal{C}, \mathcal{T}_p, \mathcal{T}_f$, Delay Model)

Require: $\mathcal{C}, \mathcal{T}_p, \mathcal{T}_f, DelayModel$
1: Identify the fault free set $\mathcal{F}$, tested by robust tests in $\mathcal{T}_p$
2: Identify the suspect set $\mathcal{S}$, tested by all tests in $\mathcal{T}_p$
3: **for all** PDFs s such that $s \in \mathcal{F}$ **do**
4: **if** s is present in $\mathcal{S}$ **then**
5: Check for the correctness of s
6: **if** s is faulty **then**
7: Remove s from $\mathcal{F}$
8: **else**
9: Remove s from $\mathcal{S}$
10: **end if**
11: **end if**
12: **end for**
13: **for all** PDFs s such that $s \in \mathcal{F}$ **do**
14: Generate additional tests for s
15: **if** s is fault free **then**
16: Remove s from $\mathcal{F}$
17: **end if**
18: **end for**
19: Return $\mathcal{S}$

4 A Hybrid ATPG Approach

In this section we briefly present a timed ATPG technique that uses a combination of boolean functions (implemented using BDDs) and structural techniques (like PODEM) to generate test vectors. Timed ATPG for path delay faults was introduced in [2]. However a modified PODEM based approach was used to generate test vector. It can be observed from [2] that using purely structural techniques for timed ATPG can be extremely time complex to find the existence of a solution/test vector for a given path and timing constraints. To over come this problem we propose a hybrid approach.

For a given PDF p and the timing constraints, a boolean function based approach similar to [1] is used to generate a boolean function $\mathcal{L}$ that contains all possible tests for the PDF p. However the boolean function only satisfies the logical constraints for the target PDF. Each minterm in $\mathcal{L}$ is a potential test that can possibly satisfy the timing constraints for p. A PODEM based approach is used to check if any of the minterms in $\mathcal{L}$ satisfies the timing constraints for p. This is done by using the function $\mathcal{L}$ to guide the PODEM based technique during the backtracking procedure involved in the PODEM algorithm. This hybrid approach is very effective for timed ATPG because $\mathcal{L}$ helps reduce the search space during the test generation process.

The ATPG technique is capable of using any delay model for the gates and interconnects. We use a delay model derived from the technology libraries of TSMC standard cell libraries. The delays associated with the gates and interconnects play a vital role in generating tests that is capable of masking the effect of noise on the propagation delay as described in Section 3.

Techniques like [13] can be used if the test generated is needed to excite the crosstalk effect at a site. However for diagnosis purposes, we mask the effect of crosstalk by making sure that the timing window for the signal transition on the PDF p is mutually disjoint with the timing window on the other potential crosstalk sites. Potential sites which can possibly be the source of crosstalk can be identified using [7].

5 Experimental Results

The proposed approach has been implemented in the C language. The performance of the tool was experimentally verified using the ISCAS'85 benchmarks on a Sun Blade 1000 workstation. The information about the delay ranges for each gate was obtained from the TSMC 0.5μ technology files using the corner values for the nMOS and pMOS transistors. The approach can benefit from any recently proposed delay model such as the one in [13].

Table 1. Adaptive Improvement of Diagnostic Resolution

Circuit Name	Passing Set	Failing Set	Conventional Diagnosis			Proposed Approach				
			Fault Free Set	Suspect Set	time (s)	Fault Free Set	Suspect Set	New Passing Tests	New Failing Tests	time (s)
c880	2,485	112	5,383	282	101.2	5,010	56	127	14	197.3
c1355	6,258	158	9,376	381	165.3	8,747	91	364	22	375.5
c1908	4,450	203	8,330	365	139.1	7,591	102	228	26	364.4
c2670	3,003	224	8,489	521	144.6	7,844	138	343	31	253.5
c3540	9,498	396	19,491	446	205.2	17,398	132	318	19	363.1
c5315	5,382	273	9,437	592	169.3	8,678	167	391	29	390.2
c6288	12,549	355	17,539	743	344.8	14,836	182	323	35	429.7
c7552	5,592	246	13,438	334	187.4	11,893	126	146	27	347.8

The results if the experiments are presented in Table 1. For each circuit listed in Column 1, the size of the initial passing and failing sets[1] are represented by Columns 2 and 3 respectively. These tests were generated using a boolean function based ATPG [6]. Columns 4 and 5 show the size of the fault free and suspect sets identified using the pattern independent/conventional diagnosis approach [8, 9]. Column 6 shows the CPU time required for this diagnosis procedure. Columns 7 and 8 show the size of the fault free and suspect sets identified using the proposed pattern dependent diagnosis approach. Column 11 shows the required CPU time.

It can be observed by comparing the values in Columns 4 and 7 that the size of the fault free set identified by the proposed approach is smaller. This is due to the fact that some of the PDFs in the fault free set are indeed faulty and are eliminated. These PDFs are identified using the procedure outlined in Section 3. This process also makes the proposed approach somewhat slower in terms of execution time due to the extra computations required to guarantee that the set of PDFs in the fault free set is indeed fault free.

After identifying the fault free set $\mathcal{F}$ and the suspect set $\mathcal{S}$, the hybrid ATPG from Section 4 is used to adaptively and on a PDF-enumerative basis generate additional tests $\mathcal{T}_n$ based on the contents of $\mathcal{F}$ and $\mathcal{S}$. $\mathcal{T}_n$ can be then used to improve the diagnostic resolution further. Columns 9 and 10 show the passing and failing tests which comprises to form $\mathcal{T}_n$. Column 8 shows the size of the suspect set after improving the resolution using the passing set from $\mathcal{T}_n$. Column 11 shows the CPU time required for the adaptive test generation and diagnosis. The increase is in part due to the enumerative nature of the proposed method.

The result represented in Columns 4 and 7 outlines the main advantage of the proposed approach over the conventional PDF diagnosis methods. The difference between columns 4 and 7 represents the number of faults in $\mathcal{F}$ that is classified as fault free and is used for further improving the diagnostic resolution. This error is observed to be between 5-10%. This erroneous result can greatly affect the set of faults identified as faulty using conventional diagnosis methods.

It can be observed from Columns 5 and 8 that the adaptive approach presented here results in the reduction of the size of the suspect set by an average of 300%. However it is noted that the diagnostic resolution is attained by using a small number of additional test vectors (sum of columns 9 and 10).

[1]The initial passing and failing test sets together form the test set $\mathcal{T}$

6 Conclusions

Necessary conditions to perform correct diagnosis considering pattern dependence and effect of noise on the propagation delay along a path is presented. An efficient timed ATPG using a combination of structural and boolean function based approach is also introduced for this purpose. The ATPG is also used for adaptively improving the diagnostic resolution. The experimental results clearly shows the merits of the proposed diagnosis methodology. Future work will focus on the non-enumerative implementation of the proposed methodology.

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