Supply and Substrate Noise Tolerance Using Dynamic Tracking Clusters in Configurable Memory Designs

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Abstract

Pattern-sensitive soft errors, subject to varied supply and substrate noises, have become increasingly significant for configurable memories embedded in SoCs. In this paper, we study their effects on memory cell, array, and circuit design. It is found that the ground bounce reduces the cell current more severely than the supply voltage drop and substrate bias dip. This encourages the use of metal wires along the wordline or row direction. Bitline tracking by current ratio achieves better accuracy and design for manufacturing (DFM) capability than by capacitance ratio. It requires further enhancement to be resilient to the supply and substrate noises. The proposed dynamic tracking cluster technique provides necessary timing relaxation, while minimizing the speed degradation. Configurable embedded SRAM and ROM in 0.18µm CMOS process are studied.

1. Introduction

Configurable memories have been embedded in SoCs with increasing demands for higher speed, lower power, and larger density. Their circuit design and manufacturing yield become the bottlenecks for the success of SoCs [1] in view of the unique characteristics in circuit and layout to be applicable to a large number of configurations. Considering the variations in foundry process corners, power supply voltages, and working temperatures (PVT), which must be equally tolerable as all other components in the SoC, the architecture of the configurable memories can be different from that of the commodity memories. Bitline tracking [2-3], for example, is a commonly used scheme in embedded memories and instance generators that is rarely adopted in commodity memories.

As digital, mixed-signal, radio-frequency (RF), and memory blocks are integrated on the same substrate of a chip, the supply and substrate noises may not only degrade the overall system performance, but also cause sensitive blocks suffering functional failures. Furthermore, the operating environments can be varied from chip to chip which are unpredictable by the circuit designers. Thus, high-quality embedded memories must be designed to operate under noisy environments in SoCs.

Previous works studied the effects of supply and substrate noises on digital [4-5], mixed-signal [6-7], and RF [8-10] circuits. Also, there are reports [4, 11] pointing out that the power supply noise is a dominant source for substrate noise. Therefore, dedicated substrate bias and guard ring have been proposed and proven to be very effective in substrate noise reduction for digital and mixed-signal circuit [12-14].

Because embedded memories occupy an increasingly large area in SoCs, a detailed study of the effects of supply and supply noises on the embedded memories is necessary. Unfortunately, there are few reports on this topic. This paper deals with supply and substrate noises in configurable SRAM and ROM, where the sensing timing is controlled by bitline tracking circuit. A dynamic tracking cluster scheme is proposed to improve the noise immunity.

The remainder of our presentation is organized as follows. Section 2 discusses the effects of supply and substrate noises on the memory cells and arrays. Section 3 discusses the effects of supply and substrate noises on the configurable memory circuit design. Section 4 presents the dynamic bitline tracking cluster scheme. Section 5 contains our conclusions.

2. Supply and Substrate Noises on Memory Cells and Arrays

When a transient current occurs in a chip, the power and ground lines may encounter voltage drop and ground bounce which could be oscillating or ringing, primarily due to the parasitic resistance and inductance on the power mesh interconnects and package bonding wires. In popular embedded memories, such as SRAM and ROM, the power and ground lines in the cell array are usually implemented by narrow-width metal or diffusion strips in order to meet the tight area constraints. Hence, each memory cell may be subject to varied supply and substrate noises, depending on its location and neighborhood data pattern at the same column, row, or block. This causes fluctuations in cell currents during the read operation, which alter the bell-shape normal distribution to a different center and/or extreme values. The effect is more severe in large-sized memory array in that sufficient margins must be reserved.

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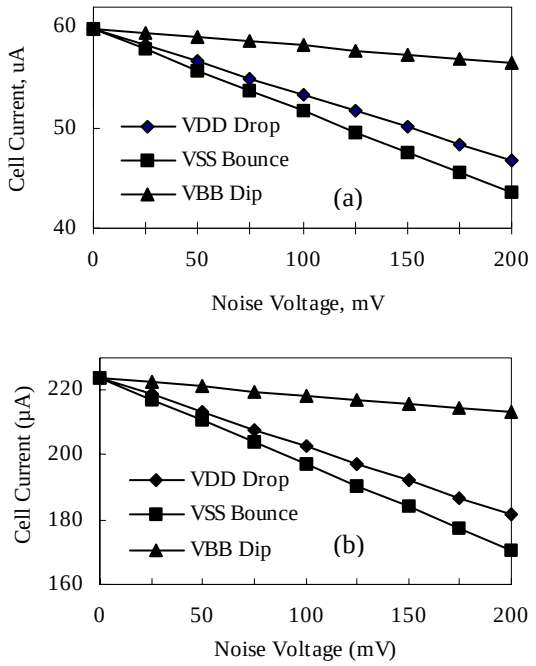

Fig. 1. Cell current fluctuations due to supply voltage (VDD) drop, ground (VSS) bounce, substrate bias (VBB) dip on (a) 6T SRAM and (b) ROM cell in 0.18μm logic process.

The cell current fluctuations have a linear relationship with supply voltage drop, ground bounce, and substrate bias dip, respectively, as shown in Fig. 1. If the supply voltage drop, ground bounce, or substrate bias dip occurs uniformly in a cell array, the sink current of each memory cell fluctuates essentially in the same way. The distribution still keeps a similar shape but has a different mean value. However, if the supply and substrate noises vary at different locations in the cell array, the distribution may change dramatically, which spreads to a wider range than the one without the noises.

Given the same amount of voltage variation, ground bounce leads to the most severe cell current degradation, compared to supply voltage and substrate bias, since the drain-to-source voltage decreases and the source-to-bulk voltage increases at the same time. This effect applies to other types of memory cells as well, which has at least an NMOS transistor in the current path. As a result, trading the silicon area of a memory cell for noise immunity can emphasize more on ground connections than power. Clearly, it encourages the use of metal wires in a mesh connection.

For SRAM and ROM, substrate contacts are usually placed outside the memory cell and shared to save silicon area. To provide the extra connections, the array adds the strap cells, which are shared along the row (wordline) direction by every *n* memory cells, where, in practice, *n* may range from 16 to 64 for SRAM and is larger than 32 for ROM. Fig. 2 illustrates the placement of strap cells in the memory array.

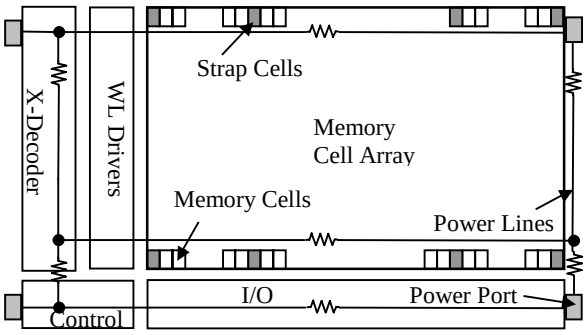

Fig. 2. An embedded memory architecture using strap cells for power and ground connections in the array.

Due to the relatively high resistance in substrate and diffusion areas and the different paths of noise propagation, the substrate noise induced by the ground line has a phase delay, depending on the location of the memory cell in the array. For the memory cell located between two strap cells, the mixing effect occurs due to its unequal distances to the two strap cells, which couples the ground noise into substrate. The location-dependent noise phase shift and accompanied mixing effects induce varied substrate noise and voltage difference between the source and bulk of the NMOS transistors in memory cells, and cause their cell currents to fluctuate due to the body effect, as shown in Fig. 3. This makes the cell current distribution change wider than without the substrate noise variation.

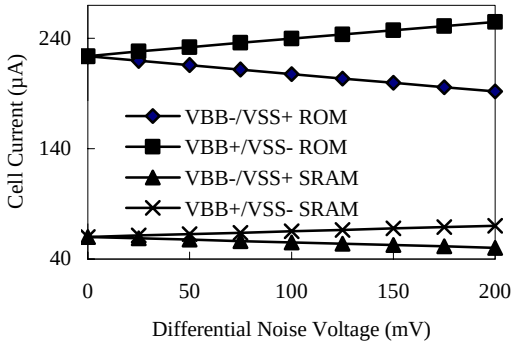

Fig. 3. Memory cell current fluctuations due to positive (VBB+/ VSS–) and negative (VBB–/VSS+) voltage difference between bulk and source on 6T SRAM and ROM cells.

In typical layouts of memories, the ground line of those memory cells that are on the same row is connected by a narrow metal wire in SRAM, and by a diffusion strip and/or metal wire in ROM. During an access operation, when a word line is selected, all memory cells connected to the word line are activated, sinking current to the same ground line. The more the memory cells connected to the word line, the larger the current sink. This simultaneous current sink to the same ground line raises the potential of the ground line and degrades the memory cell currents.

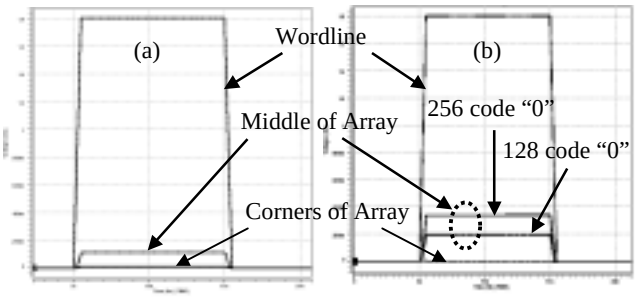

Fig. 4. Self-generated ground bounces in (a) 6T SRAM and (b) ROM with 512 and 256 cells per row, respectively.

Intuitively, the memory cells located at the middle of the array and between two strap cells have the worst-case word-line induced ground bounce. Hence, they suffer the most serious cell current degradation, as shown in Fig. 4, because the resistance (distance) to the power connectors of an embedded memory is largest. Moreover, different ROM codes introduce another factor of variation on the ground bounce, as in Fig. 4b. It determines the number of memory cells at the same row discharging to the ground line. Clearly, the divided word-line technique [15-17] can decrease the word-line induced ground bounce by reducing the number of activated memory cells on a row.

3. Supply and Substrate Noises on Configurable Memory Architectures

3.1. Bitline Tracking

The bitline tracking scheme has been adopted in configurable memory designs in view of its self-timed loading tracking capability and nice PVT characteristics. Instead of reserving a fixed timing margin which is often implemented by a long delay chain, the scheme employs an extra column of cell replicas to keep track of the voltage swings on normal bitlines. This dummy column is placed at the edge of a memory array. Its bit line is fed to the control circuit for controlling the sensing timing and word-line pulse. The tracking features are capable to satisfy the requirements for high speed and low power, while applicable to a variety of array configurations.

During the word-line pulse width, each selected memory cell develops the bitline swing by its own cell current. Clearly, the bitline swing developed by a *tail* bit, which has a lesser cell current than the other, is smaller. In the following, we shall discuss the sensing for the tail bit.

Let us assume that k tracking cells are connected to the dummy bit line. Their cell currents are summed together to develop the dummy bitline swing, as in (1).

$$I_{TRACK} = \frac{1}{k}\sum_{i=1}^{k} I_{CELL}(i) \tag{1}$$

If the average cell current of the tracking cells, I_{TRACK}, on the dummy bit line is close to the average cell current I_{TYP} of the memory array, the cell current variation ΔI_{CELL} tolerable by the bitline tracking scheme is the difference of cell currents between a typical bit and the tail bit; i.e.,

$$\Delta I_{CELL} = I_{TYP} - I_{TAIL} \tag{2}$$

The outcome of the design tradeoff between speed and manufacturability is the voltage difference of their bitline swings, $\Delta V_{TYP\text{-}TAIL}$. Then, the cell current distribution deviating no larger than ΔI_{CELL} is covered. In other words, the smaller the $\Delta V_{TYP\text{-}TAIL}$ is targeted, the smaller the ΔI_{CELL} is tolerated to correctly sense the tail bit. We have

$$\Delta V_{TYP-TAIL} = \Delta I_{CELL} \times T \tag{3}$$

where T is the word-line pulse width or the delay time to enable the sense amplifier. The bitline capacitance is normalized to 1.

Using the bitline tracking scheme, T is decided by the voltage swing on the dummy bit line. Since for the high-speed requirement, there should be little room left for further timing relaxation, the tracking accuracy on the bitline voltage, together with the cell current coverage, becomes very critical.

Current ratio and capacitance ratio [18] are two commonly used schemes in the bitline tracking circuit. The capacitance-ratio scheme activates one and only tracking cell ($k = 1$), while the current-ratio scheme activates multiple tracking cells ($k > 1$) at the same time.

The minimum cell current I_{SENSE}, which can be sensed correctly, varies by the value of I_{TRACK}.

$$I_{SENSE} = I_{TRACK} - \Delta I_{CELL} \tag{4}$$

That is, a large I_{TRACK} leads to fast sensing timing but small cell current coverage. On the other hand, a small I_{TRACK} leads to large cell current coverage but slow sensing timing. Some examples are given in Table 1.

As we can see now, the cell current fluctuations of the tracking cells pose a new DFM problem. Combining (2) and (4), we have

$$I_{SENSE} = I_{TAIL} + (I_{TRACK} - I_{TYP}) \quad (5)$$

When considering the nature of semiconductor manufacturing process, a tracking cell can have cell current, even at the opposite end of the distribution to the tail bit. This is somehow circumvented by simultaneously activating a sufficiently large number of tracking cells. Consequently, the current-ratio scheme can achieve better tracking accuracy on the average cell current of the memory array than the capacitance ratio scheme.

Table 1. Tail-Bit Sensing of 6T SRAM

Case	I_{TYP} (μA)	I_{TAIL} (μA)	I_{TRACK} (μA)	I_{SENSE} (μA)	Tail-Bit Sensing
$I_{TRACK} = I_{TYP}$	79.5	59.9	79.5	59.9	Pass
$I_{TRACK} > I_{TYP}$	79.5	59.9	85.6	64.4	Fail
$I_{TRACK} < I_{TYP}$	79.5	59.9	73.6	55.4	Pass

3.2. Supply and Substrate Noises

When supply and substrate noises occur uniformly in a memory array, the tracking cells of the dummy bit line experience the same variations in supply voltage and substrate bias as the memory cells to be tracked. This assures the dummy bitline swing keeping the relationship with the normal bitline swing. The bitline tracking technique is still capable of tracking the effects of supply and substrate noises.

The bitline tracking circuit needs to adjust the sensing timing *T*, however, based on the cell current fluctuations of the tracking cells to satisfy the targeted bitline swing and sensing margin. The relationship between ΔI_{CELL} and the average cell current of tracking cells can be written as follows (assuming a fixed value of $\Delta V_{TYP\text{-}TAIL}$)

$$\Delta I_{CELL-NOISE} = \Delta I_{CELL} \times (I_{TRACK-NOISE} / I_{TRACK}) \quad (6)$$

where $I_{TRACK\text{-}NOISE}$ is the average cell current of the tracking cells in the presence of supply and substrate noises. From (6), when $I_{TRACK\text{-}NOISE}$ is smaller than the original design target I_{TRACK}, the tolerable cell current degradation $\Delta I_{CELL\text{-}NOISE}$ under the influence of noises is smaller than ΔI_{CELL}.

This makes the tail bits near the lower bound of the design target fall out of the cell current coverage. In fact, the cell current distribution may become even wider, as mentioned in Section 2, and more tail bits fall out of the cell current coverage.

In a similar manner, we derive the minimum cell current $I_{SENSE\text{-}NOISE}$, which can be sensed correctly.

$$I_{SENSE-NOISE} = I_{TRACK-NOISE} \times (1 - \Delta I_{CELL} / I_{TRACK}) \quad (7)$$

Table 2 gives examples for SRAM using the conventional bitline tracking and operating with ground or substrate noise of 100mV. The tracking cells, acting as a static current source, do not seem to cope with the noises very well. As a result, the tail bit is not sensed correctly. From (7), it is easy to understand that $I_{TRACK\text{-}NOISE}$ needs to be reduced further on purpose, so as to lower $I_{SENSE\text{-}NOISE}$ and extend the cell current coverage.

Because the ground lines are usually noisy and couple the noises into substrate through substrate contacts, separating substrate bias from the ground lines is attractive for the substrate noise reduction. It tends to make the supply voltage and substrate bias less relevant. However, the voltage difference between them is not predictable for memories embedded in different SoCs, since the supply and substrate noises vary for different data patterns. This leads to a wider cell current distribution, although it may not change the average cell current of the memory array.

Table 2. Tail-Bit Sensing Using Conventional Bitline Tracking of 6T SRAM

Case	I_{TRACK} (μA)	I_{TAIL} (μA)	$I_{TRACK\text{-}NOISE}$ (μA)	$I_{SENSE\text{-}NOISE}$ (μA)	Tail-Bit Sensing
VSS+	79.5	51.6	69.7	52.5	Fail
VSS–	79.5	68.2	89.6	67.4	Pass
VBB+	79.5	61.6	81.6	61.5	Pass
VBB–	79.5	58.1	77.5	58.4	Fail
VBB+/VSS–	79.5	64.9	85.6	64.5	Pass
VBB–/VSS+	79.5	54.8	73.6	55.4	Fail

Under the extreme condition, where the tracking cells encounter the most negative voltage difference between the supply and substrate noises, while the tail bits encounter the most positive voltage difference, separating substrate bias would make the immunity to the substrate and power noises worse.

4. Dynamic Tracking Cluster Technique

As discussed earlier, the external and self-generated supply and substrate noises and their location-dependent voltage difference in embedded memories lead to a wide cell current distribution. The cell current degradation, particularly in the tail bits, causes sensing failure using the conventional *static* bitline tracking scheme.

Relaxing timing with a fixed amount of delay may not be a realistic solution in that the appropriate timing margin is hard to determine during the design phase of the embedded memories. On the other hand, pessimistically reserving too much timing margin for yield improvement reduces the speed performance and increases the power consumption.

We propose the use of a tracking cluster, which consists of *k* tracking cells and $n - k$ memory cells (see Fig. 5).

The value of *n* is usually chosen as a power of two (8, 16, or 32) and the value of *k* depending on the design tradeoff between speed, sensing margin, and cell current coverage.

The ground line is shared by the *n* cells in a tracking cluster and connected to the horizontal ground lines of the neighboring memory cells. However, it is vertically isolated from other tracking clusters. The physical layout assures all tracking cells in the tracking cluster have the same ground condition as the neighboring memory cells in the same row. Note that the horizontal ground lines are routed using multiple metal layers, for example, metal 1 and metal 3.

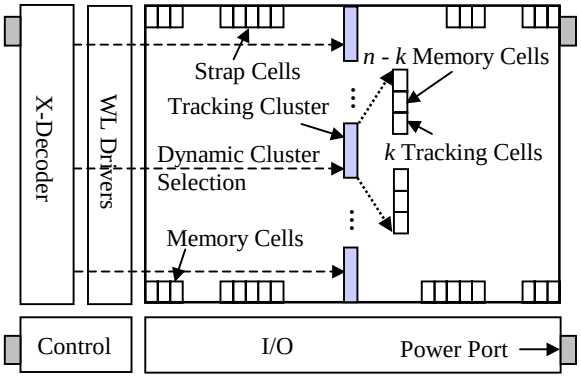

Fig. 5. Dynamic tracking clusters.architecture

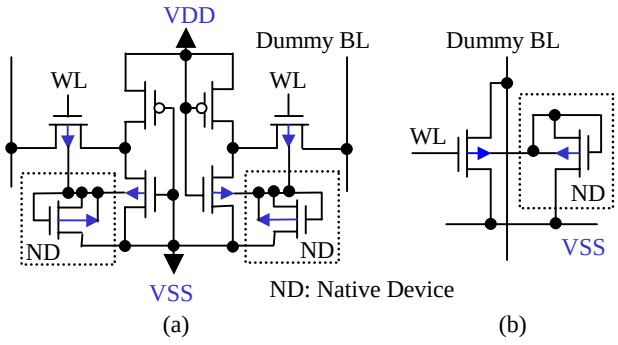

Fig. 6. Tracking cells for (a) 6T SRAM and (b) ROM.

The tracking cells are implemented with a pair of native NMOS transistors on the two sides of a modified 6T SRAM cell, or a native NMOS transistor on the side of a replica ROM cell, as showed in Fig. 6. The poly and active region of the modified SRAM and replica ROM cells have exactly the same layout pattern as normal ones. Only the metal connections in the SRAM cell are different so as to store a fixed value. Therefore, the cell current mismatch between the memory cell and the tracking cell can be minimized.

The drain and gate of the native NMOS transistor, which has zero threshold voltage, are shorted together to form a MOS diode. The diode will block the positive portion of the ground noise but pass the negative portion into the local substrate. On the other hand, the positive portion of the substrate noise will be filtered out around the diode area. Therefore, this diode assures the local substrate bias no larger than the local ground voltage around the tracking cells (see Fig. 7).

The tracking cluster is activated dynamically by a selection signal that is correlative to the accessed row in the memory array. All other tracking clusters then mimic the loading of a normal bitline. The selection of a tracking cluster can be shared with row decoders. The area overhead is minimal. The dynamic tracking clusters are physically placed between two strap cells at the middle of the memory array. Since the ground line of the tracking cluster and that of the accessed row have been connected together, the worst-case ground noise on the accessed row also reflects on the tracking cluster.

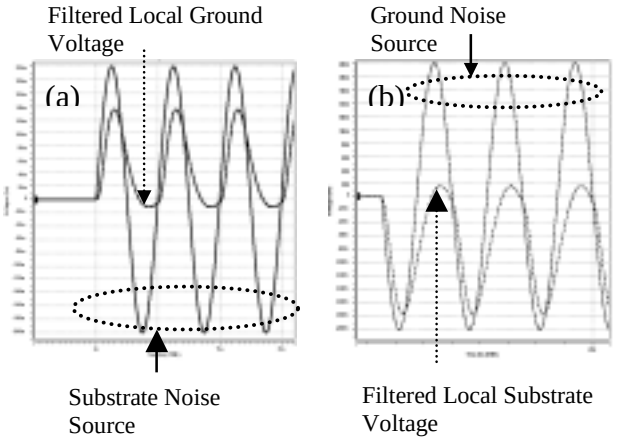

Fig. 7. Filtering effects in tracking cells with noise source from (a) substrate and (b) ground.

Table 3. Tail-Bit Sensing Using Dynamic Tracking Clusters of 6T SRAM

Case	I_{TRACK} (μA)	I_{TAIL} (μA)	$I_{TRACK\text{-}NOISE}$ (μA)	$I_{SENSE\text{-}NOISE}$ (μA)	Tail-bit Sensing
VSS+	79.5	51.6	59.6	44.9	Pass
VSS–	79.5	68.2	78.1	58.8	Pass
VBB+	79.5	61.6	69.3	52.2	Pass
VBB–	79.5	58.1	68.1	51.3	Pass
VBB+/VSS–	79.5	64.9	74.2	55.9	Pass
VBB–/VSS+	79.5	54.8	63.5	47.8	Pass

Table 3 gives examples for SRAM using the dynamic tracking cluster and operating with ground or substrate noise of 100mV (compare also to Table 2). The self-generated ground bounce of 114mV has been observed at the middle of the memory array with 512 cells per row. The proposed dynamic tracking cluster scheme can provide more accurate timing relaxing. It also increases the cell current coverage.

5. Conclusion

We have presented a study on the effects of supply and substrate noises on configurable SRAM and ROM. The ground line routing in the memory array is important for minimizing the cell current variations. A dynamic tracking cluster scheme is proposed to track the noise-induced cell current degradation when the supply and substrate noises occur, and provide necessary timing relaxation for correct sensing. This scheme achieves better noise immunity than the conventional bitline tracking scheme.

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