Layout Printability Optimization using a Silicon Simulation Methodology

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Abstract

The manufacturing complexity at the 90nm and 65nm technology nodes severally impacts the design. The traditional use of design rule based verification is no longer a guarantee of high yield once the chip has been manufactured. This paper describes many of the trends behind this phenomenon.

A new approach to layout that moves from an abstraction approach to a modeling approach is proposed. In this new methodology layouts are processed using resolution enhancement techniques and the results are simulated using lithographical models for a specific manufacturing process. The simulation results are used to identify critical regions in the layouts. The layouts are then optimized based on this analysis to improve their printability, manufacturability and yield.

1. Introduction

Being the fundamental building blocks of most chip designs, standard cells are the link between process and design. Standard cells must take into account all the complexity of the target process.

In the sub-wavelength domain, this process complexity is rapidly increasing, making a DRC based manual layout approach not only incredibly difficult but also inadequate. The problem lies in the design rules that are starting to fail in their attempt to use a discreet modeling approach on a continuous system.

High yield is getting very difficult to achieve when only meeting the basic DRC of a target process. A Design For Manufacturability (DFM) approach going beyond design rules must be used in order to optimize layouts for yield.

The core layouts of memories are already being manually optimized using silicon simulation technology. This time-consuming effort is worth doing because the memory cells are small and used million of times.

We propose a similar optimization approach for standard cells. The manual approach is not viable for libraries that contain hundreds of cells; therefore a more automated solution is recommended.

2. Problem Statement

Before optimizing a standard cell layout for yield one must understand yield. Yield is generally divided into two components; the first is random yield, due to particle contamination during manufacturing, and the second is systematic yield, due to the equipment and the materials used during manufacturing.

2.1 Systematic Defect Become Dominant

In the past systematic yield was a minor issue because of the high correlation between the layout geometries and the final printed image. This is no longer true as we move to sub-wavelength manufacturing. Instead we find systematic yield loss quickly catching up to random yield loss [1]. They are about equal at the 0.13um node and by the 65nm node, yield will be dominated by systematic yield problems.

Systematic yield can be divided into a number of factors. We cannot address all of them at the standard cell level but there are many that we can. These include:

- Lithography
  - Defocus
  - Mis-alignment
  - Field/aberrations
  - Dose variations
- Etching
  - Threshold
  - CD effects

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These issues can have a direct impact on a circuit by making it non-functional or reducing its performance.

2.2 Design Rule Explosion

To try and address systematic yield the design rules have been rapidly increasing in complexity. Between the 0.13um and the 90nm nodes the number of design rules has increased by 300%. The new rules can be attributed to new layers in the technology, new recommended rules and more complex conditional rules that are broken up into multiple sub rules.

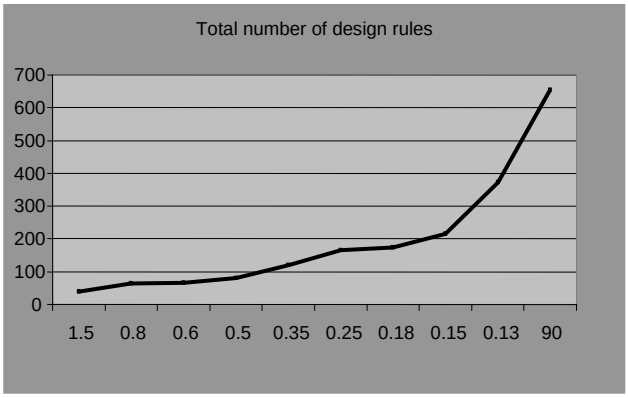

Figure 1: Design Rule Explosion

The new layers found in 90nm technologies are mostly coming from an increased number of metal layers. These new layers only increase the rule set by a small amount since the top metal layers are relatively simple to print.

The bulk of the new rules come from the new complex conditional rules and recommended rules.

Complex conditional rules are replacing simpler rules that would result in either a large area penalty or regions that would not yield. They often describe complex 2D topological situations with multiple valid solutions.

On top of the larger number of required design rules, the designer is also asked to use recommended rules wherever possible. The number of recommended rules between process nodes has quickly increased. Most of these rules are used to steer designers towards more conservative layouts in regions where the area is not impacted. Using these rules will make the end result more lithographically robust. It may also result in a simpler mask and possibly more space for applying Resolution Enhancement Techniques (RET).

Needless to say these are a true nightmare for layout designers since it greatly increases the complexity of the layout.

2.3 Manufacturing Complexity and RET

The driving force behind the rapid increase of both recommended rules and complex conditional rules stems from the same root cause. Design rules are starting to fail in their ability to properly model the complex 2D behavior of sub-wavelength manufacturing.

Manufacturing is now so aggressive that the ability to print a shape is dependant on a number of surrounding shapes and how much RET must and can be inserted in and around that shape.

When using 193nm steppers, how well a shape prints is dependent on all the shapes that are with-in ½ um of it. At the 65nm node this region can represent almost half the height of a cell and can enclose numerous shapes. Even complex rules only deal with two or three neighboring edges at once.

Extensive use of RET has also made predicting printing behavior all the more difficult.

For example the use of Off-Axis Illumination (OAI) benefits from the use of assist features. The ability to insert assist features is determined by the topology of a pattern and the space contained between its features. Assist features are lost and the printing quickly degrades when enough space is not available or two assist features collide.

The use of Alternating Phase Shift Masks (Alt-PSM) is another RET example where the insertion of phase shift shapes is so complex that it cannot easily be abstracted or modeled.

In sub-wavelength design the use of RET has moved from weak RET to strong RET where multiple techniques can be applied to the same layout. For example some 90nm processes use attenuated PSM with off-axis illumination and assist features simultaneously.

All of these problems are best addressed at the layout level and only using design rules does not appear to be a practical solution.

3. A DFM Approach

Before a layout can be optimized, a DFM analysis tool must first take the layout and simulate it through the target manufacturing process. The results must then be analyzed its to identify problem areas. These problem areas are used by an optimization tool that modifies the layout and deliver improved yield.

3.1 DFM Analysis

To reliably predict the printed quality of a design, its layout must go through all the RET steps normally used during manufacturing. The ability to simulate the lithography and etching effects of a layout is available today but will yield unreliable result if any of the RET is missing.

The technology to model both the lithographical and RET behaviors for specific layouts is already widely used during Mask Synthesis (MS). MS tool results are verified under different lithographical conditions using a dedicated verification tool based on silicon simulation such as Synopsys's SiVL. SiVL generates a contour of the final printed pattern and checks it with respect to the original layout. A flexible set of qualification criteria's may be specified by the user. This allows for a thorough assessment of quality.

All of this capability must be integrated into the standard cell layout methodology before we can even start analyzing layouts for yield.

3.3 Layout Optimization

If hundreds of standard cells are to be successfully processed, a layout optimization tool must be used on each layout. Synopsys's Cadabra tool set represents an ideal candidate for standard cell layout optimization. This product is already used extensively either to automatically create new cells or to automatically optimize existing cells. Its use of a transistor placer, a router and especially a 2D compactor offers a high level of flexibility.

AbraCAD already implements a number of DFM related rules. The most commonly used today include recommended extension on contacts and transistors, Electro-Migration rules on the width of metal wires and recommended spacing rules on field poly. The tool is able to optimize a layout for area and then apply recommended rules as efficiently as possible.

Recommended rules have been of great value to improve the quality of layouts but they are applied globally. A global approach does not reflect the non-linear behavior of the process that may print well at minimum rules in some areas and print poorly at recommended rules in others. Through DFM analysis, extra information can be provided to the optimization tool and help make trade-offs based on actual printed results.

4. Experimental Results

To evaluate the benefit of this methodology we used a set of production worthy 0.13um standard cell layouts. We then used Synopsys MS tools to evaluate the quality of printed results and finally used Synopsys's Cadabra tool to optimize these layouts.

4.1 DFM Analysis

For 0.13um the layouts are processed through model based OPC before they can be lithographically simulated. Simulation is done through focus and through dosage.

Figure 3 shows a half adder layout to the left and its printed poly image to its right, which was created using Synopsys's SiVL product. For best-printed performance an edge is best define by a large gray scale contrast between the feature and the field area.

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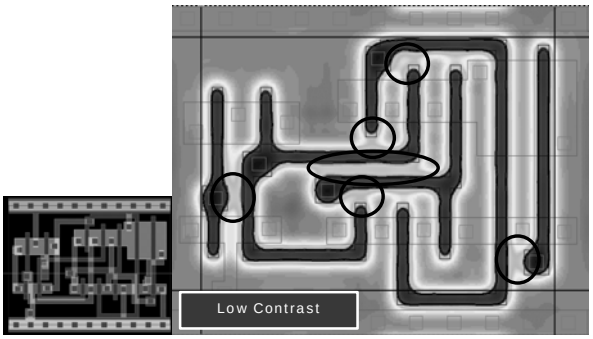
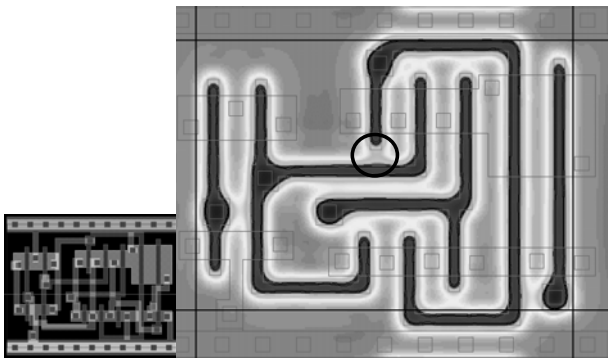


Figure 2: Original layout and its DFm analysis

This simulation shows at least six low contrast areas. These might result in significant dimensional variation causing performance loss, short end of lines on transistors causing large leakage currents, or short circuits causing failures. These problems will not manifest themselves in every cell but will reduce the overall yield of the product.

To improve this layout we can force the tool to increase the separation between features in as many of these areas as possible. The result is shown in Figure 3. All but one of our original problems have been fixed. The remaining one could not be resolved because of a lack of vertical free space in this fixed height standard cell.

Figure 3: Optimized Layout



To resolve this final issue the layout was modified by moving the contact found above the transistor to the side thus allowing more vertical movement. The final result found in Figure 4 shows improved contrast in all areas which will result in a much higher tolerance to process fluctuation.

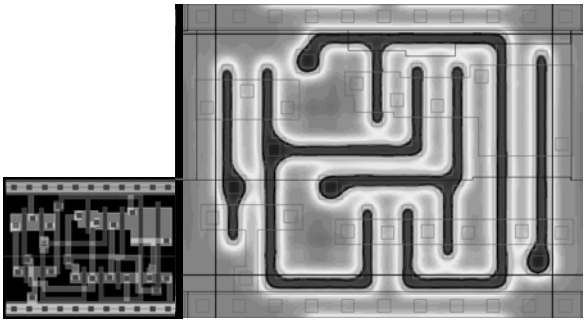


Figure 4: Final Optimized result

This example shows a straightforward case where spacing makes a difference to the quality of poly printing and an optimal result can be easily achieved. As the layout becomes more complicated so does the printed behavior.

4.2 DFM Optimization Trade-Offs

Figure 5 shows four version of the core of a scan flop. The first is the original layout without the use of any recommended rules. The printed image highlights a number of printing problems. Both a lack of contrast, as shown by the gray tone, and poor CD control, shown with black contour lines, can be observed.

To resolve these issues, see second image, we applied a recommended spacing rule between all poly edges. This has resolved many of our problems but not all. One important gate found to the left still doesn't print correctly. This layout did not have enough available free space to meet the recommended rule without an area penalty.

If we force the recommended rule around this gate we get the same behavior on a different gate found at the right of the layout. To properly optimize this layout a trade-off is needed were the available free space is shared between the two gates (see fourth image). If these gates have a different environment then the space needed for an optimal result on each gate can be different. Using the simulated results we can identify how much space is needed for each case and make a balanced trade-off.

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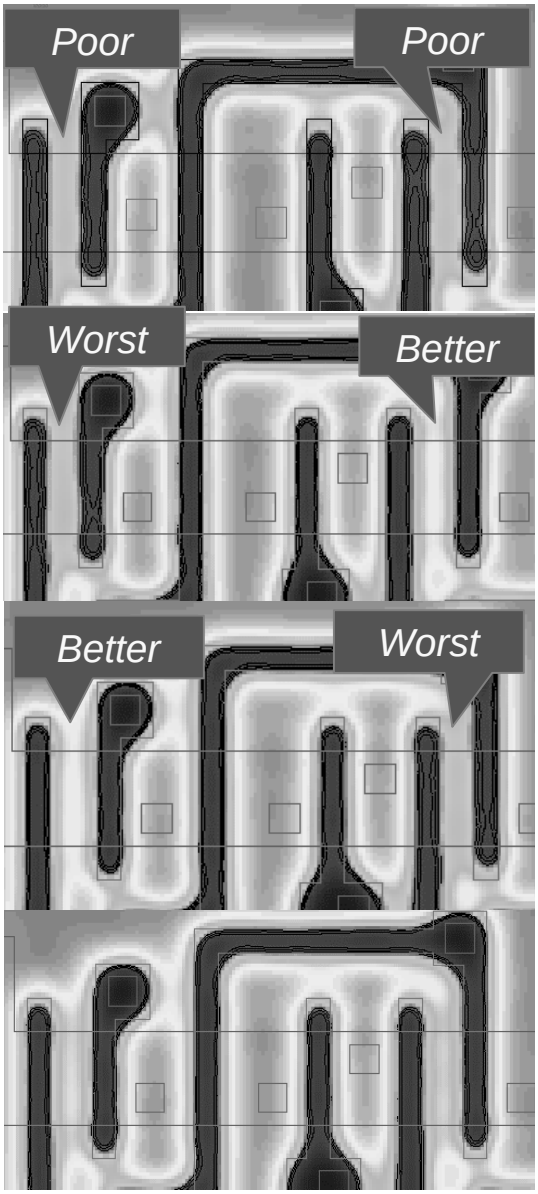
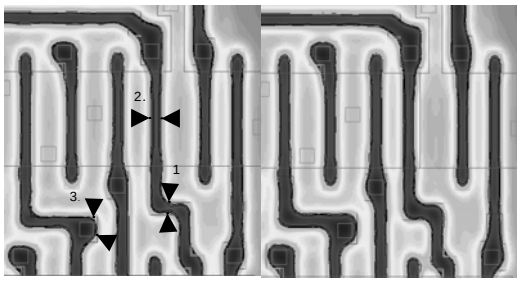


Figure 5: Original Layout
2. Recommended Rule
3. Recommended Rule Forced on Leftmost Gate
4. Space Shared Between Gates

4.3 Optimization Factors

The lithographical performance of a given layout is controlled by many factors. We have optimized the CD control and separation contrast of layouts but more can be done for improved yield. To truly make a layout robust Gate CD, field poly CD, contact extension and other aspects of the design must be optimized. Figure 6 shows a layout that has been fully



optimized. The contours found to the right are much better defined and deliver a solid pattern at various process settings.

Figure 6: Optimization of field polys, Contact Extensions and Gate CDs

We now have a robust layout that can better tolerate changes in focus, mask alignment and dosage but how much improvement have we achieved?

4.4 Parametric Performance

The most sensitive part of a layout is its transistors. Transistor performance is dictated by how much their width and length change from die to die due to process changes. To better understand the CD performance of our last example we analyzed its defocus performance.

We select a transistor that was manifesting poor lithographical performance in the original layout and perform a number of 1D analyses on its cross section. Our analysis involved finding the common depth of focus window on this gate for a maximum of 10% of gate length change. We can see from Figure 7 that our original layout should yield for a focus deviation of up to 200nm giving us a depth of focus window of 400nm.

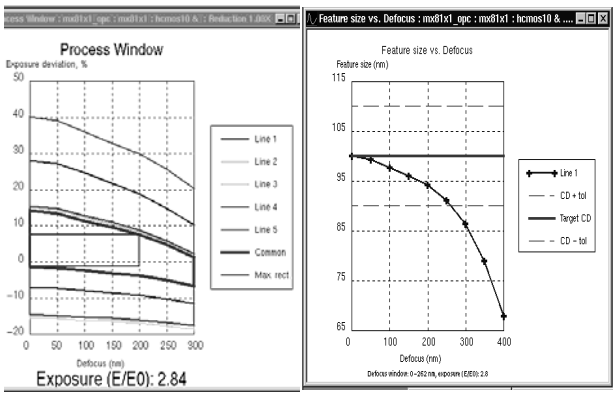


Figure 7: Original Layout Defocus Performance

When we apply the same analysis on our optimized results the numbers have improved by 20% with a 100nm improvement in the depth of focus window.

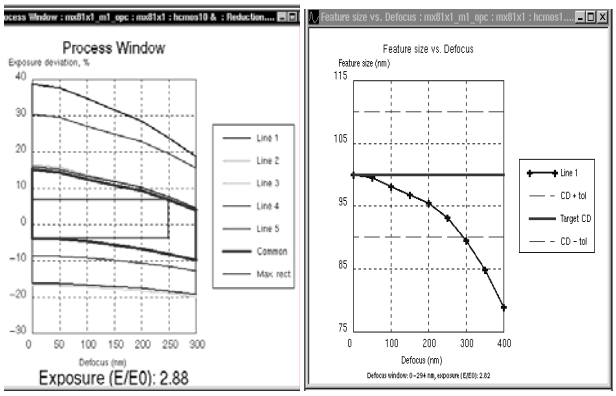


Figure 8: Optimized Layout Defocus Performance

Even with the good lithographical performance of our 0.13um process we are easily getting a 20% improvement. The amount of improvement found using this methodology will quickly increase as it gets applied to the 90nm and 65nm process nodes.

5. Applications

The layout optimization methodology described in this paper can be used in many different ways.

It may be used for yield optimization of library cells. All cells of a library can now be both qualified and optimized for a target process.

It can also be used by the process development team [2] or even design teams to help analyze the impact of design rules on layout density and print quality. With design rule complexity increasing, it's very hard to predict how a new design rule, an ECO change or a rule waiver impacts a layout's printability.

Designers with strong relationships with their Fabs may also use this flow to improve density. This would require violating some of the design rules and relying on their DFM flow to guarantee a minimum print quality.

6. Conclusion

In this paper we have described many of the challenges the industry is facing when implementing a deep sub-micron design. We have described how the current use of design rules even with recommended rules is limited in its ability to achieve both yield and density.

A lithography aware optimization was shown and evaluated for it flexibility and it ability to improve both printing and parametric performance of layouts.

7. References

[1] C. N. Berglund, "Trends in systematic non-particle yield loss mechanisms and the implication for IC design", *SPIE 2003.*

[2] Dipankar Pramanik, Michel Cote, "Lithography Driven Layout of Logic Cells for 65nm node", SPIE 2003