# A New Multi-Ramp Driver Model with RLC Interconnect Load

Lakshmi K. Vakati
Dept. of ECE, University of Arizona
Tucson, AZ 85721
520.882.4391
vakatil@ece.arizona.edu

Janet Wang
Dept. of ECE, University of Arizona
Tucson, AZ 85721
520.219.9057
wml@ece.arizona.edu

## ABSTRACT
As the feature size is scaled down to 90 nm and below, fundamental modeling changes, such as the nonlinearity and higher frequencies of signals, require driver-load models to take into account propagation delay and slew rates. The conventional single Ceff (one-ramp) with lumped RC model is no longer accurate. In this paper we propose a new multi-ramp model with general RLC interconnects as loads. This new model accurately predicts both the 50% delay and the overall output waveform shape with inductance effects.

## Categories and Subject Descriptors
B.7.2 [**Integrated Circuits**]: Design Aids, B.8.2 **[Performance and Reliability]**: Performance Analysis and Design Aids

## General Terms
Performance, Design

## Keywords
Interconnect Modeling, Multi-Ramp Driver Model, Transmission line effects, Inductance Criteria, Effective Capacitance.

## 1. INTRODUCTION
The one-ramp single Ceff driver model [2][9] has been the cornerstone for driver delay and slope calculation. However, at 90 nm and below, it can generate delay errors and cause timing failures when used in conjunction with lumped RC load model. In order to capture the overall waveform shape at outputs, it is important to improve the accuracy of both the driver's model and the driven load's model.

Current work in driver-load modeling techniques have been focused on developing driver's model and output load model incoherently. Some important properties of nanometer designs, such as nonlinearity and higher frequency of the signals, have been neglected. As a result, both the inductance effect and the time of flight of propagated signals are not captured in the existing driver-load models. For example, in [10], driver load is modeled as RC circuit and a pi-model is synthesized by matching

the first three moments of driving point admittance. However, the pi-model may no longer be synthesized if the inductive effects are significant.

In [6], a new driving point model, similar in spirit to the RC pi-model, is proposed for on-chip interconnect wires with inductance. Yet, the model is based on matching the first four moments of driving point admittance. It may produce fake ringing and lose the time of flight effects. In [1], the authors proposed a two-ramp driver model to capture the time of flight effects. Then again, they model the driving point admittance by matching the first five moments. Their model may fail for interconnects with noticeable inductance effects.

In this paper, we present a new multi-ramp driver-load model. The driver's load is modeled as a distributed interconnect and is mapped to an effective capacitance value. Our model predicts both delay and slew accurately at no additional computation cost compared to [1].

The reason behind mapping the driving point admittance model to an effective capacitance value is to resolve the incompatibility that exists between the pre-characterized look-up tables and RC/RLC loads. Traditionally gate delays are pre-characterized in terms of input transition time and output load capacitance using detailed circuit simulators such as SPICE and implemented using look-up tables. However RC/RLC loads are incompatible with existing pre-characterized look-up tables. This incompatibility is resolved by mapping the driving point admittance model to an "effective capacitance" value. Pillage et al. [9] mapped RC pi-model load to an effective capacitance value and this effective capacitance based methodology has been extended to RLC interconnects by Arunachalam et al in [2].

The paper is organized as follows. We review the performance criteria to evaluate the importance of on-chip inductance and the concept of transmission line theory in the next section. Section 3 describes the proposed model including the implementation specifics and a summary of the modeling flow. In section 4 we present experimental results that show the effectiveness of the proposed model. And we conclude in section 5.

## 2. BACKGROUND
Deutsch et al. provided detailed conditional expressions to determine when distributed interconnect effects (usually modeled as transmission lines) are important for on-chip interconnects [3]. Consider a point to point net with length l, characteristic impedance $Z_0$, resistance, capacitance and inductance per unit length R, C and L, total capacitance $C_T$, and driven by a source impedance $Z_{drv}$. The line inductance needs to be included when

$$Z_{drv} < Z_0 \quad (1.a)$$

$$\frac{Rl}{2Z_0} < 1 \quad (1.b) \qquad (1)$$


*ISPD'04*, April 18-21, 2004, Phoenix, Arizona, USA.

$$T_r < 2T_f \quad (1.c)$$

$$C_L << Cl, C_T \approx Cl \quad (1.d)$$

According to transmission line theory when $Z_{drv} = Z_o$ there will be no reflections at the near end. But it is necessary to over-drive the line to minimize delays. The second condition (1.b) is introduced to ensure that the attenuation of the wave at the sink is small. If the attenuation constant is greater than one, the magnitude of reflections decrease and the RLC approximation coincides the RC approximation. The third condition (1.c) is introduced to ensure that the line is long enough relative to the rise time of the signal. $T_r$ is the rise time at the output of the driver. It was proved in [5] that inductance effects had little dependence on the driver's input transition times but were heavily dependent on the driver's output transition times. When the rise time is much larger than the time of flight reflections come back to the source end even before the output has risen to the initial step. Hence the waveform coincides with RC approximation.

When the criteria given by (1) are satisfied inductance of the line cannot be ignored. These criteria are satisfied in case of global interconnects whose resistance is less than 100 Ω/cm. The driver output waveform of one such interconnect is as shown in Figure 1.

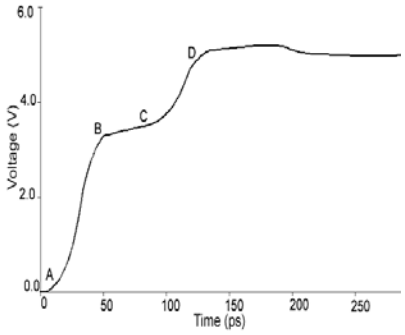



**Figure 1. Driver output waveform of a 5mm RLC line driven by a 75X inverter. (R=70 ohm/cm, L=5.64 nH/cm, C=1.2 pF/cm)**

As shown in Figure 1. the driver output waveform of an interconnect with significant inductance is not smooth as in RC cases and exhibits inflection points. The nature of the above waveform can be explained based on transmission line theory. First the output rises to an initial step (AB) and then, since the rise time is less or comparable to twice the time of flight delay, it waits for the reflections to return from the far end. The waiting period is $2T_f - T_r$ shown by the plateau (BC). Once the reflections return from the far end the output rises to another step (CD). The height of the initial step during the transition is given by,

$$\text{Height of initial step} = V_{DD} * f \text{, where } f = \frac{Z_0}{Z_0 + Z_{drv}} \quad (2)$$

Since $Z_{drv}$ is less than $Z_o$ the height of the initial step is greater than 50% of $V_{DD}$. The first reflection overshoots $V_{DD}$ but the magnitude of the overshoot is in general negligible.

## 3. PROPOSED MODEL

From the previous discussion, it is clear that on-chip interconnects behave like transmission lines when the inductance criteria are satisfied. Hence we use admittance of a distributed lossy transmission line to model the driving point admittance. Ideally the driver output waveform should be modeled as a multipiecewise linear waveform or multi-ramp to capture the complete waveform including multiple reflections. But as the magnitude of the initial step is greater than 50% $V_{DD}$, only the first reflection is prominent. The overshoots and undershoots due to later reflections are negligible. As such we require a three-piece linear waveform to model the initial step, the plateau and the first reflection. The slope of the plateau depends on the equivalent capacitance of the transmission line. In most practical cases the plateau has minor slope though not clear flat as shown in Figure 2.

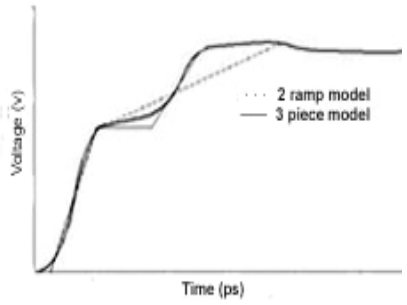



**Figure 2. Driver output waveform, 3-piece and 2-ramp approximations**

So, as shown in Figure 2, representing the plateau by a flat step is more appropriate than the approach of finding a ramp that fits both the plateau and the first reflection [1]. The approach in [1] gives accurate delay prediction but may fail in accurate slew prediction. Though fitting the plateau with a linear piece rather than a flat step works better, it adds to the computational cost and it does not achieve noticeably better delay and slew accuracy. Hence we model the initial step by a ramp and the plateau by a flat step and the first reflection by another ramp. When inductive effects are not significant the entire transition can be modeled by one ramp. But if resistance shielding effects are predominant gate resistor model should be used to capture the exponential tail. Figure 3 shows our simplified driver output model. To model the driver output waveform as shown in Figure 3, we need to determine the slope of each ramp and the voltage breakpoint. Voltage breakpoint in our case is the voltage point the initial step rises to and is calculated by Equation 2.

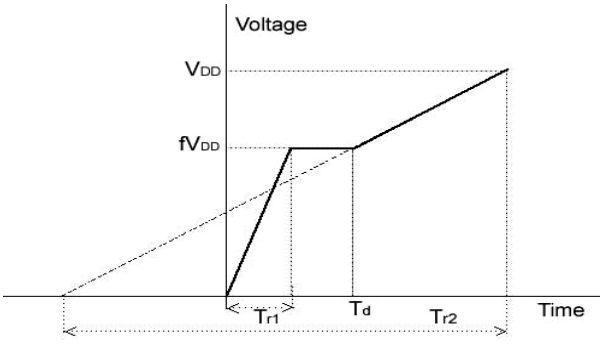



**Figure 3. Simplified three-piece model of driver output waveform**

The slope of the first ramp is ($fV_{DD}/T_{r1}$) and the slope of the second ramp is ($V_{DD}/T_{r2}$). The expressions are given by,

$$V(t) = fV_{DD}\frac{t}{T_{r1}} \qquad 0 < t < T_{r1}$$

$$V(t) = V_{DD}\frac{t}{T_{r2}} + \left(1 - \frac{T_d}{fT_{r2}}\right)fV_{DD} \quad T_d < t < T_d + (1-f)T_{r2} \quad (3)$$

Here $T_d = 2T_f$ .

As we discussed in section 1, the interconnect model should be mapped to an effective capacitance value to resolve the incompatibility that exists between pre-characterized look-up tables and RC/RLC loads. The approach to determine the effective capacitance value is to determine the capacitance load that has the same average current (therefore the same total charge transfer) as the transmission line model load. The charge averaging is for a finite period of time which we will refer to as the active region. The determination of this active region is critical to an accurate approximation. It was shown in [9] that equating the charge up to 50% point captures delay accurately, but fails in modeling the tail portion of the transition. Also equating the charge up to 100% point will not address this problem as this approach yields an averaged curve where both the delay and slew may be inaccurate [1]. A single effective capacitance cannot model the entire transition accurately. So we find two effective capacitances, where the first effective capacitance models the first ramp and the second effective capacitance models the second ramp.

## 3.1 Implementation

The first effective capacitance is obtained by equating the charge transfer required by the admittance model and the capacitance value during the transition of the first ramp. The second capacitance is obtained by equating the charge transfer during the transition of the second ramp. We modeled the interconnect as a distributed lossy transmission line. As such we need to compute the moments of input admittance (impedance) of the transmission line to model the interconnect.

Consider a transmission line terminated into a load ($Z_L$) as shown in Figure 4.

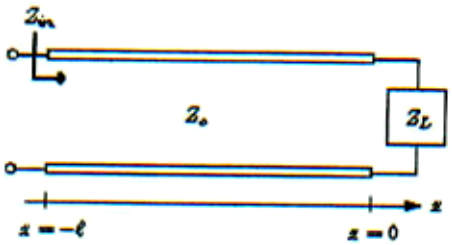



**Figure 4. Transmission line terminated into load $Z_L$**

The voltage and current on the transmission line as functions of z are of the form

$$V(x) = V_+(e^{-jkx} + \Gamma_L e^{jkx})$$

$$I(x) = \frac{V_+}{Z_o}(e^{-jkx} - \Gamma_L e^{jkx}) \quad (4)$$

The ratio of voltage to current at the input end is known as the input impedance ($Z_{in}$). It can be calculated from its definition,

$$Z_{in} = \frac{V(x=-l)}{I(x=-l)} = Z_o\frac{e^{jkl} + \Gamma_L e^{-jkl}}{e^{jkl} - \Gamma_L e^{-jkl}} \quad (5)$$

where $\Gamma_L$ is the reflection coefficient at the load and is given by

$$\Gamma_L = \frac{Z_L - Z_o}{Z_L + Z_o} \quad (6)$$

and $Z_o$ is the characteristic impedance of the line. For short rise times or high frequencies a transmission line displays a characteristic impedance (50 – 300 Ω), depending on its materials and physical dimensions.

In Table 1 we compare $Z_{in}$ and $Z_o$ for lines of different dimensions. It is obvious from Table 1 that at higher frequencies input impedance of the line is infact equal to the characteristic impedance. Hence we use characteristic admittance of the line in calculating Ceff.

**Table – 1 $Z_{in}$ and $Z_o$ comparison results**

| Len/Wid mm/µm | Line parasitics R(Ω)/L(nH)/C(pF) | Input Slew (ps) | $\frac{Z_{in}}{Z_0}$ |
|---|---|---|---|
| 4/1.6 | 56.3/4.98/1.67 | 50 | 1.0002 |
| 5/1.6 | 72/6.40/1.61 | 50 | 1.0000 |
| 5/2.2 | 56/6.30/1.76 | 50 | 1.0000 |
| 6/1.6 | 94/7.82/1.64 | 100 | 1.0003 |
| 6/2.2 | 77.4/7.28/1.80 | 100 | 1.0003 |

The characteristic admittance is given by,

$$Y(s) = \sqrt{\frac{G + sC}{R + sL}} \quad (7)$$

$$Y(s) = \sqrt{\frac{C}{L}}\sqrt{\frac{1 + \frac{G}{C}y}{1 + \frac{R}{L}y}} \quad (8)$$

where $y = \frac{1}{s}$. Y(s) can be expanded into a Maclaurin series of y around y = 0, or s = ∞. Therefore,

$$\sqrt{\frac{1+\frac{G}{C}y}{1+\frac{R}{L}y}} = 1 + m1y + m2y^2 + \cdots + mky^k + \cdots \quad (9)$$

where k-th moment is

$$m_k = \frac{d^k \sqrt{\frac{1+\frac{G}{C}y}{1+\frac{R}{L}y}}}{dy^k} \qquad (10)$$

we calculate the first five moments and use them directly instead of mapping them to a lower order model. And we experimentally found that the first three moments are sufficient to capture the time of flight effects. Several techniques related to stability problems in moment matching and realizable models have been explained in detail in [4]. For the first ramp,

$$V(s) = \frac{fV_{DD}}{T_{r1}} \frac{1}{s^2} \qquad (11)$$

The current delivered to the interconnect is given by

$$I(s) = V(s)Y(s) = \sqrt{\frac{C}{L}} \frac{fV_{DD}}{T_{r1}} \frac{1}{s^2} \left( \frac{s^5 + m_1 s^4 + m_2 s^3 + m_3 s^2 + m_4 s + m_5}{s^5} \right) \qquad (12)$$

The first effective capacitance $C_{eff1}$ is the capacitance that requires the same charge transfer as the interconnect moments during the interval when the first ramp is in transition. Charge transferred to moments can be calculated by integrating I(t) from t = 0 to t = $T_{r1}$. The charge transfer associated with charging the effective capacitance for this interval is given by $C_{eff1} f V_{DD}$.

$$\int_0^{Tr1} I(t)dt = C_{eff1} f V_{DD} \qquad (13)$$

Solving the above equation for $C_{eff1}$

$$C_{eff1} = \sqrt{\frac{C}{L}} \sum_{n=0}^{5} m_n \frac{Tr1^{n+1}}{(n+2)!} \qquad (14)$$

$C_{eff1}$ can be obtained by iterating on $T_{r1}$. We start with an initial guess of $C_{eff1}$ equal to the total capacitance and iteratively improve the effective capacitance until the value converges. $T_{r1}$ at each step can be obtained from pre-characterized cell information and the $T_{r1}$ corresponding to the converged $C_{eff1}$ is used to model the first ramp.

For the second ramp

$$V(s) = \frac{V_{DD}}{T_{r2}} \frac{1}{s^2} + \left(1 - \frac{T_d}{fT_{r2}}\right) fV_{DD} \frac{1}{s} \qquad (15)$$

The second effective capacitance $C_{eff2}$ is the capacitance that requires the same charge transfer as the interconnect moments during the interval when the second ramp is in transition. Charge transferred to interconnect moments can be calculated by integrating I(t) from t = $T_d$ to t = $T_d$ + (1-f)$T_{r2}$. The charge associated with charging the effective capacitance for this interval is given by $C_{eff2}$ (1-f)$V_{DD}$.

$$\int_{Td}^{Td+(1-f)Tr2} I(t)dt = C_{eff2}(1-f)V_{DD} \qquad (16)$$

solving the above equation for $C_{eff2}$

$$C_{eff2} = a\left[\sum_{n=0}^{5} \frac{m_n(A^{n+2} - B^{n+2})}{(n+2)!}\right] + b\left[\sum_{n=0}^{5} \frac{m_n(A^{n+1} - B^{n+1})}{(n+1)!}\right]$$

$$a = \frac{1}{T_{r2}(1-f)}$$

$$b = \left(1 - \frac{T_d}{fT_{r2}}\right)\left(\frac{f}{1-f}\right) \qquad (17)$$

$$A = T_d + (1-f)T_{r2}$$

$$B = T_d$$

$C_{eff2}$ can be calculated by iterating on $T_{r2}$. However $T_{r2}$ calculated this way needs to be modified. The idea behind modeling the plateau by a flat step is that there is no charge transfer during this period ($T_d$ – $T_{r1}$). Since effective capacitance is calculated by equating charge transfer, the $T_{r2}$ corresponding to the converged $C_{eff2}$, should be modified to include this plateau time.

$$T_{r2n} = T_{r2} + T_d - T_{r1} \qquad (18)$$

The modeling of driver output waveform requires calculating voltage breakpoint apart from determining slope of the two ramps. In order to model the voltage breakpoint we need to calculate on-resistance of the driver. We model on-resistance by a similar approach as adopted by thevinin models [11].

$$R_S = \frac{t_{90}(t_{in}, C_L) - t_{50}(t_{in}, C_L)}{\ln 5 C_L} \qquad (19)$$

Ideally one should find an effective capacitance and calculate on-resistance of the driver for this value of the load capacitance. However resistance does not change significantly by using total capacitance instead of effective capacitance [1].

Based on the above modeling a reduced order circuit can be synthesized for RLC interconnects. In [6] a driving point model, similar in spirit to the RC pi-model, was synthesized for on-chip interconnects with inductance. They modeled the interconnect by lumped RLC elements with ten segments representing a 1 mm wire, where each segment is made of a R, L and a C to ground. As their synthesis was based on matching the first four moments of the input admittance of a lumped model it failed to capture the time of flight effects. Since our synthesis is based on the exact driving point admittance (admittance of a distributed model) rather than the admittance of a lumped model the near end and far end waveforms obtained by our model are accurate.

When the inductive effects are not significant one effective capacitance is sufficient to model the entire transition accurately. This effective capacitance can be calculated by equating the charge over the entire region of transition. The equations to

calculate $C_{eff1}$ can be used with f = 1 to obtain this single effective capacitance.

## 3.2 Summary of modeling flow

Given the following information:

1. Line parasitics
2. precharacterized delay table for the driver

Steps for modeling driver output:

- Find admittance moments $m_1$, $m_2$, $m_3$, $m_4$ and $m_5$ using Equation 10.
- Find driver on-resistance using Equation 19 and calculate voltage breakpoint using Equation 2.
- Perform $C_{eff1}$ iterations using Equation 14 and compute $T_{r1}$.
- Check inductance criteria using Equation 1.

If inductance is significant

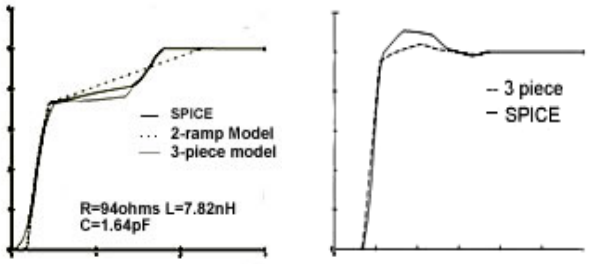
- Model plateau by a flat step for a period of $T_d - T_{r1}$.
- Perform $C_{eff2}$ iterations using Equation 17 and compute $T_{r2}$.
- Modify $T_{r2}$ to $T_{r2n}$ using Equation 18.
- Model the driver output waveform using $T_{r1}$, $T_{r2n}$ and voltage breakpoint.

If inductance is not significant

- Perform $C_{eff}$ iterations using Equation 14 with f=1 and compute $T_r$.
- Model the output as a single ramp.

# 4. RESULTS

We tested our three-piece model by sweeping line lengths from 4mm to 10 mm and line widths from 1.2µm to 2.6µm. We swept driver strengths from 50X to 125X and input transition times from 50ps to 150ps. We performed all experiments using 0.18µm CMOS technology. First we compare driving point waveforms obtained by our model with that of two-ramp model and SPICE simulations. Figure 5 shows one such waveform. Driver size is 100X and input slew is 50ps. Line length is 6 mm and line width is 1.6 µm. Figure 5a shows near end waveforms and Figure 5b compares corresponding far end waveforms. We classified our test cases into low and high inductance nets. Table 2 and 3 show a set of cases with noticeable and low inductance effects. SPICE delay and slew numbers are compared with our new model, two-ramp and single ramp modeling results. From the table it is clear that for noticeable inductance effect nets, slew predictions of 2-ramp modeling exhibits substantial error and our multi-ramp model provided good results. In our model, the average error in delay was 9% and the average error in the slew rates was 2.2%.




**5a** **5b**

**Figure 5. Three-piece driver output response compared to SPICE and two-ramp response**

**Table 2. SPICE, new model, two-ramp[1] and one-ramp model comparison results for nets with inductance effects**

| Len/ Wid mm /µm | Line parasitics R(Ω) L(nH) C(pF) | Driver Size | Input Slew (ps) | Delay (ps) | | | | Slew (ps) | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | SPICE | new model (%error) | 2 ramp model [1] (% error) | 1 ramp model (%error) | SPICE | new model (%error) | 2 ramp model [1] (%error) | 1 ramp model (% error) |
| 4/1.2 | 75/5.9/1.42 | 100X | 50 | 33.33 | 30.64 (-8.1%) | 28.85 (-13.4%) | 41.38 (24.2%) | 112.16 | 102.16 (-8.9%) | 138.36 (23.4%) | 82.77 (26.2%) |
| 4/1.4 | 67.7/5.3/1.52 | 100X | 50 | 34.61 | 31.30 (-9.5%) | 29.47 (-14.8%) | 41.69 (20.45%) | 113.51 | 103.46 (-8.8%) | 141.69 (24.8%) | 83.39 (-26.5%) |
| 4/1.6 | 56.3/4.98/1.67 | 100X | 50 | 36.03 | 32.58 (-9.6%) | 30.67 (-14.9%) | 43.68 (21.2%) | 114.86 | 110.60 (-3.7%) | 143.58 (25.0%) | 84.36 (-26.6%) |
| 5/1.2 | 81.5/6.44/1.57 | 100X | 50 | 33.68 | 29.91 (-11.9%) | 28.36 (-14.3%) | 51.28 (52.2%) | 140.09 | 137.03 (-2.2%) | 172.91 (23.4%) | 102.57 (-26.8%) |
| 5/1.6 | 72/6.40/1.61 | 100X | 50 | 34.12 | 30.32 (-11.1%) | 29.78 (-12.72) | 52.15 (52.84%) | 143.69 | 140.04 (-2.5%) | 180.25 (25.4%) | 104.30 (-27.4%) |
| 5/2.2 | 56/6.3/1.76 | 100X | 50 | 34.69 | 30.86 (-11.0%) | 29.92 (-13.7%) | 53.56 (54.39%) | 144.59 | 145.60 (0.7%) | 183.98 (27.2%) | 106.11 (-26.6%) |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 6/1.6 | 94/7.82/1.64 | 100X | 50 | 32.88 | 29.69 (-9.7%) | 28.65 (-12.8%) | 62.95 (91.4%) | 180.08 | 179.12 (-0.5%) | 224.57 (24.7%) | 125.91 (-30.1%) |
| 6/2.2 | 77.4/7.28/1.80 | 100X | 50 | 34.16 | 31.07 (-9.0%) | 30.92 (-9.5%) | 65.55 (91.9%) | 185.14 | 185.97 (0.4%) | 237.63 (28.3%) | 131.11 (-29.2%) |
| 6/2.4 | 62.8/6.74/1.92 | 100X | 50 | 35.14 | 32.28 (-8.1%) | 31.26 (-11.0%) | 66.99 (90.63%) | 189.18 | 190.33 (0.6%) | 240.27 (27.0%) | 134.00 (-29.2%) |

**Table 3. SPICE, new model and one-ramp model comparison results for low inductance nets**

| Len/Wid mm/µm | Line Parasitics R(Ω)/L(nH)/C(pF) | Driver Size | Input Slew (ps) | Delay(ps) | | | Slew(ps) | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | SPICE | 3 piece model (% error) | 1 ramp model (% error) | SPICE | 3 piece model (% error) | 1 ramp model (% error) |
| 5/1.6 | 72.4/5.1/1.11 | 100X | 50 | 32.88 | 29.41 (-10.5%) | 41.76 (27.0%) | 112.61 | 103.44 (-8.1%) | 83.54 (-25.8%) |
| 5/2 | 59.7/5/1.22 | 100X | 50 | 33.78 | 29.83 (-11.7%) | 43.25 (28.1%) | 116.67 | 108.74 (-6.8%) | 86.51 (-25.9%) |
| 5/2.5 | 49.5/4.8/1.31 | 100X | 50 | 34.60 | 30.65 (-11.4%) | 44.79 (29.5%) | 118.91 | 114.33 (-3.8%) | 89.58 (-24.7%) |
| 6/1.2 | 91/6.3/1.19 | 75X | 50 | 35.92 | 32.53 (-9.4%) | 56.12 (56.2%) | 153.15 | 149.80 (-2.2%) | 122.25 (-20.2%) |
| 6/1.6 | 82.3/6.2/1.33 | 75X | 50 | 36.93 | 33.73 (-8.7%) | 60.09 (62.7%) | 167.57 | 161.42 (-3.7%) | 120.19 (-28.3%) |
| 6/2 | 71.6/6/1.46 | 75X | 100 | 74.32 | 65.38 (-12.0%) | 95.63 (28.6%) | 209.46 | 186.01 (-11.2%) | 154.83 (-26.1%) |

# 5. CONCLUSIONS

In this paper we proposed a new multi-ramp model based on transmission line theory that accurately predicts delay and slew for both low and high inductance nets. Results show that our multi-ramp model significantly reduces the error incurred due to modeling the driver's load as a lumped interconnect and the approach of fitting a single ramp for both plateau and first reflection.

# 6. REFERENCES


[1] Kanak Agarwal, Dennis Sylvester, and David Blaauw, "An effective capacitance based driver output model for on-chip RLC interconnects," *Design Automation Conference*, 2003, pp. 376-381

[2] R. Arunachalam, F. Dartu, and L.T. Pileggi, "CMOS gate delay models for general RLC loading," Int. Conf Computer Design, 1997, pp. 224-229

[3] A. Deutsch *et al*., "When are transmission line effects important for on-chip interconnections?" *IEEE Trans. on Microwave Theory and Techniques*, 45, (Oct. 1997), 1836-1846.

[4] S. Lin and E. S. Kuh, "Pade approximation applied to lossy transmission line circuit simulation," *Int Symp. Circuits and Systems,* 1992, pp. 93-96.

[5] S. Lin, N. Chang, and O.S. Nakagawa, "Quick on-chip self and mutual inductance screen," *Int. Symp . Quality Electronic Design*, 2000, pp. 513-520.

[6] C.V. Kashyap and B.L. Krauter, "A realizable driving point model for on-chip interconnect with inductance," *Design Automation Conference*, 2000, pp. 190-195.

[7] B. Krauter, S. Mehrotra, and V. Chandramouli, "Including inductive effects in interconnect timing analysis," *Custom Integrated Circuits Conference*, 1999, pp. 445 -452.

[8] Y. Ismail, E. Friedman, and J. Neves, "Performance criteria for evaluating the importance of on-chip inductance," *Int. Symp.Circuits and Systems*, 1998, pp. 244-247.

[9] J. Qian, S. Pullela, and L.T. Pillage, "Modeling the effective capacitance for the RC interconnect of CMOS gates," *IEEE Trans. CAD*, 13, (Dec 1994), pp. 1526-1535.

[10] P.R. O'Brien and T.L. Savarino, "Modeling the driving point characteristic of resistive interconnect for accurate delay estimation," *Int. Conf. Computer Aided Design*, 1989, pp. 512-515.

[11] F. Dartu, N. Menezes, and L.T. Pileggi, "Performance computation for pre-characterized CMOS gates with RC loads," *IEEE Trans. CAD*, 15, (May 1996), pp. 544-553.

[12] L.T. Pillage and R. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Trans. CAD*, 9, (April 1990),pp.352-366.