Technology, Performance, and Computer-Aided Design of Three-Dimensional Integrated Circuits

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ABSTRACT

We present an overview of a new monolithic fabrication technology known as **three-dimensional integration**. 3-D integration refers to any process by which multiple conventional device layers may be stacked and electrically interconnected. By combining state-of-the-art single-wafer integration with a high-density inter-wafer interconnect, our 3-D integration process is capable of providing improved circuit performance in terms of metrics such as wire length, area, timing, and energy consumption. In this paper, we will discuss the overall 3-D integration process flow, as well as specific technological challenges and the issues they present to circuit designers. We will also describe how these issues may be tackled during the placement, routing, and layout stages of physical design. Finally, we will present some performance results that may be obtained by integrating circuits in three dimensions.

Categories and Subject Descriptors

B.7.1.{a,i} [**Integrated Circuits**]: Types and Design Styles—*advanced technologies, VLSI*; B.7.2.c [**Integrated Circuits**]: Design Aids—*placement and routing*

General Terms

Algorithms, Measurement, Performance, Design, Experimentation

Keywords

3-D integration, 3-D IC, 3-D VLSI, placement, routing, layout

1. INTRODUCTION

It is well known that interconnect consumes an inordinate portion of the energy and delay budgets available to circuit designers [1], and that this portion is ever increasing [2]. Many solutions to this problem come in the form of methodological improvements; however, few proposed solutions are scalable in a way that will continue to meet consumer performance demands as device technology improves. To meet such scaling demands, we must turn to a technology that also scales. One such technology is three-dimensional integration.

Three-dimensional integration consists of the aggregation of multiple conventional (i.e. single-wafer) integrated circuits in a stack, together with some means of interconnecting the individual conventional circuits. Each individual conventional circuit in a 3-D IC is called a "device layer" (though in some technologies it may be called a "wafer" for simplicity), and the 3-D wiring is thus referred to as "inter-layer interconnect." Figure 1 shows a sample 3-D IC in a candidate integration technology.

There are many approaches to fabricating three-dimensional integrated circuits. These may be classified as either packaging or monolithic approaches and may be characterized in terms of the maximum number of device layers and the maximum density of interconnects between these layers. We classify as packaging approaches those that involve the stacking of pre-packaged ICs. One example is MCM-V, a vertically-stacked multi-chip module technology [3]. Fully-integrated technologies, on the other hand, are those where multiple dice or wafers are stacked, or multiple active-

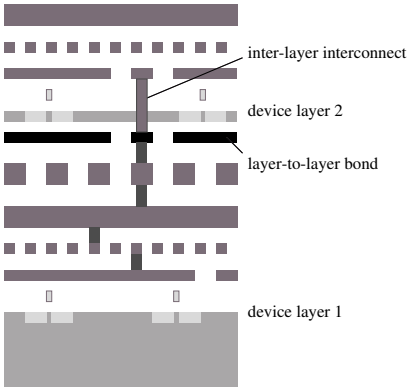

Figure 1: Wafer-bonded structure with two device layers and copper interconnect interface.

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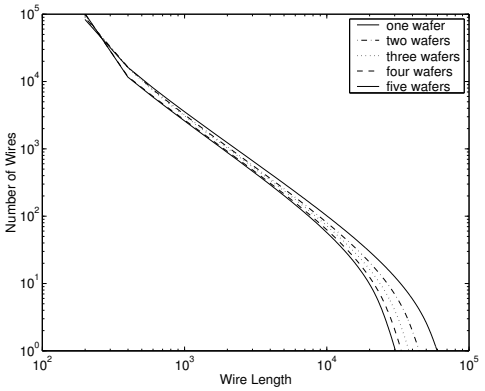

Figure 2: Predicted wire length distribution for a sample circuit as a function of the number of device layers used.

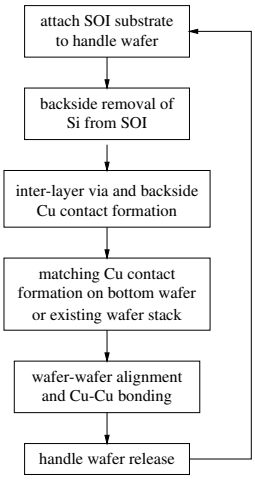

Figure 3: 3-D integration process flowchart.

device planes are fabricated on a single seed foundation, prior to packaging. Such technologies include solid-phase crystallization [4] and wafer bonding [5, 6]. There are other candidate 3-D integration technologies such as liquid-phase [7] and flip-chip.

Numerical studies have shown that for a variety of general and special-purpose circuits, 3-D integration provides significant benefit [8, 9, 10]. For example, as shown in Figure 2, the distribution of wires according to wire length is different for 3-D ICs using varying numbers of device layers. In particular, it is expected that for a typical custom-logic circuit with a modest number of device layers, the wire-length distribution will be shifted away from long, global wires towards having more short, local wires, thus lowering the total overall wire length and hopefully also the delay and energy consumption of the circuit.

In this paper, we will describe our process flow for monolithic three-dimensional integration. In doing so, we will identify challenges and opportunities both from the process point of view and from the viewpoint of circuit design. We will also provide an overview of our design tools for 3-D ICs, as well as some performance data arising out of our use of these tools on some sample circuits.

2. 3-D INTEGRATION PROCESS FLOW

2.1 Overview

In our 3-D integration scheme, multiple device wafers are sequentially bonded to each other using low-temperature copper- copper thermocompression. Figure 1 depicts our definition of a 3-D circuit, in which any number of device layers are both mechanically bonded and electrically interconnected using matching copper pads.

For circuit purposes, it is desirable to have the smallest possible lateral dimensions for the copper pads and inter-wafer vias. The ultimate determinant of these dimensions will be the wafer-wafer alignment tolerances during bonding and aspect-ratio limitations on the via creation. When the top device layer is a thin SOI wafer, as shown in Figure 1, the aspect ratio of the inter-wafer vias can be relaxed to around 3:1 or even 2:1 for ease in fabrication, while still maintaining a relatively high lateral density across the wafer.

The goal of our process flow is to create a 3-D stack by successive bonding of SOI device layers on top of each other. These device layers may be bonded *face-to-face*, where the front-side metallizations are adjacent, or *face-to-back*, as shown in Figure 1, where the oxide of one layer abuts the metallization of the other.

Figure 3 is a flowchart of such a process, in which the 3-D stack begins with the bonding of two device wafers. Subsequent device layers can be added to the stack in a short turn-around process loop. As seen in the chart, the majority of the processing steps revolve around the preparation of the SOI substrate prior to bonding.

We start with a typical SOI substrate (100 nm SOI / 400 nm buried oxide) that contains both CMOS devices and the corresponding multi-level interconnects. From a conventional process perspective, the substrate is essentially a "finished" circuit. In order to stack this SOI on top of another device layer, we first undertake backside substrate thinning to remove the bulk silicon. For mechanical support during grindback, it is imperative to attach the SOI to a handle wafer. Thinning and bonding processes are then executed, and the handle wafer must then be detached to complete the process.

Specifically, the process flow begins with a designated "top" wafer and an existing single wafer or 3-D stack of wafers (the "bottom" wafers). (300 / 50) nm thick copper/tantalum contact pads are patterned on top of the top SOI substrate. The substrate is then passivated by an overlayer of 500 nm PECVD oxide, followed by oxide CMP for global planarization. These copper pads will eventually participate in bonding with a subsequent (third) wafer, once the current top wafer becomes part of the 3-D stack. Once passivated and planarized, the SOI substrate is ready for handle wafer attachment, as will be detailed in subsection 2.4.

With the handle wafer in place, the next task involves the complete removal of the SOI bulk silicon using a combination of mechanical grindback and aqueous chemical etching that will stop selectively on the 400 nm buried-oxide (BOX) layer.

To start, 400-420 μm of the SOI bulk silicon are removed using grinding, while the remaining 80 to 100 μm of silicon are etched in a solution containing 4.38 M (20% wt) KOH at 80°C for approximately two hours. The solution has a silicon-to-oxide selectivity of about 300 : 1.

As can been seen in Figure 4, upon completion of the SOI substrate removal, inter-layer vias are created by etching through the BOX, SOI, and first inter-layer dielectric, finally stopping on metal layer M1. This is followed by PECVD oxide sidewall passivation and via filling using a damascene process. A typical via aspect ratio is around 2:1, with a via width of about 0.5 μm.

Next, (300 / 50 nm) thick copper/tantalum pads are patterned onto the inter-layer vias. The thinned SOI substrate in Figure 4,

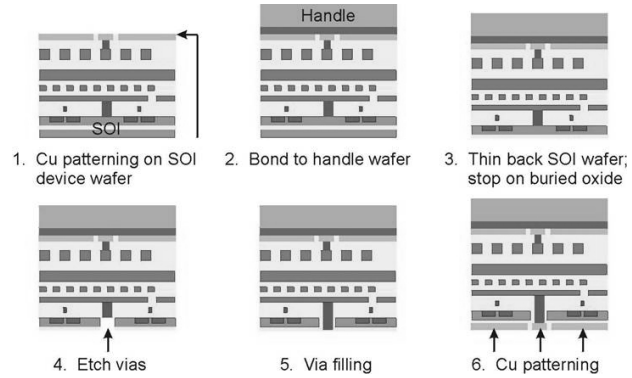

Figure 4: Handle-wafer attachment, grindback, via formation, and copper patterning steps of the wafer bonding process.

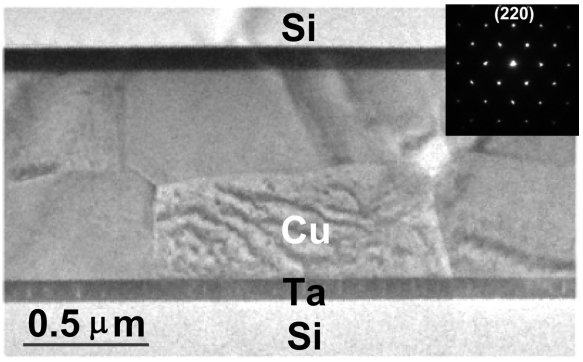

Figure 5: TEM images of the Cu-Cu bonded layer and the major diffraction pattern of single grains for selective area after 30 min. bonding and annealing at $400^{\circ}\mathrm{C}$ [12].

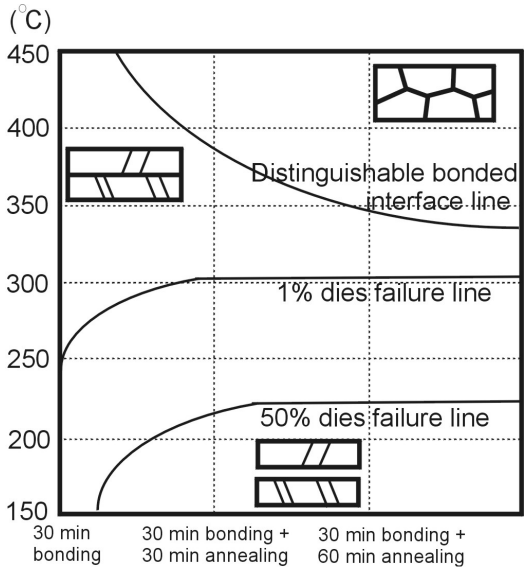

Figure 6: Morphology and strength map for copper wafer bonding under different bonding temperatures and conditions [13].

complete with backside inter-layer vias and copper bond pads, is now ready to be bonded to another CMOS device wafer with its own set of multilevel interconnects and copper/tantalum bond pads that mirror those of the thinned SOI.

The wafers are aligned, clamped, and transferred to a bonding chamber, where both substrates are heated to $300 - 400^{\circ}\mathrm{C}$ in vacuum and hot-pressed for 30 minutes under 4000 mbar of pressure. An optional further annealing at the bonding temperature for 30-60 minutes in nitrogen completes the copper-copper bond.

Finally, the handle wafer is released, and the resulting 3-D stack, largely resembling the initial 3-D stack or single wafer, is ready for the bonding of additional wafers as desired.

2.2 Process Optimization for Copper Wafer Bonding

For the purposes of designing 3-D integrated circuits, it is important to understand the process conditions under which such circuits may be fabricated. In some proposed technologies, the required 3-D integration steps may constrain the performance of devices or interconnect on some device layers of the circuit. We have performed several analyses that indicate that our process is fully CMOS compatible without introducing any "weak links" in the functionality or reliability of a given circuit.

The microstructure morphologies and oxide distribution of copper bonded wafers were examined by means of transmission electron microscopy (TEM) and energy dispersive spectrometer (EDS) [11]. Copper exhibits good bond properties when wafer contact occurs at $400^{\circ}\mathrm{C}$ and 4000 mbar for 30 min., followed by an anneal at $400^{\circ}\mathrm{C}$ for 30 min. in nitrogen ambient atmosphere. The distribution of different defects shows that the bonded layer became a homogeneous layer under these bonding conditions. The oxidation distribution in the bonded layer is uniform and sparse. Figure 5 shows a TEM image of the copper-copper bonded layer and the major diffraction pattern of single grains for selective area after 30 min. bonding and annealing at $400^{\circ}\mathrm{C}$ [12].

Evolution of microstructure morphologies and grain orientations of copper-copper bonded wafers during bonding and annealing were studied by means of transmission electron microscopy, electron diffraction and X-ray diffraction [12]. The bonded copper grain structure reaches steady state after post-bonding anneal.

The morphology and bond strength of copper-bonded wafer pairs prepared under different bonding/annealing temperatures and durations are presented in [13, 14]. The interfacial morphology was examined by transmission electron microscopy (TEM) while the bond strength was examined from a diesaw test. Physical mechanisms explaining the different roles of post-bonding anneals at temperatures above and below $300^{\circ}\mathrm{C}$ are shown in Figure 6. This map summarizing these results provides a useful reference on process conditions suitable for actual microelectronics fabrication and three-dimensional integrated circuits based on copper wafer bonding [13].

A novel test structure for the measurement of the contact resistance of bonded copper interconnects in 3-D integration technology was proposed and fabricated in [15]. This test structure requires a simple fabrication process and eliminates the possibility of measurement errors due to misalignment during bonding. Specific contact resistances of bonding interfaces with different interconnect sizes of approximately $10^{-8}\ \Omega \cdot \mathrm{cm}^2$ were measured. A reduction in specific contact resistance is obtained by longer anneal time. The specific contact resistance of bonded interconnects with longer anneal time does not change with interconnect sizes.

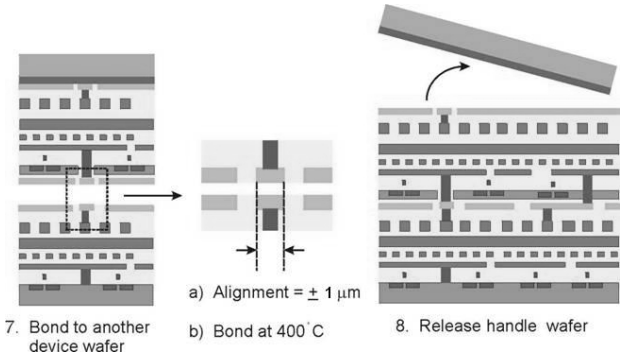

Figure 7: Thermocompression and handle release steps of the wafer bonding process.

2.3 Challenge #1: Wafer Alignment

Both wafer-to-wafer alignment and bonding are performed in an Electronic Vision EV 450 Aligner and AB1-PV Bonder [5, 11]. Since the system has an inherent $\pm 3\ \mu\mathrm{m}$ alignment tolerance, any copper bond pads less than or equal to 3 $\mu\mathrm{m}$ in width are unacceptable. Thus, wafer-to-wafer alignment is the ultimate factor in determining the inter-layer via density.

With better optical alignment systems, it is possible to decrease the copper pad size down to around 0.5 to 1 $\mu\mathrm{m}$, which corresponds to a substantial increase in via density.

2.4 Challenge #2: Handle Wafer Attachment and Release

The handle wafer must be attached with a special adhesive that is (a) strong enough to withstand vigorous shearing force from grinding, (b) chemically inert to hot aqueous hydroxide solutions, and (c) easily removed with another solution. Because hot basic solutions will usually delaminate organic polymers from their substrates, it is very difficult for CMOS-compatible polymer adhesives to satisfy all three criteria. However, these requirements can be met with a careful choice of metallic bonding layers; hence, one can use a copper-copper bond as the adhesion layer itself, while flanking layers of zirconium can be used as the "wafer release" medium. This is due to the fact that copper generally resists hydroxide attack, and zirconium dissolves extremely rapidly in dilute HF (much faster than does silicon dioxide). This handle wafer attachment scheme is shown below in Figure 7.

In this scheme, the substrate is bonded to a 100 nm LPCVD nitride handle wafer. On both the SOI substrate and the handle wafer, 150 nm zirconium and 300 nm copper are deposited in sequence. With no need for wafer-wafer alignment, the SOI and the nitride handler are simply bonded at $300 - 400^{\circ}\mathrm{C}$ in vaccuum with a persistent contact pressure of 4000 mbar for 30 min. The wafer pair may then undergo a further anneal in nitrogen, in which the copper-copper interface forms a strong bond that passes both the razor test [5, 11] and subsequent mechanical substrate grinding.

Alternatively, an oxide-oxide bond can be used to attach the handle wafer. This method has the advantage that the bond is materially distinct from the permanent copper-copper bond used for electrical and mechanical connectivity.

In this layer transfer method, the finished SOI wafer is coated with 1-2 $\mu\mathrm{m}$ of Plasma-Enhanced Chemical Vapor Deposition oxide (PECVD oxide). Since the PECVD oxide is porous, a low-temperature densification is performed at $350^{\circ}\mathrm{C}$ for 12 hours in inert nitrogen ambient. This step allows degassing from the porous silicon dioxide, which is detrimental to the bonding, to take place prior to bonding. Surface smoothness is very critical to successful wafer bonding, and it is well known that the PECVD oxide has a very rough surface. Therefore, it is necessary to smoothen the oxide surface by means of chemical mechanical polishing (CMP). It is also essential to ensure that a particle-free post-CMP oxide surface emerges from the CMP slurry. Since the SOI wafer-thinning step (silicon etching) comes partly in the form of a KOH chemical etch, the silicon handle wafer needs to be protected against KOH attack. It is well known that silicon dioxide is an effective etch stop layer during silicon KOH etch. So 5000 $\mathring{A}$ of oxide is grown on the handle wafer. High-dose, high-energy H^{+} ions are implanted into the handle wafer with the expected range of about 0.5 $\mu\mathrm{m}$. Hydrogen plays a role in wafer exfoliation during handle wafer release.

Prior to bonding, the SOI and the handle wafers are chemically cleaned, rinsed in deionized water, and dried. The two wafers are bonded face-to- face, i.e. thermal oxide (on the handle wafer) with PECVD oxide (on the SOI wafer) bonding, with no requirement for precision alignment at room temperature. In order to enhance the bonding strength, the bonded pair will be annealed at $300^{\circ}\mathrm{C}$. We have successful demonstrated the ability to bond thermal oxide to PECVD oxide with careful surface preparation [16]. The SOI wafer is ready for thinning now as described in Section 2.1. Upon formation of vertical electrical vias and copper pads on the BOX, the SOI wafer is aligned to the bottom wafer (a finished wafer with copper bonding pads) and bonded. This can be done at $350^{\circ}\mathrm{C}$ and 4000 mbar for 30 min. After bonding, the stack is annealed in nitrogen ambient for 30 min. at $400^{\circ}\mathrm{C}$ to allow copper grain growth that will enhance the bond. This step might potentially lead to handle wafer release as well. Under this condition, the hydrogen will cluster together and cause lateral cracking, thus releasing the handle wafer from the actual 3-D device stack. The remaining thin silicon (about 0.5 $\mu\mathrm{m}$) can be stripped away easily by a five-second dip in KOH solution.

3. CIRCUIT DESIGN OPPORTUNITIES AND CHALLENGES

3.1 Digital IC Design

Three-dimensional integration presents significant opportunities for digital system design. As seen in Figure 2, the wire-length distribution of a given circuit is expected to shift so that fewer long global wires are required to lay out the circuit. In order to determine ultimately what performance benefits may be obtained from this shift, it is necessary to place and route some sample circuits. In the following sections, we will describe our place-and-route methodology for 3-D ICs. Furthermore, using a methodology we will also describe shortly, we may evaluate the usefulness of 3-D integration technology in comparison with other potential means of achieving the same scalability. For example, "flip-chip" bonding (also known as chip-scale packaging) may be leveraged to create a likeness of 3-D integration. However, as shown in Figure 8, we can see that wafer bonding outperforms the packaging technology.

3.2 Mixed-Signal IC Design

3-D integration permits the realization of systems on a chip (SOC) and can result in substantial performance improvements. For example, 3-D integration using bonding allows monolithic integration of disparate technologies. A device layer that is optimized for analog circuits could be combined with another device layer that is optimized for logic, yielding optimal system performance. Also, a significant challenge to mixed-signal design is substrate noise coupling generated by high-speed digital circuits. Analog circuits lack

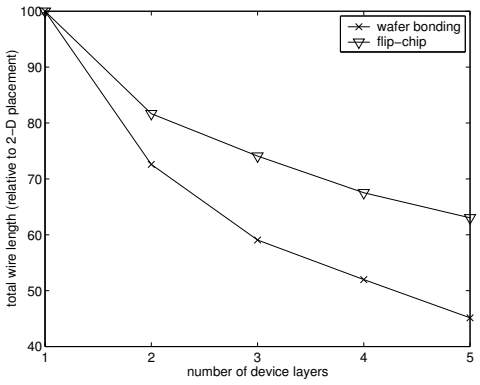

Figure 8: Total wire length (as a function of number of device layers) of a benchmark circuit, using wafer bonding vs. using flip-chip.

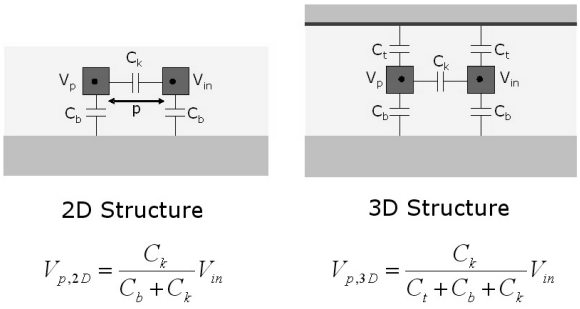

Figure 9: Signal-line charge sharing in 2-D and 3-D ICs.

the large noise margins of digital circuit and thus are easily corrupted by substrate noise. 3-D integration mitigates this coupling by breaking the resistive connection that exists because of a shared substrate. Nearly perfect isolation can be achieved by fabricating the analog and digital systems on separate substrates while communicating through high-density vias. Furthermore, crosstalk within a digital block as a result of capacitive coupling of switching signals can also be reduced in a 3-D design. The additional capacitance due to the presence of another device layer diverts field lines from the wire-wire interaction, thus reducing the wire-wire coupling as depicted in Figure 9. In Figure 10, V_p is the voltage induced in a wire as a result of a switching voltage, V_{in}, in an adjacent wire.

4. AUTOMATED DESIGN: PLACEMENT AND ROUTING

Our design tools are meant to replace existing tools in a digital design flow wherever such tools need to be aware of the three-dimensionality of the circuit. A simplified design flow is given in Figure 11. In order to adapt this flow for a 3-D integration technology, we have developed a standard-cell placement tool, global routing tool, and a layout editor for 3-D ICs [17, 18].

Our standard-cell place-and-route tool, PR3D, operates on circuit netlists in GSRC [19] or Cadence LEF/DEF [20] formats, either of which may be generated from Verilog or VHDL descriptions of the circuits. The user specifies the number of device layers to be targeted, as well as the wire-length cost of inter-layer vias relative to the cost of 2-D wire (for example, if least interconnect power is the target, the cost of inter-layer vias may be given as the capacitance of such vias relative to the capacitance of a unit length of 2-D

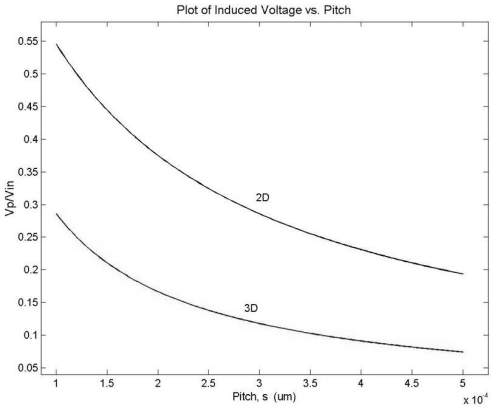

Figure 10: Induced voltage in an adjacent victim wire in 2-D and 3-D ICs.

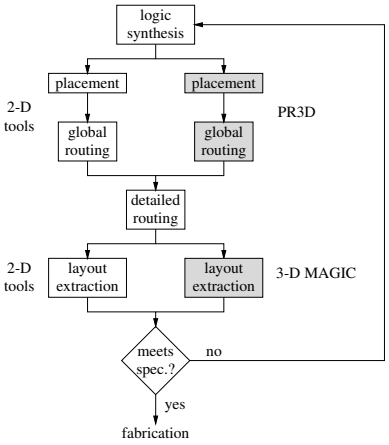

Figure 11: Design flow for 3-D integrated circuits. Highlighted areas indicate where our tools replace tools for conventional ICs.

wire). The user also must choose whether to minimize the total wire length or to minimize the number of inter-layer vias (for technologies where the inter-layer wire pitch dominates over other factors such as capacitance). Placement is performed using a min-cut partitioning algorithm [21] that we have adapted for 3-D placement [17].

Once placement is complete, global routing is performed in order to localize the routes taken by nets in the circuit. In our 3-D global router, we must allocate area for inter-layer vias: in the face-to-back configuration, such vias present obstacles not only for device placement, but also for routing in first-level metal. We perform the allocation of routes, including inter-layer vias, using a hierarchical algorithm based on [22]. When the locations of inter-layer vias have been set, the individual layers of the placement may be passed to existing tools for detailed routing.

Using our tools on the ISPD '98 set of 18 digital benchmark circuits [23], we have performed several analyses of the potential of 3-D integration [18]. In our first analysis (Figure 12), we show the total wire length of the average of these circuits as a function of number of device layers, determined from placement. We observe that relative to a 2-D (conventional single-die) placement, 28% to 51% reduction in total wire length is possible; we expect that capac-

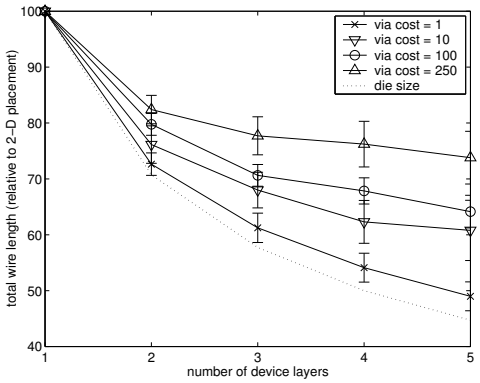

Figure 12: Total wire length (as a function of number of device layers) for various inter-layer via capacitances, obtained from placement. Total wire length is minimized by the placement tool. Via cost is the via capacitance expressed relative to the capacitance of one micron of metal wire.

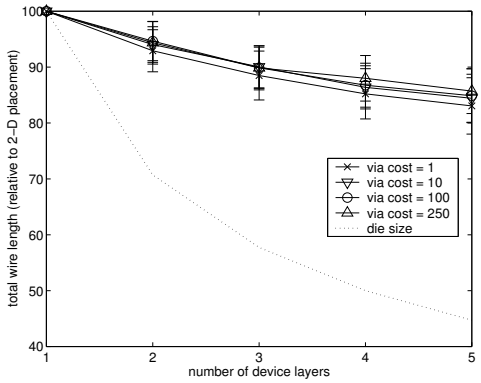

Figure 13: Total wire length (as a function of number of device layers) for various inter-layer via capacitances, obtained from placement. The number of inter-layer vias is minimized by the placement tool. Via cost is the via capacitance expressed relative to the capacitance of one micron of metal wire.

itance (and therefore energy consumption) follows the wire length. Furthermore, with our tool we can set the capacitance of an inter-layer via relative to the capacitance of an equal length of wiring from, say, metal 1. The four curves in the figure show quantitatively how as the inter-layer via capacitance increases, the benefit of 3-D integration decreases. We conclude that optimizing inter-layer interconnect is of key importance for 3-D integration technologies. As stated before, for example, we compare wafer bonding to flip-chip technology in Figure 8. (It is important to note that for three or more device layers, through-wafer vias must be used in conjunction with the solder bumps. However, in the two-wafer case, we assume a face-to-face implementation, where such vias are not required.) It is clear that technologies such as wafer bonding offer significant performance improvement even when compared to existing die-stacking methods.

Our second analysis, in Figure 13, shows the same experiment, but where we minimize the number of inter-layer vias (as opposed to minimizing the total wire length). We see that the benefit of 3-D integration is not so great here (up to 7% to 17% reduction in total wire length), but that the results are more immune to inter-layer via capacitance variation.

Figures 14 and 15 show the length of the longest wire from the same two analyses, where we observe up to 31% to 56% reduction in this length. We see that the longest wire is not affected strongly by the inter-layer via capacitance. We can also see that this length tracks the side length of the die fairly well.

Additionally, for purposes of comparison with Figure 2, we obtain the placed wire length distribution for the same circuit, shown in Figure 16.

5. LAYOUT OF 3-D ICS

We have extended the Berkeley layout editor Magic [24] to manage multiple-layer designs. Our tool, called 3-D Magic, automates the methodology introduced in [25] for 3-D IC design. 3-D Magic allows hand-design of 3-D integrated circuits, as well as manipulation of designs generated by our place-and-route tool. The display of inter-layer vias between the two relevant layers of the circuit is automated, and electrical-connectivity information for circuit nodes is maintained across all layers. 3-D Magic can also extract an entire 3-D circuit at once, using a user-configurable lumped-parameter model for the inter-layer interconnect. With this extraction, existing tools can be used to simulate circuit performance and close the design loop.

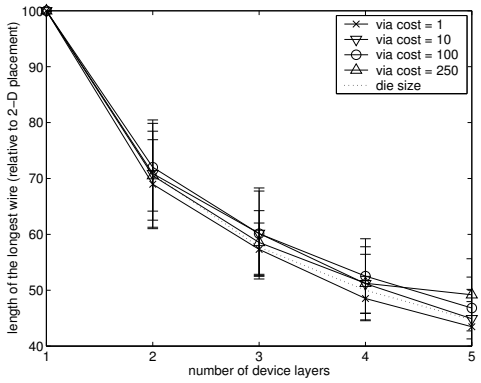

Figure 14: Length of the longest wire (as a function of number of device layers) for various inter-layer via capacitances. Total wire length is minimized by the placement tool. Via cost is the via capacitance expressed relative to the capacitance of one micron of metal wire.

In Figures 18 and 17, we show 3-D Magic layout of a sample circuit that has been placed and routed in two device layers using our tools.

6. CONCLUSION

Three-dimensional integration is a new class of fabrication and packaging technology that promises to offer increased performance and scalability to designers of future digital and mixed-signal integrated circuits. We have presented our candidate 3-D integration technology and illustrated some of the key capabilities and challenges of our method.

In addition, we have illustrated some issues particular to the design of digital and mixed-signal 3-D ICs, as well our suite of design tools for these circuits. Using these design tools, we have performed analyses of 3-D IC performance. For example, in digital circuits, we see up to 28% to 51% total wire-length reduction and 31% to 56% reduction in length of the longest wire using two to five device layers. We also observe that 3-D technology parame-

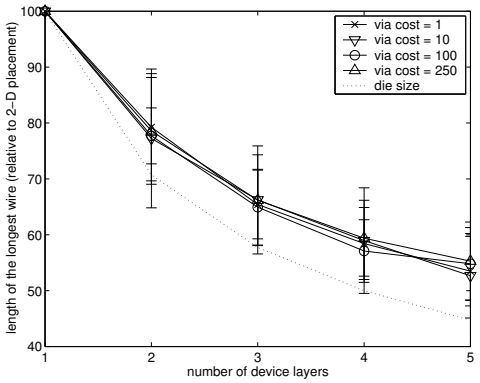

Figure 15: Length of the longest wire (as a function of number of device layers) for various inter-layer via capacitances. The number of inter-layer vias is minimized by the placement tool. Via cost is the via capacitance expressed relative to the capacitance of one micron of metal wire.

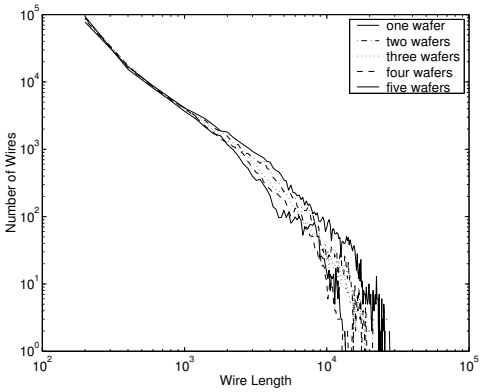

Figure 16: Placed wire length distribution for a sample circuit as a function of the number of device layers used.

ters such as inter-layer via capacitance have significant impact on these savings. It is clear, therefore, that further research both in 3-D fabrication technology development and in 3-D IC CAD will be of benefit to the design community.

7. ACKNOWLEDGMENTS

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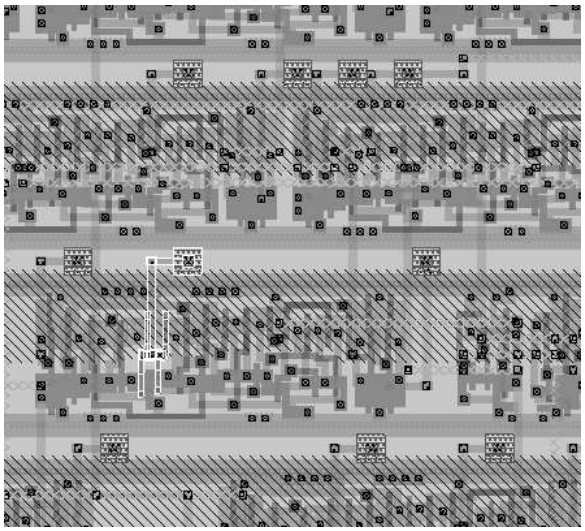

Figure 17: Top wafer of a two-wafer layout of a standard-cell circuit, as viewed in 3-D Magic. Highlighted wire spans both wafers.

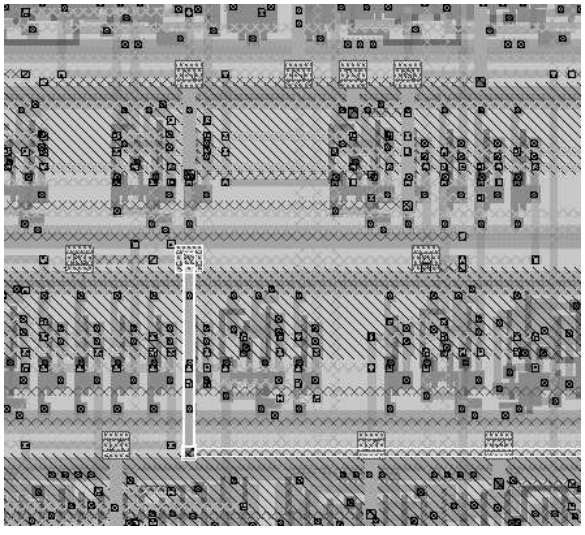

Figure 18: Bottom wafer of a two-wafer layout of a standard-cell circuit, as viewed in 3-D Magic. Highlighted wire spans both wafers.

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