Multilevel Routing with Antenna Avoidance

Tsung-Yi Ho[1], Yao-Wen Chang[2*], and Sao-Jie Chen[2†]
[1]Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan
[2]Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan

ABSTRACT

As technology advances into the nanometer territory, the antenna problem has caused significant impact on routing tools. The antenna effect is a phenomenon of plasma-induced gate oxide degradation caused by charge accumulation on conductors. It directly influences manufacturability and yield of VLSI circuits, especially in deep-submicron technology using high density plasma. Furthermore, the continuous increase of the problem size of IC routing is also a great challenge to existing routing algorithms. In this paper, we propose a novel framework for multilevel full-chip routing with antenna avoidance using a built-in jumper insertion approach. Experimental results show that our approach reduced antenna-violated gates by about 98% and also achieved 100% routing completion for all circuits.

Categories and Subject Descriptors

B.7.2 [Integrated Circuits]: Design Aids - Layout, Place and Route; J.6 [Computer Applications]: Computer-Aided Engineering - computer-aided design (CAD)

General Terms

Algorithms, Designs

Keywords

Physical design, routing, multilevel optimization, process antenna effect, nanometer, design for manufacturability (DFM)

1. INTRODUCTION

With the continuous and rapid increase in complexity of VLSI designs and fabrication technologies, manufacturing yield and product reliability are now among the most important design issues, such as quick turn-around time, small die size, high speed, low power, and so on [6]. The fine feature size of modern IC technologies is typically achieved by using plasma-based processes. As the technology enters the deep-submicron era, more stringent process requirements cause some advanced high-density plasma reactors adopted in the production lines to achieve fine-line patterns [11]. However, these plasma-based processes have a tendency to charge conducting components of a fabricated structure. The existing experimental evidence indicates that charging may affect the quality of the thin oxide. This is called the *antenna effect* (also called "plasma-induced gate oxide damage"). During metallization, chips are usually processed "from the bulk up", each time adding an additional layer of interconnect. While the metal interconnect chip is being assembled, the interconnect of a net will consist of a number of disconnected pieces of floating metal. Long floating interconnects act as temporary capacitors to store charges gained from the energy provided during fabrication steps such as chemical mechanical polishing (CMP). A random discharge of the floating node due to subsequent process steps could permanently damage transistors, rendering the IC useless [9, 16, 19]. For example, the exposed polysilicon and metal structures connected to a thin oxide transistor will collect charge from the processing environment (e.g., reactive ion etch) and damage the transistor when the discharging current flows through the thin oxide.

Although the mechanism of the gate oxide damage is not very well understood, the precise experimental relationships between the amount of damage and the antennas have been studied [16, 19]. Since the plasma damage is caused by the electrical charging of devices during plasma processes, the damage increases with an increase in the area of the exposed conductor (antenna) during the plasma process. In order to reduce or prevent damage to the gate oxide from the plasma process, and thus to ensure reliability of a chip, a circuit layout rule that considers the antenna effect (antenna rule) is employed. The conventional antenna rule restricts a maximum antenna size or antenna ratio allowed for circuit layout. Recent studies show that the damage, considering all plasma-based manufacturing operations, increases in proportion to both the area and the perimeter of the antennas [17]. A more accurate model considering the cumulative oxide damage is discussed in [1]. These models provide a good guideline for routers or physical EDA tools to help re-

*Yao-Wen Chang's work was partially supported by the National Science Council of Taiwan ROC under Grant No. NSC 91-2215-E-002-038.

†Prof. Sao-Jie Chen is with IBM T. J. Watson Research Center during his sabbatical leave; his work was partially supported by the National Science Council of Taiwan ROC under Grant No. NSC 91-2215-E-002-042.

ISPD'04, April 18–21, 2004, Phoenix, Arizona, USA.

duce damage from the antenna effect and get higher yield and reliability.

Maly et al. [14] proposed a method for detecting antenna violation. He calculated both the area and the perimeter of antennas using a general-purpose design rule checking (DRC) program. However, the method does not indicate any measures to feed the antenna information back to a layout generation. On the other hand, Wang et al. [18] proposed a channel router which considers the antenna effect. They introduced a layer restriction to a conventional channel router, which limits the maximum length of the wires with antenna problems. Chen and Koren [2] also proposed a network bipartitioning approach for layer restriction. But both of them consider antenna effect minimization only in 3-layer channel routing. Shirota et al [17] proposed a router which combines a traditional router with a modification of wires for reducing the antenna effect damage, using a rip-up and reroute method. But this method fixes the antenna after routing; it is not a built-in approach. The diode insertion method is also proposed to fix the antenna problem [1, 8]. It is the simplest way to deal with antenna problems by forcing a discharge path. But in today's high-density VLSI layouts, there is simply not enough room for "under-the-wire" diode insertion for all wires. Furthermore, it will cause congestion, add capacitance to the net, reduce room for ECO, and generate leakage power. Thus, people often prefer a jumper-based solution to a diode-based solution for more advanced process technology.

Routing complexity is also an important problem for modern routers. To cope with the increasing complexity, researchers have proposed multilevel approaches to handle the problem [3, 4, 7, 13]. The multilevel framework has attracted much attention in the literature recently [5]. It employs a two-stage technique: coarsening followed by uncoarsening. The coarsening stage iteratively groups a set of circuit components (e.g., circuit nodes, cells, modules, routing tiles, etc.) based on a predefined cost metric, until the number of components being considered falls below a certain threshold. Then, the uncoarsening stage iteratively ungroups a set of previously clustered circuit components and refines the solution by using a combinatorial optimization technique (e.g., simulated annealing, local refinement, etc). The multilevel framework has been successfully applied to partitioning, floorplanning, placement and routing in VLSI physical design.

In this paper, we propose a multilevel router for reducing the antenna effect damage by built-in jumper insertion. The three main features of the proposed method are: (1) an optimal bottom-up jumper insertion approach for antenna avoidance; (2) an antenna-aware, routability-based multilevel router for better routing completion and antenna avoidance; (3) an antenna fixer for fixing and/or re-routig nets that violate the antenna rule at the uncoarsening stage. Experimental results show that our approach reduced antenna-violated gates by about 98% and also achieved 100% routing completion for all circuits.

The rest of this paper is organized as follows. Section 2 describes the antenna effect damage. Section 3 presents our multilevel framework for reducing antenna effect damage. Experimental results are shown in Section 4. Finally, we give concluding remarks in Section 5, as well as our goals for future work.

2. ANTENNA EFFECT DAMAGE

The mechanism of antenna damage is not fully understood, but there is experimental evidence indicating when charging occurs and how it may affect the quality of gate oxide [16, 19]. Charging occurs when conductor layers not covered by a shielding layer of oxide are directly exposed to plasma. The amount of such charging is proportional to this plasma-exposed area. If the charged conductor layers are connected only to the gate oxide, Fowler-Nordheim (F-N) tunneling current will discharge through the thin oxide and cause damage to it.

Process antenna rules adhere to the design requirement that the total charge accumulated on metal connected to a polysilicon gate during any stage of metalization cannot exceed a certain threshold, beyond which the excessive charge accumulation may permanently damage the gate. Let *gate-strength*(g, L) be the maximum length of a wire of minimum width on layer L that can be directly connected to the gate g without causing an antenna violation. The larger the values of gate-strength, the easier it is to fix the antenna violation. In 0.18-micron technology and above, gate-strength of 1000 microns and above is not uncommon, and fixing by post-processing suffices. In 0.13-micron and below technology, however, the average and worst-case gate-strength's are substantially reduced (about $20 \sim 100$ microns [12, 15]). This is due in part to the use of cells with small gate areas (for example, extensive use of low-power cells) and a tightening of the antenna ratio. When the worst-case gate-strength is merely a handful of cellrows, antenna fixing becomes very challenging.

On the other hand, if the amount of charging collected by connected conductor layer patterns could be released through a low impedance path, such as a previously formed diffusion layer pattern (e.g., source/drain), it will not introduce the gate oxide damage.

A more accurate analysis of the cause of the charging collected during the deep submicron VLSI manufacturing operations shows that the perimeter length of conductor layer patterns must also be included in the calculation [17]. There are three types of plasma-based manufacturing processes:

- Conductor layer pattern etching processes: The amount of accumulated charge is proportional to the perimeter length of conductor layer patterns. Etching processes divide conductor layer plates into innumerable routing patterns. In the late stage of the processes, the perimeters of the routings are directly exposed to plasma.

- Ashing processes: The amount of accumulated charge is proportional to the area of the conductor layer patterns. Ashing processes remove remaining photo resist layers after etching processes of a conductor layer. In the late stage of the processes, the area of a conductor layer pattern is directly exposed to plasma.

- Contact etching processes: The amount of accumulated charge is proportional to the total area of the contacts. Contact etching processes dig holes between two conductor layers. In the late stage of the processes, the area of all the contacts on the lower conductor layer pattern is directly exposed to plasma.

As a result, considering all the plasma-based processes, the risk of gate-oxide damage is proportional to the area and perimeter length of antenna routings and inversely proportional to the area and perimeter length of the gate oxide.

There are three kinds of solutions to reduce the antenna effect [1]:

- Jumper insertion: Break only signal wires with antenna violation and route to the highest level by jumper insertion. This reduces the charge amount for violated nets during manufacturing.
- Embedded protection diode: Add protection diodes on every input port for every standard cell. Since these diodes are embedded and fixed, they consume unnecessary area when there is no violation at the connecting wire.
- Diode inserting after placement and routing: Fix those wires with antenna violations that have enough room for "under-the-wire" diode insertion. During wafer manufacturing, all the inserted diodes are floating (or ground). One diode can be used to protect all input ports that are connected to the same output ports. But this approach works only if there is enough room for diode insertion.

Jumper insertion is the most popular way to solve the antenna problem. Let us show its usage in the following example. Suppose we have a two-terminal net in which a is the source node and b is the terminal node (see Figure 1(a), (b)). In this case, the approximated gate-strength of b is the sum of the length of segments 4, 5, and 6, which may violate the minimum allowable gate-strength. If we add a jumper at the long segment 5 (see Figure 2(a), (b)), the approximate gate-strength of b is just the sum of the length of segments 8, 9, and 10, which will not violate the minimum allowable gate-strength. Thus, if we add jumpers appropriately, the antenna problem can be easily solved.

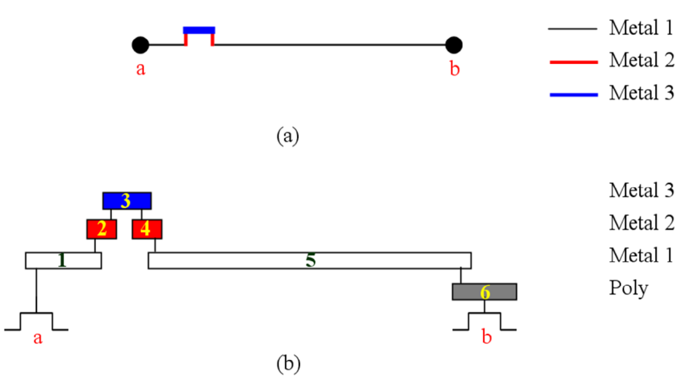

Figure 1: (a) A two-pin net (b) The cross section view

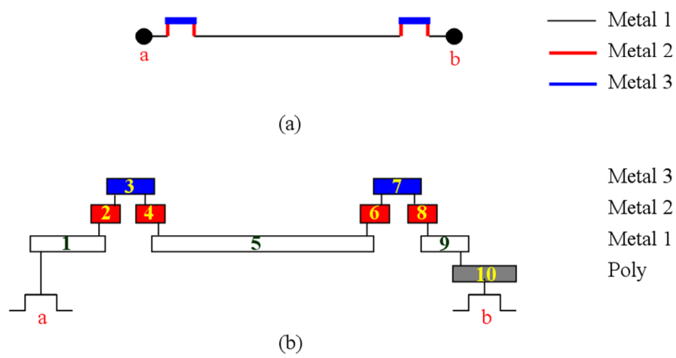

Figure 2: (a) A two-pin net with jumper insertion (b) The cross section view

3. MULTILEVEL ROUTING FRAMEWORK

Our multilevel routing algorithm is inspired by the work of [13]. As illustrated in Figure 3, G_0 corresponds to the routing graph of the level 0 of the multilevel coarsening stage. At each level, our global router first finds routing paths for the *local nets* (or *local 2-pin connections*) (those nets [connections] that entirely sit inside a tile), and then the distance-aware detailed router is used to determine the exact wiring and jumper position. After the global and detailed routing are performed, we merge four adjacent tiles of G_0 into a larger tile and at the same time perform resource estimation for use at the next level (i.e., level 1 here). Coarsening continues until the number of tiles at a level, say the k-th level, is below a given threshold. After finishing coarsening, an antenna check process for every terminal is performed. If nets have antenna violations, we identify them as failed nets that will be routed at the uncoarsening stage. During uncoarsening, the unroutable and antenna-violated nets are considered. Maze routing and rip-up and re-route are performed to refine the routing solution. Then we proceed to the next level (level $k-1$) of uncoarsening by dividing each tile to four finer tiles. The process continues up to level 0 when the final routing solution is obtained.

3.1 Bottom-Up Optimal Jumper Prediction

Given a netlist, we first run the minimum spanning tree (MST) algorithm to construct the topology for each net. Then we decompose each net into 2-pin connections, with each connection corresponding to an edge of the minimum spanning tree. Each net to be connected is composed of a set of terminals, one of which is a driver and the others receivers. At the beginning of the interconnect fabrication process, the receiver-type terminals are in poly and driver-type terminals are in diffusion. Any incomplete interconnect segments connected to one or more receivers forms the antenna. The risk of gate oxide damage is proportional to the amount of charges collected by the antenna and inversely proportional to the area of the gate oxide. In order to reduce the negative impact of antenna effects, the antenna area of each terminal has to be minimized. Thus, it is natural to formulate the antenna area of a terminal as the interconnect length spread from it. To minimize the total antenna area, we can break signal wires with antenna violation and route them to highest levels by jumper insertion. This reduces the charge amount for violated nets during manufacturing. But each jumper needs at least two vias and will cause delay. In the $0.13\mu m$ technology, the short gate-strength results in a dramatic increase in the number of jumpers that need to be added to the wire. Thus, it is very important to minimize antenna area and jumpers at the same time.

In this paper, we proposed a bottom-up approach to predict the jumper positions by inserting a minimum number of jumpers. Given a net and a source, we first hang the net by using the source as root (see Figure 4). Then we

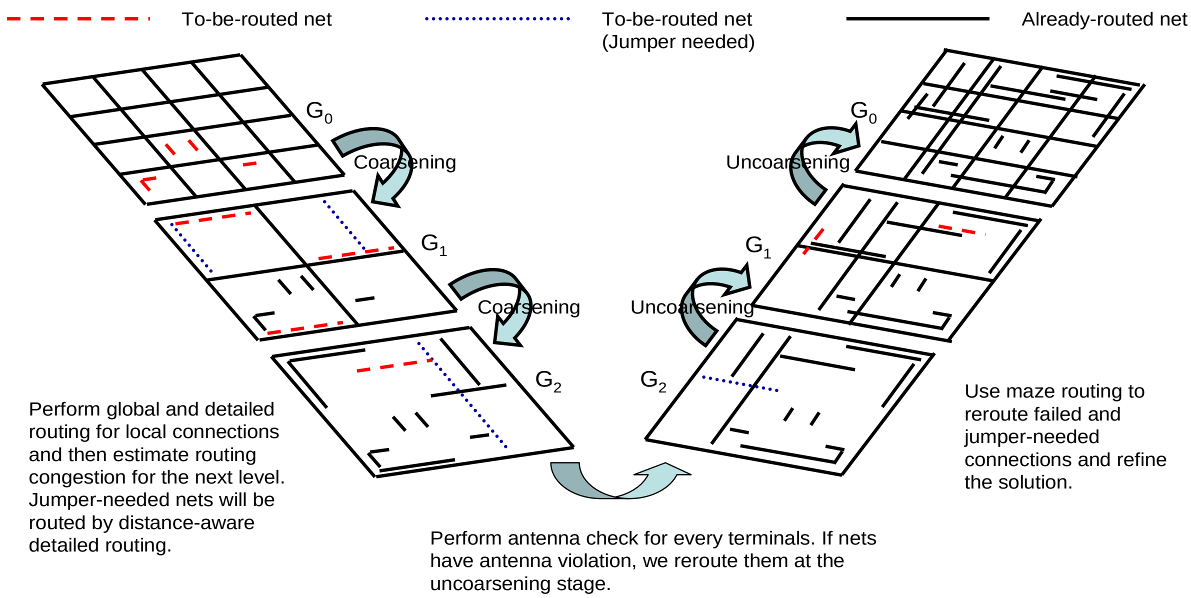

Figure 3: The multilevel framework flow.

compute the position of the jumper by accumulating interconnect length from each terminal in bottom-up fashion. To compute it, we have two possible scenarios as shown in Figure 4. Line 4 considers whether the cumulative length $C(v)$ of descendants of the terminal v (e.g., $\sum_{i=1}^{m} d(e_i)$ in Figure 5(a), where $d(e_i)$ denotes the length between the node v and the root of the i-th subtree and m denotes the number of subtrees) is less than the allowable antenna area ($Amax$). For this case, there are two possible scenarios. First, if the sum of $C(v)$ and the length between v and its precedent w (i.e. u(e)) does not exceed the $Amax$, we accumulate the total length and the number of gates to w for further computation. Second, if the sum of $C(v)$ and the length between v and its precedent w exceeds the $Amax$, we add a jumper at the position near v (see Figure 5(b)). After that, if the remaining length connecting to w also exceeds the $Amax$, we add a jumper at the position near w. Line 10 considers whether the cumulative length of descendants ($C(v)$) of the terminal v is greater than the allowable antenna area ($Amax$). For this case, we first rank the length of edge adjacent to v in increasing order. If the cumulative length exceeds the $Amax$, we add a jumper at the edge near v (see Figure 5(c)). If we add a jumper at the edge (v, w), then goto Line 4. The algorithm is summarized in Figure 4.

Given a net with n nodes, the best case time complexity of our jumper-prediction algorithm is $O(n)$ when the cumulative length of descendants for all nodes is less than the allowable antenna area (Lines 4–9). And the worst case time complexity happens when the net topology is a star graph (all the nodes are connected to the source directly) and the cumulative length of descendants for a source is greater than the allowable antenna area (Lines 10–26). Since the complexity is determined by sorting, the worst case time complexity is $O(n \lg n)$.

By this algorithm, we can predict which edges are in the best position to insert jumpers and then route these edges by distance-aware detailed routing at the coarsening stage.

3.2 Routability-Driven Multilevel Routing

After the jumper position is predicted, our multilevel framework starts by coarsening the finest tiles of level 0. At each level, tiles are processed one by one, and only local nets (connections) are routed. At each level, the two-stage approach of global routing followed by detailed routing is applied. (See Figures 6 for an illustration.) The global routing is based on the approach used in the Pattern Router [10]. It first routes local nets (connections) on the tiles of level 0. Let the multilevel routing graph of level i be $G_i = (V_i, E_i)$. Let $R_e = \{\ e \in E_i \mid e$ is the edge chosen for routing$\}$. We apply the cost function $\alpha : E_i \rightarrow \Re$ to guide the routing:

$$\alpha(R_e) = \sum_{e \in R_e} c_e, \qquad (1)$$

where c_e is the congestion of edge e and is defined by

$$c_e = 1/2^{(p_e - d_e)},$$

where p_e and d_e are the capacity and density associated with e, respectively.

After the global routing is completed, we perform distance-aware detailed routing with the guidance of the global-routing results and find a real path in the chip. Our distance-aware detailed router is based on the maze-searching algorithm. It is easy to insert a jumper when the routing length almost exceed the allowable gate-strength. Pattern routing uses an L-shaped or a Z-shaped route to make the connection, which gives the shortest path length between two points. Because the wire length is minimum, we do not include wire length in the cost function at this stage. We measure the routing congestion based on the commonly used channel density. After the detailed routing finishes routing a net, the channel density associated with an edge of a multilevel graph is updated accordingly.

Our global router first tries L-shaped pattern routing. If the routing fails, we try Z-shaped pattern routing. This can be considered as a simple version of rip-up and re-route. If

Algorithm : JumperPredict(T)
Input : MST T and source s;
Output : Jumper positions of T

begin

Pick unvisited v s.t. all descendants of v have been visited and let w as the precedent of v.
for all node v, set $C(v) = 0$ and $visit(v) = 0$
while $w \neq s$ **do**
  if $(C(v) < Amax)$
    if $(C(v) + leng(v, w) > Amax)$
      JumperAdded(v, Up);
      SecondJumperCheck$(leng(v, w) - (Amax - C(v)))$
    else
      AccumulateSegment();
  else
    InsHeap$(v, w, leng(v, w))$;
    UpJumper=0;
    while HeapSize $\neq 0$
      AccLen=AccLen+PopHeap()→length;
      if (AccLen>Amax)
        if (PopHeap()→node $\neq w$)
          JumperAdded(v, Dn);
        else
          JumperAdded(v, Up);
          UpJumper= 1;
      HeapSize−−;
    if (UpJumper== 1)
      SecondJumperCheck$(leng(v, w) - 1)$;
    else
      AccumulateSegment();
  visit(v)=1;

end

Figure 4: Algorithm for Jumper Prediction.

both pattern routes fail, we give up routing the connection, and an overflow occurs. We refer to a *failed net* (*failed connection*) as one that causes an overflow. The failed nets (connections) will be reconsidered (refined) at the uncoarsening stage. There are at least two advantages to using this approach. First, routing resource estimation is more accurate than that performing global routing alone, since we can precisely evaluate the routing region. Second, we can obtain a good initial solution for the following refinement very effectively since pattern routing enjoys very low time complexity and uses fewer routing resources due to its simple L-shaped and Z-shaped routing patterns.

After the coarsening stage, we perform an antenna check for every terminal. Since the accumulated gate-strength is kept in every terminal, the antenna check process can be performed in short time. An accurate damage function which considers all plasma-based manufacturing operations is adopted for the antenna check. From considerations of all such operations (etching of conductor layer pattern, ashing, etching of via pattern, etc.), it is known that the transistor-gate damage increases in proportion to the antenna area and moreover the antenna perimeter length. The adoption of this damage function makes the calculation of damage accurate. If nets have antenna violation, we regard them as the failed nets to be routed at the uncoarsening stage. The uncoarsening stage starts to refine each local failed net (con-

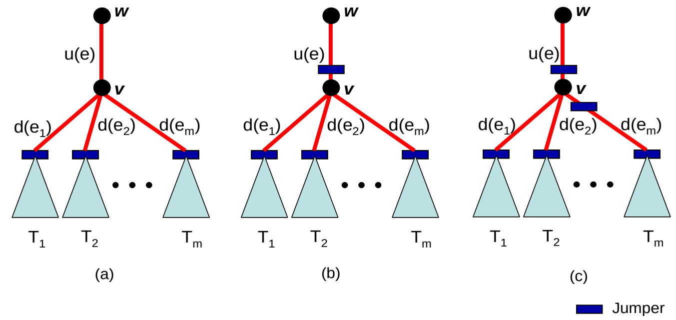

Figure 5: (a) The initial case before the jumper-prediction process (b) The case of $\sum_{i=1}^{n} d(e_i) < Amax$, but $\sum_{i=1}^{m} d(e_i) + u(e) > Amax$, we add a jumper on $u(e)$ then do SecondJumperCheck. (c) The case of $\sum_{i=1}^{m} d(e_i) > Amax$, we accumulate the length of edges adjacent to v in increasing order. If the cumulative length exceeds the $Amax$, we add a jumper at the edge near v.

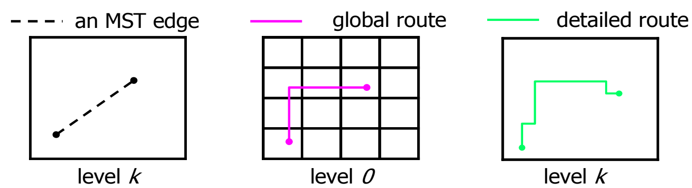

Figure 6: Global routing followed by detailed routing.

nection), left from the coarsening stage. The global router is now changed to the maze router with the following cost function $\beta : E_i \rightarrow \Re$:

$$\beta(R_e) = \sum_{e \in R_e} (al_e + bc_e + co_e), \qquad (2)$$

where a, b, and c are user-defined parameters, l_e is the length of the net (connection), and $o_e \in \{0, 1\}$. If an overflow happens, o_e is set to 1; otherwise it is set to 0.

There is a trade-off among minimizing wire length, congestion, overflow and jumper insertion. At the uncoarsening stage, we intend to resolve the overflow in a tile. Therefore, we let c be much larger than a or b. Also, a detailed maze routing is performed after the global maze routing. Iterative refinement of a failed net is stopped when a route is found or after several tries (say, three) have been made. Uncoarsening continues until the first level G_0 is reached and the final solution is found. This two-stage approach of global and local refinement of detailed routing outlines our overall refinement scheme.

4. EXPERIMENTAL RESULTS

We have implemented our multilevel system with antenna avoidance in the C++ language on a 1 GHz SUN Blade 2000 workstation with 1GB memory. See Table 1 for the benchmark circuits. The design rules for wire/via widths and wire/via separation for detailed routing are the same as those used in [13].

Table 1 describes the set of benchmark circuits. In the table, "Size" gives the layout dimensions, "#Layers" de-

Circuits	Results without antenna avoidance [13]					Our Results					
	Wirelength	#Vias	#Violated Gate	Time	Cmp. Rates	Wirelength	#Vias	#Violated Gate	Time	#Jumpers	Cmp. Rates
S5378	8.2e7	7163	107	35	100%	8.2e7	7217	0	46.9	20	100%
S9234	6.0e7	6287	89	26.2	100%	6.1e7	6326	0	35.3	15	100%
S13207	2.2e8	14938	267	106.7	100%	2.2e8	15143	7	157.2	79	100%
S15850	2.4e8	17334	310	538.8	100%	2.4e8	17653	7	669.4	127	100%
S38417	5.9e8	43551	1145	899.9	100%	5.9e8	44146	32	1469.9	236	100%
S38584	7.7e8	61053	1973	1953.7	100%	7.9e8	62451	88	2721.4	589	100%

Table 2 : Results of wirelength, vias, violated gates, run-time, jumpers and completion rate comparison.

Circuits	Size (μm)	#Layer	#Nets	#Diffusions	#Gates
S5378	4330x2370	3	3124	1694	3040
S9234	4020x2230	3	2774	1486	2699
S13207	6590x3640	3	6995	3781	6781
S15850	7040x3880	3	8321	4472	8094
S38417	11430x6180	3	21035	11309	20901
S38584	12940x6710	3	28177	14753	27836

Table 1 : The benchmark circuits.

notes the number of routing layers used, "#Nets" represents the number of two-pin connections after net decomposition, "#Diffusions" represents the number of diffusions (drivers), "#Gates" represents the number of receiver type terminals.

Experimental results on wirelength, the number of vias, the number of violated gates, run-time, the number of jumpers and completion rate are listed in Tables 2. As mentioned in [12], we set $Amax$ to $100\mu m$ in this experiment. Compared with [13], the experimental results show that our router reduced antenna-violated gates by about 98% and achieved 100% routing completion for all circuits, with very small overheads in wirelength, vias, and run-time. The results show the effectiveness of our multilevel router in coping with the antenna effects.

5. CONCLUSION

In this paper, we have proposed a novel framework for multilevel routing considering antenna avoidance. The experimental results have shown that our algorithm is very effective for antenna-aware routing . Our future work lies in multilevel routing considering other nanometer electrical effects.

6. ACKNOWLEDGEMENT

We would like to thank Mr. H. K.-S. Leung of Magma Design Automation and Professor M. Marek-Sadowska of UCSB for very helpful discussions. We also thank anonymous reviewers for their very constructive comments.

7. REFERENCES

[1] P. H. Chen, S. Malkani, C.-M. Peng, and J. Lin, "Fixing antenna problem by dynamic diode dropping and jumper insertion", *Proc. International Symposium on Quality Electronic Design*, pp 275-282, 2000.

[2] Z. Chen and I. Koren, "Layer Reassignment for Antenna Effect Minimization in 3-Layer Channel Routing", *Proc. Workshop on DFT*, pp 77-85, 1996.

[3] J. Cong, J. Fang, and Y. Zhang, "Multilevel approach to full-chip gridless routing", *Proc. International Conference on CAD*, pp. 396-403, Nov. 2001.

[4] J. Cong, M. Xie, and Y. Zhang, "An enhanced multilevel routing system", *Proc. International Conference on CAD*, pp. 51-58, Nov. 2002.

[5] J. Cong and J. Shinnerl, *Multilevel Optimization in VLSICAD*, Kluwer Academic Publishers, 2003.

[6] H. T. Heineken, J. Khare, W. Maly, P. K. Nag, C. Ouyang, and W. A. Pleskacz, "CAD at the design-manufacturing interface", *Proc. Design Automation Conference*, pp. 321-326, Jun. 1997.

[7] T.-Y. Ho, Y.-W. Chang, S.-J. Chen, and D. T. Lee, "A Fast Crosstalk- and Performance-Driven Multilevel Routing System", *Proc. International Conference on CAD*, pp.382-387, Nov. 2003.

[8] L.-D. Huang, X. Tang, H. Xiang, D. F. Wong, and I.-M. Liu, "A Polynomial Time Optimal Diode Insertion/Routing Algorithm for Fixing Antenna Problem", *Proc. Design, Automation and Test in Europe*, pp. 470-475, 2002.

[9] A. B. Kahng, "Research directions for coevolution of rules and routers", *Proc. International Symposium on Physical Design*, pp. 122-125, Apr. 2003.

[10] R. Kastner, E. Bozorgzadeh, and M. Sarrafzadeh, "Pattern routing: use and theory for increasing predictability and avoiding coupling ", *IEEE Trans. on CAD*, pp. 777-790, Nov. 2002.

[11] S. Krishnan, S. Rangan, S. Hattangady, G. Xing, K. Brennan, M. Rodder, and S. Ashok, "Assessment of charge-induced damage to ultra-thin gate MOSFETs", *Proc. International Electron Devices Meeting*, pp. 445-448, 1997.

[12] H. K.-S. Leung, "Advanced routing in changing technology landscape", *Proc. International Symposium on Physical Design*, pp. 118-121, Apr. 2003.

[13] S.-P. Lin and Y.-W. Chang, "A novel framework for multilevel routing considering routability and performance", *Proc. International Conference on CAD*, pp. 44-50, Nov. 2002.

[14] W. Maly, C. Ouyang, S. Ghosh, and S. Maturi, "Detection of an antenna effect in VLSI designs", *Proc. International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 86-94, Nov. 1996.

[15] R. H. J. M. Otten, R. Camposano, and P. R. Groeneveld, "Design Automation for Deepsubmicron:

present and future", *Proc. Design, Automation and Test in Europe*, pp. 650-657, 2002.

[16] H. Shin, C.-C. King, and C. Hu, "Thin Oxide Damage by plasma etching and ashing process", *Proc. International Reliability Physics Symposium*, pp. 37-41, 1992.

[17] H. Shirota, T. Sadakane, M. Terai, and K. Okazaki, "A new router for reducing "Antenna effect" in ASIC design", *Proc. Custom Integrated Circuit Conference*, pp. 27.5.1 - 27.5.4, Sep. 1998.

[18] K. P. Wang, M. Marek-Sadowska, and W. Maly, "Layout design for yield and reliability", *Proc. Physical Design Workshop*, pp. 190-197, Apr. 1996.

[19] H. Watanabe, J. Komori, K. Higashitani, M. Sekine, and H. Koyama , "A wafer level monitoring method for plasma-charging damage using antenna PMOSFET test structure", *IEEE Trans. on Semiconductor Manufacturing*, pp. 228-232, May. 1997.