A Low-Power Rail-to-Rail 6-bit Flash ADC Based on a Novel Complementary Average-Value Approach

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ABSTRACT

In this paper, a 6-bit 300-MSample/s(MS/s) flash analog-to-digital converter (ADC) with a novel complementary average-value (CAV) approach is proposed. Input signal is pre-processed and then steered to be compared with a fixed reference voltage level, which greatly simplifies the comparator design and thus power consumption is reduced. In addition, rail-to-rail input range can be achieved by the proposed CAV technique, and the offset as well as bubble errors can therefore be minimized as a result of similar operation condition arrangement of the comparators. Simulated with TSMC 1P5M 0.25 μm process parameters, the results show that INL < ±0.4 LSB and DNL < ±0.1 LSB, and SNDR of 32.7dB can be achieved. The converter consumes 35mW at 2.5 V power supply and the power efficiency of this converter is only 3.3pJ/conv-step which compares favorably with other published results.

Categories and Subject Descriptors

B.7.1 **[Integrated circuits]** Types and Design Styles *VLSI (very large scale integration)*

General Terms: Design

Keywords: Flash analog-to-digital converter, rail-to-rail, Low Power, CMOS analog circuit, Comparator

1. INTRODUCTION

High performance analog-to-digital-conversion (ADC) interface circuitry is widely used on mixed-signal circuit design. Current interesting topics of ADC are focused on the improvement of resolution and conversion speed. In certain applications such as communication networks or disk-drive read-channel, resolution of 6-bit is enough while speed and power consumption are the most important concerns. Several kinds of ADC architectures have been proposed in order to tackle these issues, for example, flash architecture [1]-[3] and folding/interpolating architecture [4,5]. Flash ADC takes advantage of parallel comparison for achieving high conversion rate, however with the disadvantages that power dissipation and chip area increase exponentially with the resolution. Folding architecture ADC can also provide comparable high speed as flash ADC but with fewer comparators, thus less power and area can be achieved. However, the conversion performance shrinks rapidly as the input frequency increases.

The scaling of supply voltage along with process technology has been a critical issue for analog circuit design since the available dynamic range decrease as well. Different rail-to-rail flash ADC design technique is then proposed in order to satisfy adequate dynamic range requirements [14]. However, comparator design will be the critical part to achieve rail-to-rail input range and low power consumption in the flash ADC [6, 7]. For high conversion rate, high speed comparison should be performed within a wide range of input signal and different reference voltage taps. Offset voltage associated with comparators under different operating conditions and process variations even complicates the design. Bubble errors may also arise due to mismatch of different comparators [8]. To accommodate wide-range input signal swing, the comparators are either identically designed with complex rail-to-rail technique, or separately designed to fit distinct operating point.

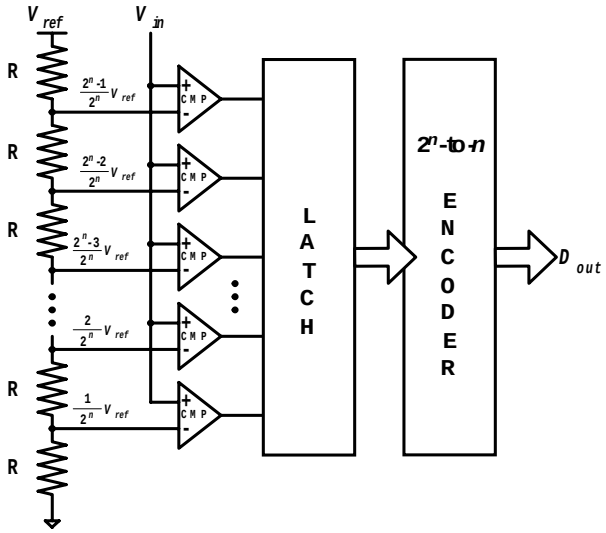


Figure 1. Block diagram of the conventional Flash ADC.

In this paper, we propose a flash ADC architecture based on a novel complementary average-value (CAV) approach, which can force every comparator to compare with only one fixed reference voltage, which greatly simplifies the comparator design.

In Section 2, the proposed complementary average-value approach and the flash ADC architecture will be described and explained in detail. Simulation results are given in Section 3 and finally Section 4 concludes the work.

2. COMPLEMENTARY AVERAGE-VALUE (CAV) APPROACH

2.1 Proposed Flash ADC with CAV Approach

Flash ADC is the simplest and fastest known architecture. A conventional flash ADC architecture is shown in Fig. 1. In a flash A/D converter, the input signal is compared to reference taps (all possible quantization levels) simultaneously. The differences between the input and reference values are amplified to digital levels and generate thermometer code. The thermometer code is then encoded to binary or grey code. The reference voltages are usually provided by tapping from a resistor ladder to guarantee the monotonic increase of reference voltages from zero to input full scale.

Such kind of flash ADC architecture may face several problems in its circuit design. From Fig. 1, each comparator compares *Vin* with a different reference voltage tap, ranging from $(1/2^n)\cdot V_{ref}$ to $(2^{n-1}/2^n)\cdot V_{ref}$, respectively. Such a wide input range poses a stringent restriction on the comparator design. If the input range is not an important concern, for example, when V_{ref} is 1 V and the supply voltage is 2.5 V or even higher, then the operating point of the input of comparator can be well defined without forcing the transistors into triode region. However, when the input range is a primary concern, then comparator design becomes a complex task. Generally there are two possible solutions. The first is to design the comparator in different types in order to meet different operating conditions. For instance, using NMOS input differential pairs when higher reference taps are applied and PMOS ones while lower reference taps are applied. Such approach complicates the comparator design since distinct design conditions must be satisfied and the matching between different comparators should also be taken care of. The second way to tackle this issue is by making use of a rail-to-rail comparator. Nonetheless, a rail-to-rail comparator usually consumes high power than a conventional one used in the flash ADC.

To overcome the problems stated above, a novel flash ADC architecture is proposed based on the concept of 2's *Complement* and *Average-Value* approach, which stands for the name *CAV*. For an n-bit ADC, the Least Significant Bit is defined to be $LSB = (1/2^n)\cdot V_{ref}$. An input signal V_{in} is quantized into n-bit binary code $A = (a_{n-1}, a_{n-2}, \cdots, a_0)$ for the range where $(A/2^n)\cdot V_{ref} \le V_{in} \le ((A+1)/2^n)\cdot V_{ref}$. Define the complementary value of A as $COM(A) = V_{ref} - (A/2^n)\cdot V_{ref}$, we can obtain that $COM(A) = ((\overline{A}+1)/2^n)\cdot V_{ref}$. The derivation is shown as follows:

$$
\begin{aligned}
COM(k) &= V_{ref} - \frac{A}{2^n}V_{ref} \\
&= \frac{(2^{n-1}+\cdots+2^1+2^0+2^0)-(a_{n-1}2^{n-1}+\cdots+a_1 2^1+a_0 2^0)}{2^n}V_{ref} \\
&= \frac{(1-a_{n-1})2^{n-1}+\cdots+(1-a_1)2^1+(1-a_0)2^0+2^0}{2^n}V_{ref} \\
&= \frac{(\overline{a_{n-1}}2^{n-1}+\cdots+\overline{a_1}2^1+\overline{a_0}2^0)+2^0}{2^n}V_{ref} \\
&= \frac{\overline{A}+1}{2^n}V_{ref} \qquad (1)
\end{aligned}
$$

From (1) we can obtain the following equation,

$$\frac{A}{2^n}V_{ref} + \frac{\overline{A}+1}{2^n}V_{ref} = V_{ref} \qquad (2)$$

Dividing both sides by 2, we can have

$$\frac{1}{2}\cdot\left(\frac{A}{2^n}V_{ref} + \frac{\overline{A}+1}{2^n}V_{ref}\right) = \frac{1}{2}V_{ref} \qquad (3)$$

From (3), we can observe that the mean value of a digital code and its 2's complement is equal to half of *Vref*. Thus, for any input signal, if $V_{in} \ge (A/2^n)\cdot V_{ref}$, the following equation must be satisfied.

$$\frac{1}{2}\left(V_{in} + \frac{\overline{A}+1}{2^n}V_{ref}\right) \ge \frac{1}{2}V_{ref} \qquad (4)$$

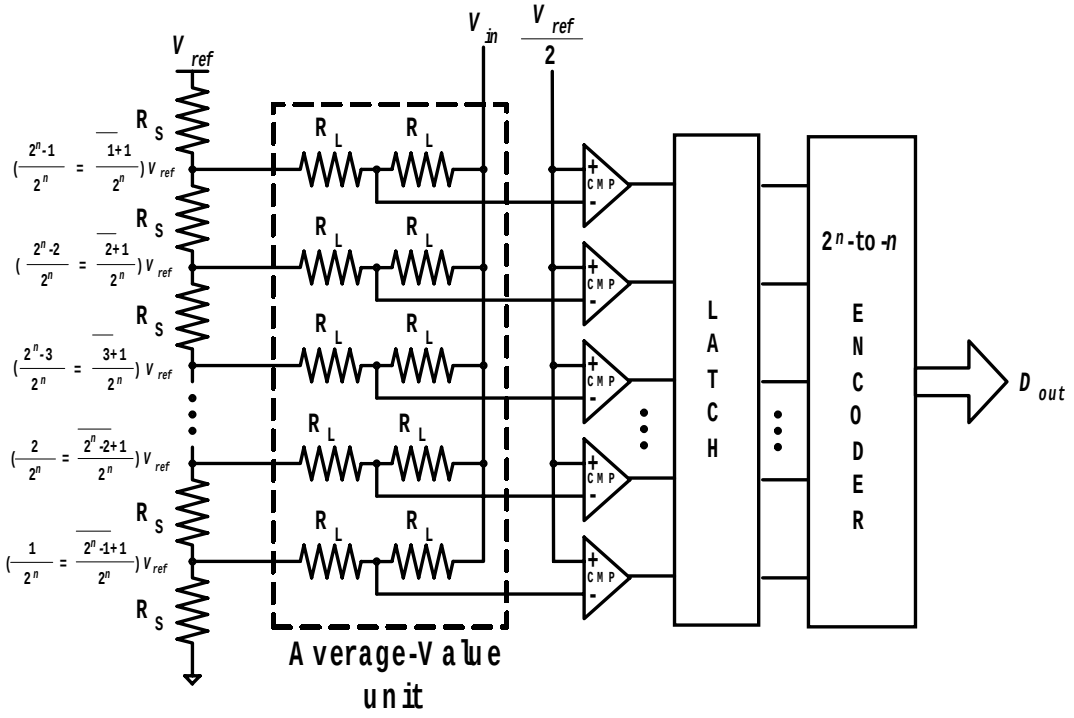


Figure 2. Block diagram of the proposed CAV-based flash ADC

As (4) indicates, we can check the corresponding binary code output of V_{in} by modifying the value of A. For example, for a 6-bit flash ADC, if $(1/64)\cdot V_{ref} \le V_{in} \le (2/64)\cdot V_{ref}$, then only $[V_{in} + (i \cdot V_{ref})/64]/2, i = 63$ can be larger than $V_{ref}/2$. Other *i's* from 1 to 62 make $[V_{in} + (i \cdot V_{ref})/64]/2$ smaller than $V_{ref}/2$. More detailed and intuitive explanation as well as circuit implementation is presented in the following section.

2.2 Circuit Design

With the proposed CAV approach, a 6-bit flash ADC architecture is rearranged as shown in Fig. 2. The CAV-based 6-bit flash ADC is divided into four parts: complementary reference voltage generation block, average-value unit, comparator string, and the encoder. As observed in Fig. 2, 63 complementary levels from $(1/64)V_{ref}$ to $(63/64)V_{ref}$ can be generated by using the conventional resistor string. Each voltage level can be transformed to a corresponding complementary-type representation as shown beside the reference tap. The averaging function is performed simply by the average-value unit constituted with a parallel combination of resistors. The mean value can be obtained from the middle node of each $R_L - R_L$ connection, which is then used to compare with $V_{ref}/2$ as described in (4). The comparison results are still in thermometer-code type, and the encoder will convert this thermometer code to Grey-code and finally to binary output.

In this design, theoretically the value of (R_L/R_S) should be as large as possible to make all the tap voltage of the resistor ladder more accurate. However, significant parasitic capacitance accompanied by the employment of large-value resistors may cause serious degradation in speed. As a trade-off, R_L with value over 1000 times greater than R_S is acceptable.

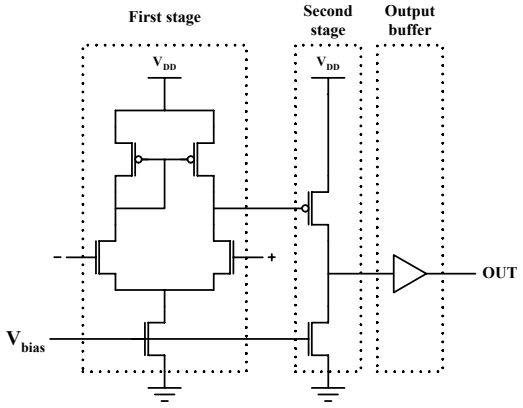


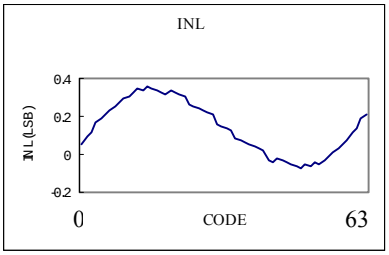
Figure 3. The circuit diagram of a low-cost, low-power comparator

The comparator used in the proposed CAV-based flash ADC is shown in Fig. 3. A simple two-stage structure is adopted since one input terminal is always fixed at $V_{ref}/2$ which is in the linear

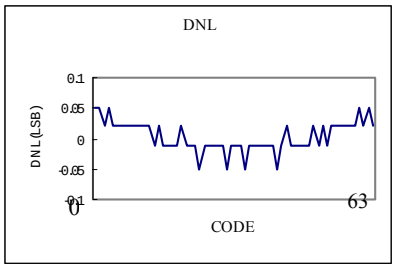
operation region of a comparator. By applying CAV approach, complicated rail-to-rail comparator or distinct comparator design that is necessary for wide input common-mode range can be avoided. The cost and power consumption can also be greatly reduced due to the simplification of the comparator design.

3. SIMULATION RESULTS

For the verification of the proposed CAV approach, different simulations using spice with TSMC 0.25 μm 1P5M process parameter are performed. From the simulation results, the conversion rate of 300 MHz at 2.5 V supply voltage can be achieved with the power consumption lower than 35 mW. The INL and DNL simulation results are shown in Fig. 4 (a) and (b). The INL and DNL are smaller than ± 0.4 LSB and ± 0.1 LSB, respectively. The signal to noise-and-distortion ratio (SNDR) is depicted in Fig. 5. The SNDR at input frequency 133.6 MHz is around 32.7dB. Fig. 6 shows the layout view of the flash ADC.



(a)



(b)

Figure 4. Simulation results of (a) INL and (b) DNL

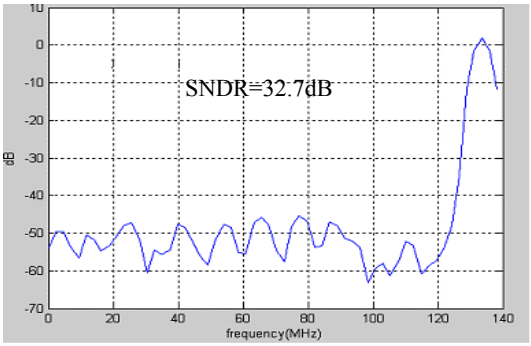


Figure 5. SNDR@ *fin*=133.6MHz and *fs*=300 MHz

Table I shows the specification of the proposed flash ADC under TSMC 0.25 μm 1P5M process. Maximum sampling frequency 300 MHz can be achieved with rail-to-rail input range. The power consumption is about 35 mW with 1.18 mm^2 core area occupied (including the resistor).

Table □ shows the power efficiency comparison between this work (simulation result) and other papers (measurement result). To make a fair comparison among different converter architectures, we normalize the power with signal bandwidth and the effective number of bits (ENOB) by the following expression [9]:

$$Energy/(conversion\_step) = \frac{Power}{2^{ENOB} \times f_{sample}} \qquad (5)$$

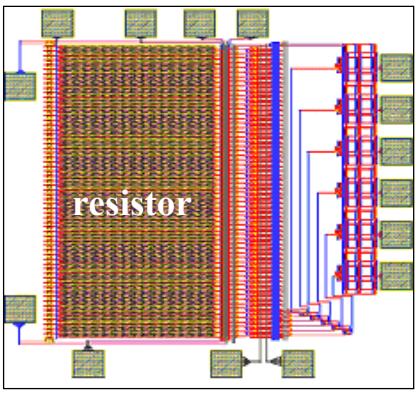


Figure 6. The layout view of proposed 6-bit flash ADC

Table Ⅰ Simulation results of the proposed 6-bit flash ADC

Resolution	6 bits
Technology	0.25 μm CMOS 1P5M
Supply Voltages (V_{dd})	2.5 V
Reference Voltages (V_{ref})	2.5 V
Input Range	0 V - V_{ref} (rail to rail)
Sampling Rate	300 MS/s
INL	± 0.4 LSB
DNL	± 0.1 LSB
SNDR	32.7 dB@ f_{in} = 133.6MHz, f_s = 300MHz
ENOB	5.14 bits@ f_s = 300MHz
Power Consumption	35 mW @ 2.5 V, f_s = 300MHz
Core Size (without pads)	1.07 mm × 1.1 mm

Table Ⅱ POWER EFFICIENCY COMPARISON

Papers	Architecture	f_{sample} (MHz)	ENOB	Power (mW)	Energy/ conv_step (pJ)
[10]	Flash	1000	5.5	500	11
[11]	Flash	400	5.5	150	8.3
[12]	Flash	1100	5.65	300	5.4
[13]	Flash	1300	5	600	14.4
[14]	rail-to-rail Flash	1000	<6	<300	>4.6
This work	rail-to-rail Flash	300	5.14	35	3.3

***** [10-13] are measurement results; [14] and this work are simulation results

4. CONCLUSION

In this paper, we proposed a novel complementary average-value (CAV) approach to design a 6-bit 300-MSample/s(MS/s) flash analog-to-digital converter (ADC) with rail-to-rail input range. Due to the pre-processing feature of the proposed CAV approach, the comparator design can be greatly simplified and thus the power consumption is reduced. Simulated with TSMC 1P5M 0.25 μm process parameters, the results show that INL < ±0.4 LSB and DNL < ±0.1 LSB, with SNDR 32.7dB is achieved. The converter consumes 35mW at 2.5 V power supply voltage. The power efficiency of this converter is only 3.3pJ per conversion step which compares favorably with other published results. From the simulation results, the proposed CAV approach proves to be low-power which also has the potential for low-voltage operation.

5. ACKNOWLEDGEMENT

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6. REFERENCE

[1] I. Mehr and D. Dalton, "A 500-Msample/s, 6-bit Nyquist-rate ADC for disk-drive read-channel applications," *IEEE J. Solid-State Circuits*, vol. 34, pp. 912-920, July 1999.

[2] A. Baschirotto, G. Brasca, V. Colonna, P. Cusinato, and G. Gandolfi, "A compact-disc analog-to-digital front-end in BiCMOS technology," *IEEE Trans. Consumer Electron*., vol. 46, pp. 343-352, May 2000.

[3] S. Tsukamoto, W. G. Schofield, and T. Endo, "A CMOS 6-b, 400Msample/s ADC with error correction," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1939-1947, Dec. 1998.

[4] M. Flynn and B. Sheahan, "A 400-Msample/s, 6-b CMOS folding and interpolating ADC," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1932-1938, Dec. 1998.

[5] B. S. Song, P. L. Rakers, and S. F. Gillig, "A 1-V 6-b 50-Msample/s current-interpolating CMOS ADC,"*IEEE J. Solid-State Circuits*, vol.35, pp. 647-651, Apr. 2000.

[6] B. Razavi and B. A. Wooley, "Design techniques for high-speed, high resolution comparators," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1916-1926, Dec. 1992.

[7] G. M. Yin, F. O. Eynde, abd W. Sansen, "A high-speed CMOS comparator with 8-b resolution," *IEEE J. Solid-State Circuits*, vol. 27, pp. 208-211, Feb. 1992.

[8] D. A. Johns and K. Martin, Analog Integrated Circuit Design, New York: Wiley, 1997.

[9] R. H. Walden, ''Analog-to-digital converter survey and analysis,'' *IEEE J. Select, Areas Commun*., vol. 17, pp. 96-101, Apr. 1999.

[10] M. Choi and A. A. Abidi, ''A 6 b 1.3GSample/s A/D converter in 0.35-μm CMOS,'' in *ISSCC Dig. Tech. Papers*, vol. 438, 2001, pp. 126-127.

[11] C. Dornovan, and Michael P. Flynn, "A digital 6-bit ADC in 0.25-μm CMOS," *IEEE J. Solid-State Circuits*, vol.37, pp. 432-437, Mar. 2002.

[12] G. Geelen, "A 6 b 1.1 GSample/s CMOS A/D converter," in *ISSCC Dig. Tech. Papers*, 2001, pp. 128-129.

[13] K. Uyttenhove, and Michiel S. J. Steyaert, "A 1.8-V 6-Bit 1.3-GHz Flash ADC in 0.25-μm CMOS," *IEEE J. Solid-State Circuits*, vol.38, pp. 1115-1122, July 2003.

[14] L. Yao, M. Steyaert, and W. Sansen, "A 1.8-V 6-bit flash ADC with rail-to-rail input range in 0.18um CMOS," in *Proc. 5th Int. Conf. ASIC*, 21-24 Oct. 2003, pp. 677-680.