Balanced Energy Optimization

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Abstract
Energy efficiency is now the number one issue for many applications, determining weight and cost, and constraining system performance. Many techniques have been developed to minimize the dynamic and static power consumed by digital designs without any impact on functionality. To achieve further savings it is necessary to employ methods that do constrain functionality in some way. The designer must then balance increased energy efficiency with the functional implications of those techniques. In communications systems non-zero error rates are accommodated and corrected in order to reduce power. In digital designs it is also possible to accept and correct errors generated when worst case timing paths exceed the clock interval. This allows the design to be operated beyond the worst case point at a reduced voltage to save energy. The increased energy efficiency must then be balanced against a decrease in determinism and the addition of error detection and correction structures. Processing scalability can also be employed to increase energy efficiency for workloads which vary dynamically. In single processor system this can be achieved using voltage and frequency scaling, and in multi-processor systems this can be supplemented with adaptive shutdown of unused processors. Scalability does imply a loss of system responsiveness when workloads transition from low to high levels, and this must be balanced against the increased energy efficiency achieved. Power efficiency can also be increased by optimising a processor for the application it is intended to run. By analyzing the algorithms to be executed it is possible to create a processor tailored to its workload. This loss of generality and flexibility must be balanced against the increased energy efficiency of a customized implementation. This talk describes work which ARM and its partners are doing to balance energy efficiency with functionality to create optimized designs.