Hierarchical Extreme-Voltage Stress Test of Analog CMOS ICs for Gate-Oxide Reliability Enhancement*

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ABSTRACT

Yield and reliability are two factors affecting the profitability of semiconductor manufacturing. High-temperature burn-in and extreme-voltage stress tests are two current industrial standard methods to speed up the deterioration of electronic devices and weed-out infant mortality. Extreme-voltage stress test aims at enhancing both quality and reliability without performance the high-cost burn-in test process. Our recent stress tests of analog/mixed–signal CMOS ICs for gate-oxide reliability enhance. This paper presents a control flow model for analog CMOS circuits and uses it to develop a circuit partition scheme. A practically large analog circuit can be partitioned into many smaller sub-circuits so that the developed stress vector generator and stressability analyzer can conformably handle in term of computational complexity. In addition, a structure-based stress vector generation process is also developed. Stress vectors are generated based on the circuit topological structure without performing circuit simulations. The performance improvement proposed in this study can significantly reduce the computational complexity so that the developed stress test system can handle practically large analog CMOS circuits.

Categories and Subject Descriptors

B.7.3 [**Reliability and Testing**]: *Built-in tests, Test generation and Testability.*

General Terms

Reliability.

Keywords

IC Reliability.

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1. INTRODUCTION

Yield and reliability are two factors affecting the profitability of semiconductor manufacturing[1]. In the manufacturing process of modern VLSI semiconductor devices, plasma is often used to deposit or remove material on wafers[2,3]. The plasma may cause destructive charges to be built on the wafers. If the charge buildup is large enough, and the charge has no other leakage path to substrate, a current flows through the connected transistor gate oxide, causing degradation of the gate oxide. The damaged gate oxide may result in performance degradation of the affected transistor and cause reliability failures. Thus, oxide defects have been found as one the major causes for the reliability problems for CMOS ICs[4-7].

Stressing testing is a technique used to weed-out infant mortality by applying higher than usual levels of stress to speed up the deterioration of electronic devices. The concept of this screening process id to accelerate the lifetime of devices such that they begin operation with a failure rate beyond the infant mortality region. The industry standard methods for screening have been high-temperature burn-in [8-10] and high-voltage screening [11-14]. Burn-in is effective in varying degrees for almost all circuits and assembly causes of premature failure. Burn-in screening decreases failure rate of a product during the early life, where overall cost and turn around time are of concerns. The added manufacturing cost may range from 5% to 40% of the total product cost, depending on the burn-in time, qualities of ICs, and product complexity.

High-voltage screening, or referred to as extreme-voltage screening, aims at improving the quality level of CMOS ICs without performing the high-cost burn-in process. Extreme-voltage screening has been implemented to enhance gate-oxide reliability of digital CMOS ICs. Recently, the screening techniques have been successfully developed and applied for endangering reliability of analog circuits [13,14].

Computational complexity is always a major concern for large analog circuits, but can be handled using hierarchical approach. In this study, a circuit-partitioning scheme based on a control flow model of CMOS circuits is used to develop the hierarchical approach. Analog only systems and analog portion of mixed-signal systems are not generally characterized by having a large number of circuit elements. However, the optimization of the analog design using the basic circuit elements (amplifiers, filter networks, comparators, etc.) is much more specialized and requires a great deal experience and knowledge. Therefore, most designers use whether possible predesigned commercially

available circuit elements for the system design. For such cases, each circuit element can be applied in a hierarchical fashion.

Based on the stress test generation and stressability analysis processes developed in [14], Section 2 presents the structure-based stress vector generation process, while the hierarchical approach is discussed in Section 3. Finally, a concluding remark is given in Section4.

2. Structure-based Stress Vector Generation

This study employs a simple control-flow model for the development of the structure-based stress vector generation process. The model is used to partition analog CMOS circuits. In order to demonstrate the effectiveness of the structure-based generation process, the following operational transconductance amplifier (OTA) circuit, as shown in Figure 1, is used as an example. Based on the circuit simulation-based generation process, the stress vectors, stress time, stressability analysis results, and coverage charts of that circuit can be found in [14].

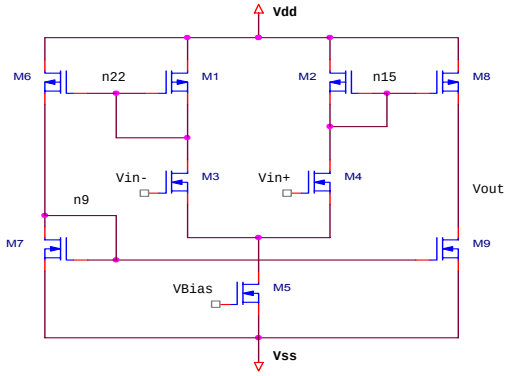


Figure 1. The OTA Circuit.

2.1 Control-Flow Model

For a CMOS network, the drain circuit and gate voltage are two major parameters in its DC analysis. A MOS network can be described by a flow graph and a control graph, where former represents the current flow of the circuit, while the latter describes the gate control voltage. More specifically, the flow graph is constructed by converting each three-terminal MOS transistor in a MOS circuit network into a two-terminal device, where the gate connection of each transistor is removed, as shown in Figure 2(a) fro the OTA circuit.

A *valid path* is defined as a path that travels form V_{dd} to V_{ss}. Both V_{dd} and V_{ss} are referred to as terminal nodes and the others are *primary modes*. A simple path-partitioning scheme is developed to partition a flow graph using the following simple rules:

Rule1: Any valid paths, which share at least, a primary node will be in the same partition.

Rule2: A valid path forms a partition if it does not share a primary node with others.

The circuit in Figure 2(a) contains four valid paths, and, by both rules, it can be divided into three partitions, namely P1, P2, and P3.

A primary node of a partition is called a *controlling node* if it connects to at least one gate of a transistor in the other partition, e.g. node n9 in P1, nodes n15 and n22 in P2. The flow "A→B: in the flow graph, as shown in Figure 2(b), means a controlling node in Partition A connects to the gate of the transistor in Partition B. A *primary partition* is the one, which is not controlled by any other partitions, e.g., P2. Note that bias generator circuits are often used in analog circuit. The circuits take no primary inputs, but their outputs are predictable and referred to as *primary-like inputs*. A partition including the primary and/or primary-like input is also referred to as a primary partition. A sequence level is assigned to each partition. The primary partitions are labeled as Level 0. A partition is labeled as in "Level k" if the highest level of its inputs is Level (k-1). For example, as shown in Figure 2(b), the primary partition P2 is in Level 0. The partition P3 has two inputs n9 and n15, which come form P2 (in Level 0) and P1(in Level 1). Thus, P3 is in Level 2. Figure 2(c) shows the circuit partitions resulted from the original circuit in Figure 1.

2.2 Stress Vector Generation Process

For simplicity of discussion, we first consider a simple circuit with a single valid path, as shown in Figure 2(a), consisting of r cascaded transistors TR_i 's, i=1,2,…,r, and each transistor, NMOS

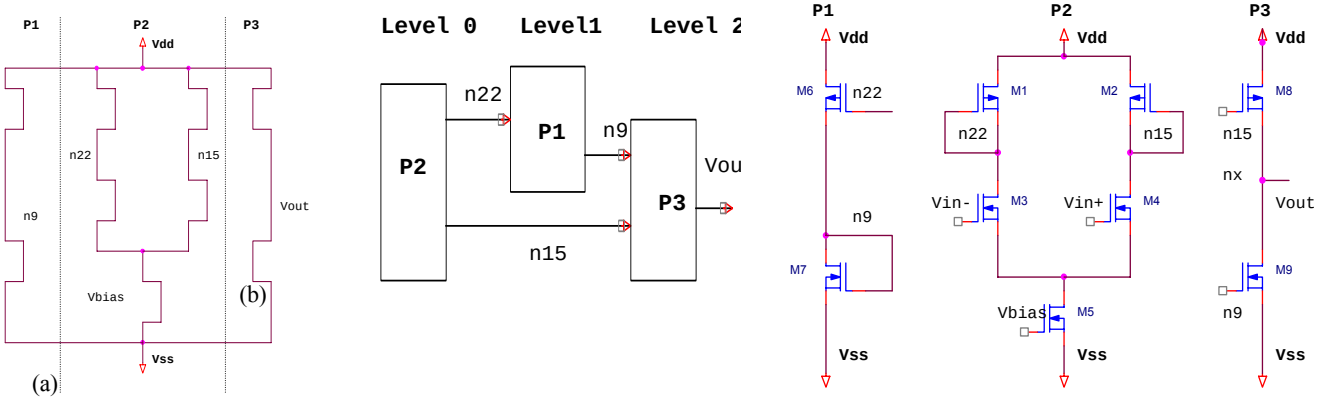


Figure 2: OTA Circuit: (a) Flow Graph; (b) Control Graph; and (c) Circuit Partitions.

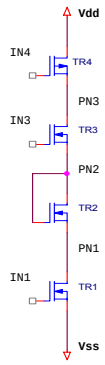
or PMOS, has an input IN_j, j=1,2,…,r. A primary node PNj is located between two transistors TR_j and TR_{j+1}. Without loss of generality, the primary nodes are lined up and labeled in an ascending order, where let $PN_0 = V_{ss}$ and $PN_r = V_{dd}$. Thus, the transistor TR_j is located between nodes PN_{j-1} and PN_j. This circuit can be viewed as a number of NMOS or PMOS switches connected in series. The following property concludes.

Property 1.

(a). The voltage at node PN_j is V_{ss} if the transistors TR_i, i=1,2,…,j, are all ON and at least one TR_i, i=j+1,…,r, is OFF.

(b). The voltage at node PN_j is V_{dd} if the transistors TR_i, i=j+1,…r, are all ON and at least one TR_i, i=1,2,…,j is OFF.

Note that an NMOS transistor is turned ON and OFF by applying V_{dd} and V_{ss} to the gate terminal, respectively. Similarly, a PMOS transistor is turned ON and OFF by applying V_{ss} and V_{dd} to the gate terminal, respectively. Diode-connected transistors are very often used as a resistor in analog circuits, where a diode-connected transistor connects its gate to its drain or source terminal. Property 1 also holds when the partition contains some diode-connected transistors.



(a)

Primary Vectors		
IN1	IN3	In4
1	1	1
0	1	0
1	1	0

(b)

	Candidate Vectors		
Regions	IN1	IN3	IN4
GS(TR1)	1	x	x
GB(TR1)	1	x	x
GD(TR1)	1 1	0 x	x 1
GS(TR2)	1	1	0
GB(TR2)	0	1	0
GD(TR2)	x	x	x
GS(TR3)	1	1	1
GB(TR3)	x	1	x
GD(TR3)	1	1	1
GS(TR4)	x	x	0
GB(TR4)	x	x	0
GD(TR4)	x 0	0 x	0 0

(c)

Figure 3: Stress Vector Generation: (a) Example Circuit;

(b)Stress Conditions & Derived Vectors, (c)Valid Vectors; and (d) Primary Vectors.

Consider the case that a circuit contains a single valid path with a diode-connected transistor, say, TR_{r-2}, which takes no other input to its gate terminal. To properly stress the GS region of TR_{r-2}, its gate voltage at node PNr-2 must be V_{dd} and its source voltage at node PNr-3 is V_{ss}. By property 1(a), the voltage at node PN_{r-3} is V_{ss} if all TR_i, i=1,2,…,r-3, are ON, and either TR_{r-1} or TR_r is OFF. By property 1(b), the voltage at node PNr-2 is V_{dd} if both TR_{r-1} and TR_r are ON, and at least one TR_i, i=1,2,…,r-3, is OFF. As a result, both conditions are conflicting to each other. It is virtually impossible to make $PN_{r-2} = V_{dd}$ and $PN_{r-3} = V_{ss}$ due to the diode-connected structure. However, when all transistors TR_i's, i=1,2,…,r-2,r-1,r, are ON, the maximum current of that circuit occurs. This results that the diode-connected transistor has the maximum voltage across its gate and source terminals. The following property results.

Property 2

Consider a circuit containing a single valid path with diode-connected transistors, the regions GS (or SG) and GD (or DG) of a diode-connected transistor are fully stressed if all non-diode-connected transistors in the valid path are turned ON.

	Stress Conditions						Derived Vectors		
Regions	IN1	IN3	IN4	PN1	PN2	PN3	IN1	IN3	IN4
GS(TR1)	1						1		
GB(TR1)	1						1		
GD(TR1)	1			0			1 1 1	0 1 0	0 1 1
GS(TR2)							1	1	0
GB(TR2)					1		0	1	0
GD(TR2)									
GS(TR3)		1			0		1 1 1	0 1 0	0 1 1
GB(TR3)		1							
GD(TR3)		1				0	1	0	0
GS(TR4)			0						
GB(TR4)			0						
GD(TR4)			0			1	1 0 1	0	0

Both Properties 1 and 2 are used to generate the primary stress vectors for the circuits with a single valid path.

Consider a circuit with a single path shown in Figure 3(a), where the circuit contains 4 transistors, 3 primary nodes, and 3 inputs. TR_2 is a diode-connected NMOS transistor. By property 1(a), the voltage at node PN_1 is V_{ss} if TR_1 is ON, i.e., $V_{IN1}=V_{dd}$, and either TR_3 or TR_4 is OFF, i.e., $V_{IN3}=V_{ss}$ or $V_{IN4}=V_{dd}$. Similarly, the voltage at node PN_3 is V_{dd}, by Property 1(b), if TR_4 is ON, i.e., $V_{IN4}=V_{ss}$, and either TR_1 or TR_3 is OFF, i.e., $V_{IN1}=V_{ss}$ or $V_{IN3}=V_{ss}$.

The first step of the stress vector generation process is to tabulate the required conditions for fully stressing the regions of all transistors in that circuit. The first column in Figure 3(b) lists all regions of the transistors in Figure 3(a). The next step is to define the stress conditions for each region. The stress conditions contain two parts, one for the inputs and the other for the primary nodes. More specifically, to fully stress an NMOS transistor, the node voltages are (V_D, V_G, V_S)=(0,1,0). Similarly, (V_D, V_G, V_S)=(1,0,1) for a PMOS transistor. Note that the "V_y=1(0)" means that V_y reaches the maximum (minimum) DC voltage of the node y="D","G","S"[14]. For example, to fully stress the region GD of the NMOS transistor TR_1, the required conditions are $V_G=V_{IN1}$=1 and $V_D=V_{PN1}$=0. Similarly, for the regions GS of TR_3, the conditions are $V_G=V_{IN3}$=1 and $V_S=V_{PN2}$=0. Note that no stress conditions are considered for both GS (or SG) and GD (or DG) regions of the diode-connected transistors, such as TR_2.

Once all stress conditions are defined, the next step is to derive the required stress vector(s) from those for the primary nodes using Properties 1 and 2. Note that the derived condition must agree with those generated from the inputs. In other words, a derived condition is invalid if it conflicts to a condition generated from the inputs. For example, for the region GD of TR1, the stress condition is $V_G=V_{IN1}$=1 and $V_D=V_{PN1}$=0. By Property 1(a), we can obtain "$V_D=V_{PN1}$=0" by setting TR_1 to be ON, and TR_3 or TR_4 to be OFF, i.e., V_{IN1}=1 and (V_{IN3}, V_{IN4})=(0,0),(0,1),or (1,1), or (V_{IN3}, V_{IN4})=(0,x) or (x,1), where x means "don't care" and can be either 0 or 1. Similarly, the stress condition for the region GS of TR_3 is $V_G=V_{IN3}$=1 and $V_S=V_{PN2}$=0.The condition $V_S=V_{PN2}$=0 results that V_{IN1}=1, and (V_{IN3}, V_{IN4})=(0,0),(0,1), or (1,1). However, the derived vectors $(V_{IN1}, V_{IN3}, V_{IN4})$=(1,0,0) and (1,0,1) have V_{IN3}=0 that conflicts the generated condition V_{IN3}=1. Thus, only the stress vector $(V_{IN1}, V_{IN3}, V_{IN4})$=(1,1,1) is valid. Finally, for the region GS(TR_2), by Property 2, the valid stress vector is $(V_{IN1}, V_{IN3}, V_{IN4})$=(1,1,0).

The table in Figure 3(c) lists the valid stress vectors for all regions of the transistors in Figure 1. The stress vectors are referred to as the *candidate stress vectors*.

Once the candidate stress vectors for all regions of the transistors in a circuit are derived properly, the final step is to minimize the set of stress vector, i.e., the primary stress vectors. The minimal set of stress vectors guarantee to fully stress all regions. Simple rules in the minimal covering problem can be used to derive the minimal set. Figure 3(d) illustrates the set of 3 primary stress vectors. The resultant primary stress vectors are exactly the same as those generated by the simulation-based approach [14].

The structure-based stress vector generation process can also be generalized for the circuits with more than one valid path. Basically, if a circuit contains more than one valid path, only one valid path is activated at a time and the remaining paths are disabled. Thus, the circuit is equivalent to containing only one valid path. Figure 4 illustrates the resultant stress vector generation for the partitions P1, P2, and P3 of the OTA circuit.

Primary Vectors	Output
n22	n9
0	1

(a) P1

Primary Vectors			Outputs	
Vbias	Vin-	Vin+	n15	n22
1	0	0	1	1
1	1	0	0	1
1	0	1	1	0

(b) P2

Primary Vectors		Output
n9	n15	nx
1	1	0
0	0	1

(c) P3

Figure 4: Primary Vectors and Associated Outputs.

3. Hierarchical Approach

A Circuit partition scheme using the control-flow model was introduced in Section 3.1 to partition an analog CMOS IC into a number of smaller partitions, which can be comfortably handled, by both stress vector generator and stressability analyzer. This section presents both hierarchical stress vector generation and stressability analysis processes.

3.1 Hierarchical Stress Vector Generation

Recalled that a *primary partition* is the one, which is not controlled by any other partitions. The *primary inputs* are the inputs to the original circuit, and a *primary-like input* is the output

Vbias	Vin+	Vin-	c11	c12	c13	c14
1	0	0	1			
1	1					
1		1	1	1	1	1
Number of regions			1	2	2	1
Column stress time			0	0.37	18.1	84.7

c11: M7_DG; c12:M7_GS, M7_GB

c13:M6_SG,M6_BG;M6_DG.

(a) P1

Vbias	Vin+	Vin-	c21	c22	c23	c24	c25	c26	c27	c28	c29
1	0	0	1	1	1						
1	1	0	1	1			1		1		1
1	0	1	1	1		1		1		1	
Number of regions			2	2	1	1	1	1	1	1	1
Column stress time			0	0.31				0.32		18.1	

c21:M1_DG,M2_DG; c22:M5_GS,M5_GB; c23:M5_Gd;

c24:M3_GB; c25:M4_GB; c26:M3_GS; c27:M4_GS;

c28:M1_SG,M1_BG,M3_GD; c29:M2_SG,M2_BG,M4_GD.

(b) P2

of a module that takes no inputs. Therefore, a primary partition takes either the primary inputs or the primary-like inputs as its inputs, and a non-primary partition may take either the primary inputs, or the primary-like inputs, or others, referred to as the *non-primary inputs*, as its inputs.

Based on the distribution of the primary inputs, two cases can be identified:(a).All these inputs are distributed to the primary partitions; and (b). Some of these inputs are connected to the non-primary partitions.

For the former case that all the primary inputs are connected to the primary partitions, the primary stress vectors of the original circuit will be the combinations of those for the primary stress vectors for the primary partitions. Therefore, we need only to

generate the primary stress vectors for the primary partitions. Consider the OTA circuit in Figure 1, it is decomposed into three partitions P1, P2, and P3, as shown in Figure 2(c). According to the control graph in Figure 2(b), P2 is the primary partition and it takes all the primary inputs. Thus, we need only generate the primary stress vectors for P2. Figure 4(b) shows the primary stress vectors of P2 and they are also the primary stress vectors of the OTA circuit.

For the later case that some of the primary inputs are connected to the non-primary partitions, the primary stress vectors for the original circuit is derived from the control graph. More specifically, without loss of generality, assume that the highest level of the non-primary partition, which takes the primary

Vbias	Vin+	Vin-	c31	c32
1				
1	1			1
1		1	1	
Number of regions			3	3
Column stress time			0.37	18.1

c31:M9_GS,M9_GD,M9_GB; c32:M8_SG,M8_DG,M8_BG.

(c)

Vbias	Vin+	Vin-	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11
1			1	1	1								
1	1		1	1			1		1			1	
1		1	1	1		1		1		1	1		1
Number of regions			3	2	1	1	1	1	1	5	5	6	1
Column stress time			0	0.31				0.32		0.37	18.1		84.7

C1=c11+c21; C2=c22;C3=c23;C4=c24;C5=c25;C6=c26;C7=c27;

C8=c12+c31;C9=c28+c13;C10=c29+c32;C11=c14.

(d)

Figure5: Stressability Analysis for the OTA: (a)-(c) for Partitions; and (d) for Entire Circuit.

input(s), is in Level k. These partitions are referred to as L(k)-partitions. In this case, we only need to generate the primary stress vectors for those partitions whose level is less than k, and for L(k)-partitions. A backward tracking process is used to combine the primary stress vectors for the original circuit. The backward tracking process starts with the primary stress vectors of the L(k)-partitions. Based on these primary stress vectors in Level k, i.e., the output of the partitions in the Level(k-1), we track the required inputs for the partitions in Level (k-1). The backward tracking process is continued to Level (k-2). The process is repeated to Level 0 and results the primary stress vectors for the original circuit. According to this backward tracking process, for those partitions whose level is less than k, but their outputs do not contribute to L(k)-partitions, we don't need their primary stress vectors and thus we don't need to generate their primary stress vectors.

3.2 Hierarchical Stressability Analysis

Based on the selected stress vectors, the stress time calculation process [14] is employed for all partitions. The stress times of the primary partitions in Level 0 are first calculated, and the remaining partitions are processed in the sequence of their levels in the control graph. However, the partitions in the same level can be processed simultaneously.

For example, we first apply the primary stress vectors of the OTA circuit to the primary partition P2, the stressability analysis results are tabulated in Figure 5(a). the circuit simulations are conducted for the primary stress vectors with the normal and stress supply voltages, respectively, for the stress time calculation. Similarly, the stressability analysis results for P1 and P3 are shown in Figure 5(b) and 5(c), respectively.

The stressability analysis result of the original circuit can be obtained by merging those for all its partitions. More specifically, tow columns will be merged if they have the same column data and stress time. For example, in Figure 5(a), the column "c11" for P2 and "c21" for P1 have the same column 'C1" in Figure 5(d) and the number of the regions are accumulated. Similarly, column "c12" for P1 and "c31" for P3 are merged as "C8" in
Figure 5(d). As a result, Figure 5(d) is the stressability analysis result for the original OTA circuit.

4. Conclusion

This paper presents a control flow model for analog CMOS circuits and uses it to develop a circuit partition scheme. A practically large analog circuit is partitioned into many smaller sub-circuits so that the developed stress vector generator and stressability synthesizer can comfortably handle in term of computational complexity. This paper also presents a structure-based technique for stress vector generation. The primary stress vectors are generated from the circuit structure without performing circuit simulations. Both hierarchical approach and structure-based stress vector generator can significant reduce the computational needs for stressing analog circuits.

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