

A Binary–Search Switched–Current Sensing Scheme for 4–state MRAM

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ABSTRACT

A current–mode binary–search sensing scheme for a 4–state one–transistor one–magnetic tunnel junction (1T1MTJ) magneto–resistive random access memory (MRAM) is proposed. By using the switched–current technique, it is able to read data non–destructively with a magneto–resistive (MR) ratio of as low as 5%. The circuit is designed using a 0.18 μ m CMOS process and the performance is verified by HSPICE. Compared to the parallel sensing approach, the proposed sensing scheme consumes less power and chip area and requires fewer comparison steps. Compared to the serial sensing approach, it allows a shorter read access time while requiring the same number of comparisons.

Categories and Subject Descriptors

B.7.1 [Integrated Circuits]: Types and Design Styles – algorithms implemented in hardware, memory technologies.

General Terms

Algorithms, Design

Keywords

Magneto–resistive random access memory, switched–current.

1. INTRODUCTION

In 2002, a multi–state MRAM is proposed [1] in which data was written at Curie point and was read using an angular–dependent magneto–resistance. Fig.1 shows a 4–state MRAM where R_{min} is the minimum MTJ resistance when magnetization directions of free and recording layers are the same, R_{max} is the maximum resistance when the directions are opposite to each other, and $\Delta R = (R_{max} - R_{min})/R_{min}$ is the MR (magneto–resistive) ratio.

In this paper, we introduce a current–mode sensing scheme together with a switched–current (SI) sensing circuit for reading data non–destructively from a 4–state 1T1MTJ MRAM. For this 4–state MRAM, the difference in the MR ratio of adjacent states is only about 7.5% to 12.5%. The magneto–resistances are usually in the order of 10k Ω , and hence, at a low bias voltage such as

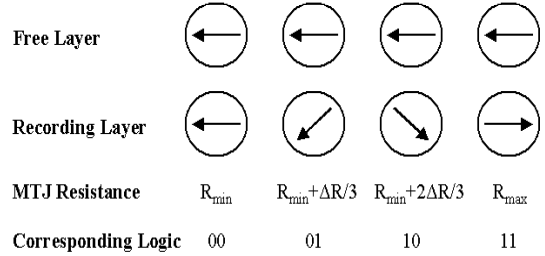


Figure 1. A 4–state MRAM structure proposed in [1].

0.3V, the difference in currents are only in the order of μ A, which are too weak for accurate and fast comparisons. By using double–regenerated SI technique, data with a difference in an MR ratio of as low as 5% can still be accessed reliably [2] and a high comparison rate can be achieved [3]. The proposed sensing circuit is designed using a 0.18 μ m CMOS process and its performance is verified by HSPICE. Section II introduces the proposed sensing scheme and Section III describes the corresponding circuit. Section IV presents simulation results and discusses the performance of the circuit. Conclusion of research efforts is drawn in Section V.

2. DOUBLE-REGENERATED SWITCHED-CURRENT SENSING SCHEME

A 4–state memory cell has 4 symbols, and each symbol is represented by $\log_2(4)=2$ bits. Therefore, determining the content of the data is equivalent to determining the logic states of these two bits, the most significant bit (MSB) and the least significant bit (LSB). Our goal is to design a sensing scheme that minimizes the number of comparison steps and shortens the read access time. Referring to the 2–state sensing scheme proposed in [4], if one bit of information is stored in an MTJ with resistance R_{bit} , where $R_{bit} = R_{min}$ if the magnetization directions are parallel and $R_{bit} = R_{max}$ if the directions are anti–parallel, reading is performed by comparing R_{bit} with the resistance of a reference cell $R_{ref} = R_{min}$. In [5], an improved referencing scheme was proposed. The reference cell is constructed by paralleling 2 series connections of R_{min} and R_{max} . The reference resistance is thus $R_{ref} = R_{ave} = (R_{min} + R_{max})/2$. The logic state of the data can be found as follows:

$$\text{Logic state of the data} = \begin{cases} 0 & \text{if } R_{bit} < R_{ref} \\ 1 & \text{if } R_{bit} > R_{ref} \end{cases}$$

Based on this mechanism, one alternative for sensing a 4–state cell is to compare the cell resistance R_{mtj} in parallel with 3

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different reference resistances using 3 sense amplifiers and a decoder [6]. Although this method can read data at high speed, the number of comparisons required is large and the chip consumes much power. On the other hand, a serial sensing approach [7] was employed to perform successive comparisons using a sense amplifier. Compared to the parallel sensing approach, the power consumption is lower and chip area is smaller, but the read access time is much slower. In order to minimize the number of comparisons, the power consumption and the chip area, a binary-search sensing scheme is proposed in which the comparisons are based on the binary search scheme (Fig.2). The algorithm of finding the MSB and LSB is as follows:

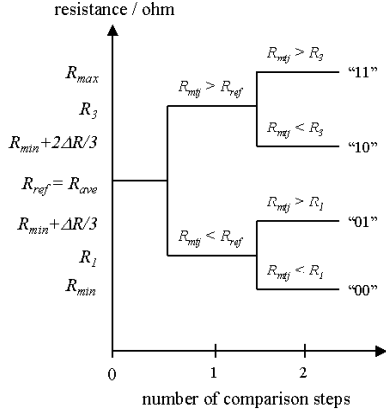


Figure 2. The binary-search scheme for finding MSB and LSB

1. **Determine the MSB.** If the cell resistance R_{mij} is larger than $R_{ref} = R_{ave}$, then MSB = 1. Otherwise, MSB = 0.
2. **Determine the LSB.** Once the MSB is determined, the LSB can be determined by comparing R_{mij} with either R_l or R_3 . If MSB = 0, i.e., $R_{mij} < R_{ref}$, then R_{mij} is compared with R_l .

$$[\text{MSB}, \text{LSB}] = \begin{cases} 00 & \text{if } R_{mij} < R_{ref} \text{ and } R_{mij} < R_l \\ 01 & \text{if } R_{mij} < R_{ref} \text{ and } R_{mij} > R_l \end{cases}$$

If MSB = 1, i.e. $R_{mij} > R_{ref}$, then R_{mij} is compared with R_3 :

$$[\text{MSB}, \text{LSB}] = \begin{cases} 10 & \text{if } R_{mij} > R_{ref} \text{ and } R_{mij} < R_3 \\ 11 & \text{if } R_{mij} > R_{ref} \text{ and } R_{mij} > R_3 \end{cases}$$

where $R_l = [R_{min} + (R_{min} + \Delta R/3)]/2$, $R_3 = [(R_{min} + 2\Delta R/3) + R_{max}]/2$.

In this way, once the MSB is determined in the first comparator, it can be passed into the second comparator immediately to determine the LSB without waiting for the first one to settle. Compared to the serial sensing approach in which only one sense amplifier is used, the read access time is improved. In addition, only one reference resistance $R_{ref} = R_{ave}$ is required. The other reference resistances, R_l and R_3 , can simply be obtained by shifting R_{ref} up or down by an offset generated by a control logic that will be discussed in Section 3.5.

3. BINARY-SEARCH SENSING CIRCUIT

The sensing circuitry should be compact in design, consume low power and operate at high speed. Fig.3 shows the block diagram of our proposed sensing circuit.

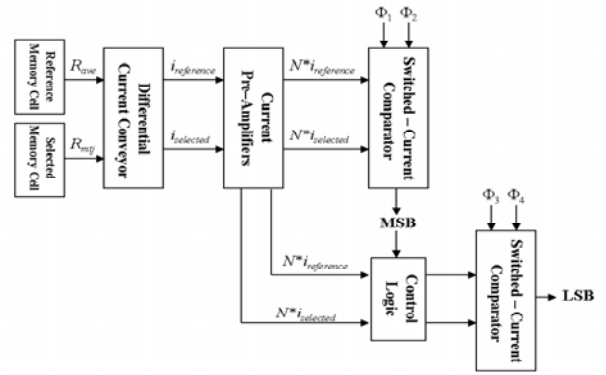


Figure 3. The proposed sensing circuit.

3.1 4-State Memory Cells

To ensure a very good matching between the selected and reference cells, the design of the reference cell follows [5], i.e. R_{ref} is generated by paralleling 2 series connections of R_{min} and R_{max} to obtain an average resistance R_{ave} . Fig.4 shows the reference and selected cells with resistances R_{ref} and R_{mij} .

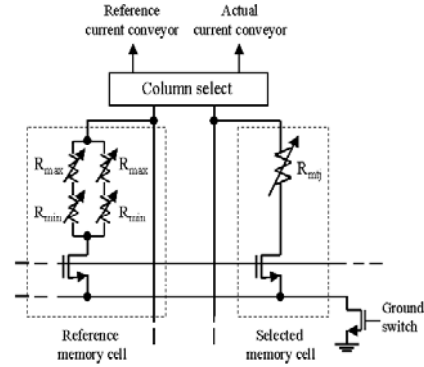


Figure 4. The reference and selected memory cells.

3.2 Differential Current Conveyor

In [4], the differential current conveyor senses the resistances from the selected and reference cells and converts them into voltages, which are passed to a 2-stage voltage-mode comparator and a regenerator to determine the content of the selected cell. If a current-mode comparator is used instead, the current-to-voltage conversion is not required and the structure of the conveyor can be simplified. This current-mode differential conveyor (Fig.5) consists of an actual and a reference current conveyors. Each conveyor is comprised of a voltage source, an operational amplifier (op-amp) and a MOS transistor. Op-amp A_0 and A_0' are used to generate currents $i_{mij} = V_{bias}/R_{mij}$ and $i_{ave} = V_{bias}/R_{ave}$, where V_{bias} is the bias voltage. Since the output resistances of the amplifiers are comparable to the magneto-resistances, current buffers M_0 and M_0' are used to drive the resistances. The actual conveyor operates as follows. A current source i_S generated from a voltage source V_b is split into 2 portions. One portion, i_{mij} , flows into the cell, whereas another portion, $i_{selected} = i_S - i_{mij}$, flows into a current pre-amplifier. The same procedure applies to the reference conveyor with $i_{reference} = i_S - i_{ave}$. These difference currents

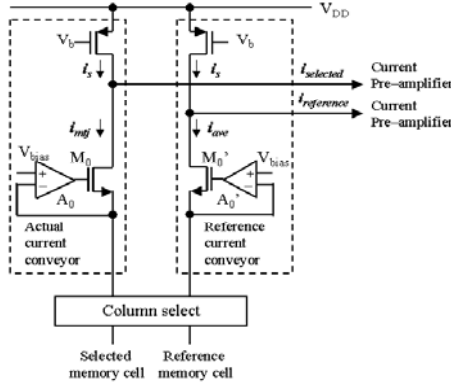


Figure 5. The differential current conveyor.

are then passed into succeeding stages to determine the content of the cell.

3.3 Current Pre-Amplifier

Referring to Fig.3, the currents $i_{selected}$ and $i_{reference}$ are passed into the current pre-amplifiers (Fig.6) with output currents $N*i_{selected}$ and $N*i_{reference}$ where N is a number greater than or equal to 1. The reasons of using pre-amplifiers are explained below.

1. The larger the difference in current levels, the larger the signal resolution for comparison. If $i_{selected}$ and $i_{reference}$ are too small, they should be amplified before passing into the comparators.
2. To prevent kickback. Referring to Fig.4, the currents are first passed into an SI comparator in phases ϕ_1 and ϕ_2 to determine the MSB and then passed into the control logic and the second comparator in phases ϕ_3 and ϕ_4 to determine the LSB. If there is no buffer to store the currents, kickback would corrupt the

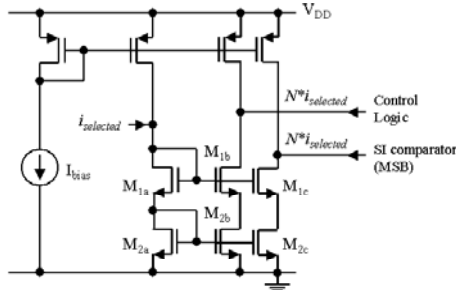


Figure 6. The current pre-amplifier.

currents to be passed into the second comparator in phases ϕ_3 and ϕ_4 , resulting in a very limited comparison accuracy [8].

3.4 Double-Regenerated SI Comparator in Φ_1 and Φ_2

Recall the MSB of a data is determined by comparing its resistance R_{mtj} with R_{ave} . This comparison can be implemented by comparing the current $i_{selected}$ with $i_{reference}$ as follows:

$$[MSB] = \begin{cases} 0 & \text{if } i_{selected} > i_{reference} \\ 1 & \text{if } i_{selected} < i_{reference} \end{cases}$$

Fig.7 shows the double-regenerated SI comparator used for current comparison. It is a simplified and power-saving version of [3] with only 2 clock phases. The main advantage is to reduce the

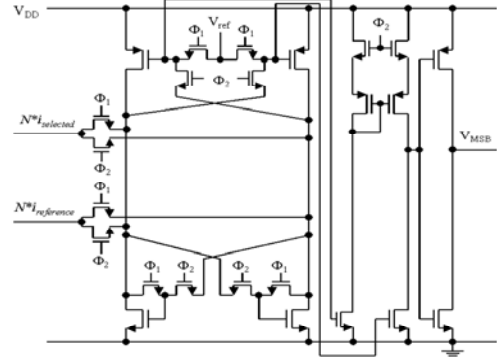


Figure 7. The double-regenerated switched-current comparator with 2-phase clock.

complexity and generation of clock phases. Please refer to [2] for a detailed description of the comparator's operation.

3.5 Control Logic and Double-Regenerated SI Comparator in Φ_3 and Φ_4

The task of the control logic to determine the LSB. If $MSB = 1$, the LSB is determined by comparing R_{mtj} with $R_3 = (R_{min} + 2\Delta R/3 + R_{max})/2$. If $MSB = 0$, the LSB is determined by comparing R_{mtj} with $R_1 = (R_{min} + R_{min} + \Delta R/3)/2$. In our control logic, only one extra current source and 2 MOS switches are used (Fig.8). Given two input currents $N*i_{selected}$ and $N*i_{reference}$ and the MSB, our goal is to shift one of the currents to a particular level and pass it to the comparator in phases ϕ_3 and ϕ_4 for comparison:

1. If $MSB = 1$, the transistor M_3' is on and an extra current $i_{control}$ is added to $N*i_{selected}$. The current representing the selected cell becomes $N*i_{selected} + i_{control}$. If $N*i_{selected} + i_{control} < N*i_{reference}$, the LSB is set to "0" and $R_{mtj} = R_{min} + 2\Delta R/3$. If $N*i_{selected} + i_{control} > N*i_{reference}$, the LSB is set to "1" and $R_{mtj} = R_{max}$.
2. If $MSB = 0$, the transistor M_3 is on and an extra current $i_{control}$ is added to $N*i_{reference}$. The current representing the reference cell becomes $N*i_{reference} + i_{control}$. If $N*i_{selected} < N*i_{reference} + i_{control}$, the LSB is set to "0" and $R_{mtj} = R_{min}$. If $N*i_{selected} > N*i_{reference} + i_{control}$, the LSB is set to "1" and

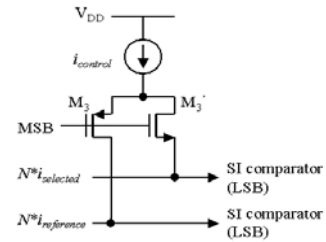


Figure 8. The control logic.

$$R_{mtj} = R_{min} + \Delta R/3.$$

At the end of the comparison, the circuit is back to its initial condition and is ready for the next operation.

4. PERFORMANCE EVALUATION

The circuit is designed using a 0.18 μ m CMOS process, and operated at a supply voltage of 2.4V. HSPICE simulations are performed at $V_{bias} = 0.3V$, the MR ratio of 37% and $N = 2$. Fig.9

shows the output transient response of (a) MSB and (b) LSB in which data “00”, “01”, “10”, and “11” are read in the four successive read cycles. The read cycle time and access time are 21.5ns and 17.5ns, the active current and power consumption are 0.588mA and 1.41mW. Fig. 10 shows the transient response of

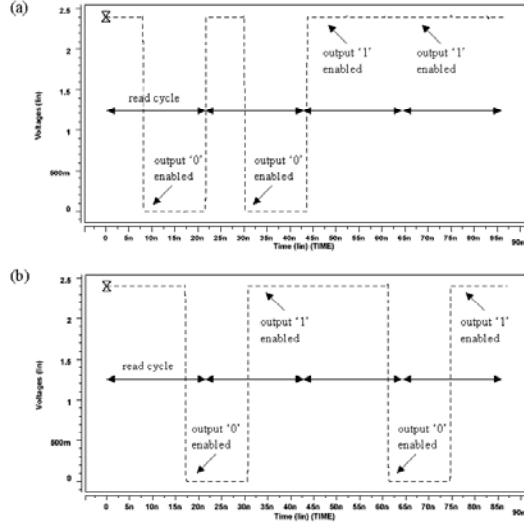


Figure 9. Output transient response of (a) MSB; (b) LSB of the data with a MR ratio of 37% at 2.4V

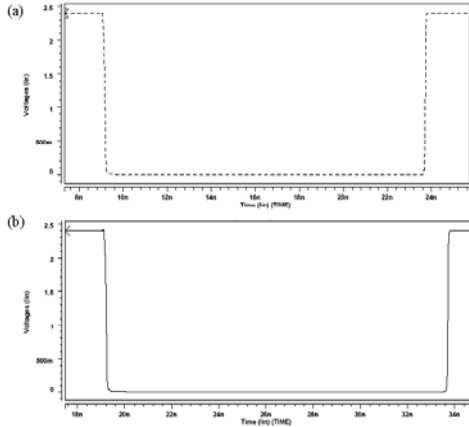


Figure 10. Output transient response of (a) MSB; (b) LSB of the data with a MR ratio of 37% at 2.4V over one cycle

the MSB and LSB in the first cycle. It is observed that the fall time and the rise time are about 0.5ns and 0.2ns, respectively.

In order to demonstrate the ability of the sensing circuit to detect weak currents, another simulation (Fig. 11) is performed in which the MR ratio is 20% at $V_{bias} = 0.3V$. In this case, the difference in MR ratio of adjacent states is only 5%. The read cycle time and access time are 23.5ns and 19.5ns. The results indicate that the circuit is able to read the data with a smaller MR ratio at the expense of longer read cycle time and access time.

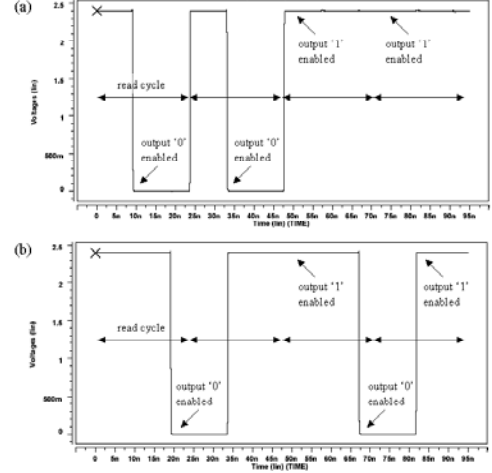


Figure 11. Output transient response of (a) MSB; (b) LSB of the data with a MR ratio of 5% at 2.4V

5. CONCLUSION

A switched-current binary-search sensing scheme is proposed to read data non-destructively from a 4-state 1T1MTJ MRAM. Compared to the conventional parallel sensing approach, it requires fewer comparison steps and lower power consumption. Compared to the serial sensing approach, it has a shorter read access time. Simulation results show that the sensing circuit can operate at a comparison rate of greater than 40MHz at a supply voltage of 2.4V with an MR ratio of as low as 5%.

6. ACKNOWLEDGEMENTS

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