Design and Optimization of Board-Level Optical Clock Distribution Network for High-Performance Optoelectronic System-on-a-Packages

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ABSTRACT
A new approach to optical clock distribution utilizing optical waveguide interconnect technology is introduced. In this paper, we develop a new algorithm for design and optimization of board-level optical clock distribution network for high-performance optoelectronic system-on-a-packages. The optimization approach takes into account bending and propagation losses of optical waveguides. Less than 26.1psec in signal timing skew is obtained for a signal flight time of 614.38psec. About 15% reduction in optical power consumption is also obtained over clock nets routed with existing (optical) methods.

Categories and Subject Descriptors
B.4.3 [**Interconnections (Subsystems)**].

General Terms
Algorithms.

Keywords
Clock distribution, clock routing, optical clock distribution, H-tree, asymmetric structure, optimization, optical waveguide loss modeling, optoelectronic system-on-a-package.

1. INTRODUCTION
Due to increasing levels of integration and sophistication in packaging technologies, the problem of routing electrical control and synchronization signals to the various subsystems of the package has assumed great significance. These control and synchronization signal networks, such as the clock distribution networks discussed in this paper, have to be designed very carefully in order to maximize the performance of the assembled electronic package while minimizing manufacturing costs. Specifically, for clock distribution, the skew of the clock signal from the source to the various destination points must be minimized in order to maximize the electrical performance of the package. In addition, overall power consumption must be minimized. These stringent design requirements necessitate the development of new computer-aided design (CAD) algorithms for emerging technologies such as optical interconnect.

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In 1984, J. W. Goodman suggested three optical clock distribution approaches [1]: unfocused free-space, focused free-space and index-guided optical interconnect. Free-space optical interconnect technology is suitable for routing on-chip interconnects using an optical interconnect layer. Special lenses and diffraction gratings are employed to route signals optically from point on the silicon die to another. This paper discusses a CAD algorithm for optimal routing of clock signals using index-guided optical interconnect. This employs advanced technology in which optical waveguides are directly integrated into the package substrate. The approach provides a compact and planar packaging of the global optical clock distribution.

A multi-GHz optical clock distribution on a Cray T-90 supercomputer multi-processor board is presented in 1999 [2]. The optical clock signal is distributed to 48 fanout points on $14.5\times27cm^2$ printed wiring board through a polyimide optical waveguide organized as an H-tree structure.

In this paper, we develop "***BOSS***" (Board-level Optical clock Synthesis and Simulation tool), a CAD tool that finds an optimal clock routing network and a best optical data input location for the network utilizing optical waveguide technology. Figure 1 shows the BOSS program layout with two simulation results of symmetric 64-fanout. The right window layout is an optimized layout of the layout shown on the left window.

Figure 1. The BOSS layout with a symmetric structure simulation

The physical design of the optical clock distribution network is composed of three steps: *partitioning*, *rough routing* and

calibration for clock skew. The three steps are described in detail in Section 4.2, 4.3 and 4.5.

2. PROBLEM DESCRIPTION

The integration configuration of an optical clock routing on system-on-a-package (SOP) substrate that is discussed in this paper is shown in Figure 2.

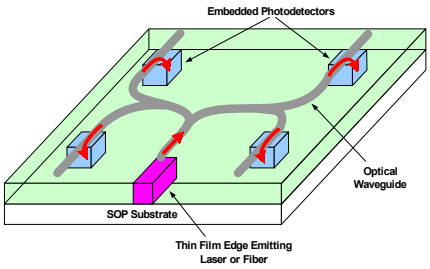


Figure 2. Integration configuration for high-speed optical clock distribution using embedded optoelectronics

In this paper, we design clock distribution networks using optical waveguide interconnections instead of electrical interconnections. It translates that other factors from replacing electrical interconnections with optical interconnections should be considered to design optical clock distribution networks. Therefore, two major losses are considered and modeled in Section 3, which are optical waveguide bending losses and inherent optical waveguide losses.

Using the loss models, we develop a new CAD algorithm that finds an optimal clock routing network and a best optical data input location for the network utilizing optical waveguide technology in Section 4.

3. MODELING OF OPTICAL WAVEGUIDE

Two major loss terms, *optical waveguide bending losses* and *inherent optical waveguide losses*, in an index-guided optical interconnect are considered to evaluate layouts from the simulation results.

3.1 Optical Waveguide Bending Losses

Figure 3 shows a fundamental guided mode wavefront is traveling in an optical waveguide.

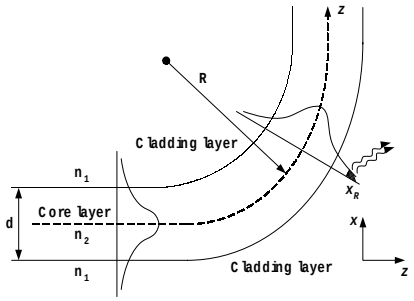


Figure 3. Bending loss derivation

When the mode passes through the bent optical waveguide, tangential velocity of the mode in a cladding layer, $v_{tan}=R(d\theta/dt)$ will exceed the velocity of light. Thus, the portion of the evanescent field tail x_R cannot stay in phase and splits away from the guided mode and radiates into a cladding layer.

The rate of total power loss along z can be described by,

$$-\frac{dP_m(z)}{dz} = \alpha_m P_m(z) \quad (1)$$

where α_m is the proportionality constant.

From Equation (1), the guided power for m^{th} mode can be written as,

$$P_m(z) = P_{0,m} e^{-2\alpha_m z} \quad (2)$$

where $P_{0,m}$ is the incident power for m^{th} mode and $z=\pi R/2$.

The α_m can be easily derived by calculating radiating aperture [3].

$$\alpha_m = C_1 e^{-2C_2 R} \quad (3)$$

where C_1 and C_2 are constants.

Therefore, Equation (2) is a function of bending radius of optical waveguide.

The result of bending loss with specific parameters is curve-fitted with Boltzmann function to specify to BOSS. The parameters which are used in this paper are taken from a real fabrication condition [4]. They are 1μm Benzocyclobutene (BCB) as a core layer, SiO_2 as a cladding layer, 1μm waveguide thickness and a wavelength of 1.3μm. The analytical regression model for the bending loss of optical waveguide is shown in Equation (4).

$$\text{Bending Loss} = [1.0508/(1+e^{(\text{radius}-4\times10^{-5})/10^{-5}})]+9.9\times10^{-4} \quad (4)$$

Equation (4) tells that the result is saturated over 240μm bending radius of optical waveguide. It translates that the bending loss is negligible over 240μm bending radius. For the simulations, the minimum bending radius of optical waveguide is assumed to be 100μm.

3.2 Inherent Optical Waveguide Losses

In optical waveguide, material absorption loss and propagation loss are directly proportional to its material. From the physical design point of view, the losses are related to the path length from a location of an optical signal input to a detector. Therefore, the algorithm minimizes the path length using maximum bending radii of optical waveguides with the restriction that there is no cross over among optical waveguides. For evaluation, the propagation loss is set to be 0.36dB/cm at a wavelength of 1.3μm measured by a fiber scanning method [4]. However, the splitting loss of optical waveguide is assumed to be negligible in this paper. As a reference, B. Bihari, *et al* show that the splitting loss is reduced to 0.4dB per splitter in their experiments [2].

3.3 Clock Signal Timing Skew Calculation

The effective refractive index of TE_0 mode in the dielectric waveguide is about 1.537. c is the speed of light in free-space. n is effective refractive index. λ is 1.3μm. $dn/d\lambda$ is approximately calculated with conventional BCB material, which is 3022 family [5]. v_g is the group velocity of the guided mode in the material with an ideal monochromatic optical source.

$$\upsilon_g = c\left[n - \lambda\frac{dn}{d\lambda}\right]^{-1} \approx 1.93675\times10^8\,(\text{m/s}) \quad (5)$$

Thus, delay $d_{optical}$ is

$$d_{optical} = \frac{x}{\upsilon_g} = \frac{x}{1.93675 \times 10^8} (\text{sec}) \quad (6)$$

where x = (a path length – the shortest path length).

However, the delay $d_{electrical}$ in electrical interconnection is

$$d_{electrical} = \frac{x}{c/5} = \frac{x}{0.6 \times 10^8} (\text{sec}) \quad (7)$$

because the signal propagation speed for repeatered global electrical interconnections can be assumed to be approximately c/5 [6].

In order to minimize clock skew, BOSS finds the maximum bending radius with the assumptions that are made in Section 4.1. This implies that path lengths are minimized and clock skews are also minimized with a given partitions and routing.

4. OPTIMIZATION ALGORITHM

The optimization goals are as follows:

- *Given*: The locations of all the terminal points (detectors) to which the clock signal is to be routed optically.
- *Determine*: (a) The location of the clock signal transmitter on the printed wiring board and (b) the optimal layout of the optical waveguides from the transmitter to each of the detectors.
- *Such that (optimization criteria)*: (a) clock signal skew is minimized and (b) bending and propagation losses due to the optical waveguides are minimized.

The optimization algorithm consists of a *layout partitioning step*, a *waveguide routing step* and a *local routing heuristic* step. These are described next.

4.1 Design Assumptions

It is assumed that different combinations of L-shaped waveguides (90° bent L-shape) are used to construct the optimal optical routing network. This provides flexibility of design as opposed to the use of a rigid H-tree structure. The optical waveguide is assumed to be Transverse Electric (TE) field polarized with single mode operation. It is also assumed that there is an isolation layer between electrical and optical substrate to avoid signal-absorption. The final layout is a 1-to-2^x fanout structure where x>1. This means that the system is a single clock system and the number of detectors on board is 2^x where x>1.

From the viewpoint of signal latency, optical interconnection has three types of latencies: transmitter latency, the time of flight and receiver latency. In this paper, the latencies in the optical transmitter and the optical receiver are not considered. However, it is reported that they are less than 100psec respectively in recent publication [7].

4.2 Layout Partitioning

The X-Y partition algorithm is used [8] to group two detectors as one group, so that we can find its "optical centroid" (see Section 4.3) in the next clock routing phase. The board B is partitioned into two subregions, B_L and B_R with equal number of detectors. The subregions B_L and B_R are then partitioned in the orthogonal direction. Alternating x- and y-direction partitioning is recursively performed until there are two detectors in each subregion. The algorithm is illustrated in Figure 4.

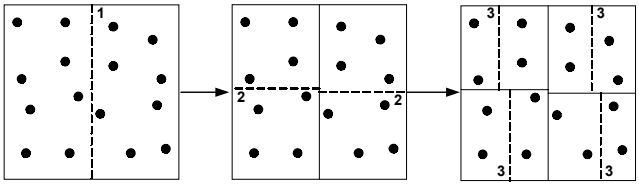


Figure 4. X-Y partition algorithm

4.3 Optical Clock Routing

For electrical clock distribution, the skew of the clock signal from the source to the various destination points must be minimized in order to maximize the electrical performance of a package. Exact zero skew algorithms using Elmore delay model have been developed for electrical clock routing [9-11].

For optical clock distribution, an algorithm which we call *the Method of Optical Centroid Searching (MOCS)* is developed. The basic idea of the MOCS algorithm is to minimize the path length difference from the transmitter to any of the detectors by finding "optical centroid" based upon Manhattan Geometry. These optical centroids represent points in the layout grid that are *equidistant* from all other points in the same layout partition at each step of the recursive layout partitioning process. Hence, there are as many optical centroids as there are recursive calls in the layout partitioning algorithm. In order to feed all the detectors corresponding to a layout partition, the signal feeding the detectors is fanned out to the detectors or other optical centroids at the optical centroid corresponding to the partition. The MOCS algorithm is illustrated in Figure 5.

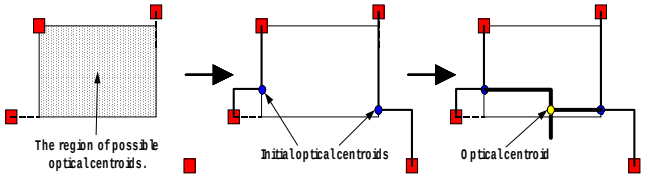


Figure 5. The method of optical centroid searching

Let C be a set of 4 optical centroids. It is assumed that 4 detectors are initially set as the first optical centroids.

$$C(x) = \{c_x(i) \mid c_x(i) \text{ is centroid sorted in x-direction}\}$$

$$C(y) = \{c_y(i) \mid c_y(i) \text{ is centroid sorted in y-direction}\}$$

where i = (1,2,3,4).

The next optical centroids of C are located in region R_C.

$$R_C = \{x, y \mid (c_x(2) \le x \le c_x(3)) \cap (c_y(2) \le y \le c_y(3))\}$$

Let C_L, C_R, C_T and C_B be initial optical centroids and C_M be the next optical centroid which is a yellow dot in Figure 5. Let PL_L, PL_R, PL_T and PL_B be path lengths from the left, right, top and bottom optical centroid to the detectors on the left, right, top and bottom side.

The pseudo code for recursive MOCS is given in Figure 6. This MOCS are recursively introduced until there is only one optical centroid after searching.

```
Find_optical_centroid( )
1.  for (all the segments by X-Y partitioning ) {
2.      decide waveguide proceeding direction;
3.      if (waveguide proceeding direction is up or down) {
4.          abs_height = abs(C_L(y) –C_R(y));
5.          difference = abs(PL_L–PL_R);
6.          PL_1 = PL_L; PL_2 = PL_R; C_1 = C_L(y); C_2 = C_R(y);
7.      }
8.      else {
9.          abs_height = abs(C_T(x)-C_B(x));
10.         difference = abs(PL_T–PL_B);
11.         PL_1 = PL_T; PL_2 = PL_B; C_1 = C_T(x); C_2 = C_B(x);
12.     }
13.     if (PL_1 > PL_2) {
14.         if ((down and C_1 < C_2) or (up and C_1 > C_2)) {
15.             d_1 = C_1 – abs_height; d_2 = C_2 –difference;
16.         }
17.         else if ((down and C_1 >= C_2) or (up and C_1 <= C_2))  {
18.             d_1 = C_1; d_2 = C_2 –difference+ abs_height;
19.         }
20.         else if ((left and C_1 < C_2) or (right and C_1 > C_2)) {
21.             d_1 = C_1; d_2 = C_2 –difference– abs_height;
22.         }
23.         else {
24.             d_1 = C_1+ abs_height; d_2 = C_2 –difference;
25.         }
26.     else {
27.         if ((down and C_1 < C_2) or (up and C_1 > C_2)) {
28.             d_1 = C_1+difference– abs_height; d_2 = C_2;
29.         }
30.         else if ((down and C_1 >= C_2) or (up and C_1 <= C_2)) {
31.             d_1 = C_1+difference; d_2 = C_2+ abs_height;
32.         }
33.         else if ((left and C_1 < C_2) or (right and C_1 > C_2)) {
34.             d_1 = C_1+ abs_height; d_2 = C_2 –difference;
35.         }
36.         else {
37.             d_1 = C_1; d_2 = C_2– difference –abs_height;
38.         }
39.     }
40.     leng_diff = (d_2 – d_1)/2;
41.     if (waveguide proceeding direction is up or down) {
42.         C_M(x) = x1 + leng_diff;
43.         if (C_1 < C_2) C_M(y) = C_2;
44.         else C_M(y) = C_1;
45.     }
46.     else {
47.         C_M(y) = y1 + leng_diff;
48.         if (C_1 < C_2) C_M(x) = C_2;
49.         else C_M(x) = C_1;
50.     }
51.     Find_optical_centroid( );
52. }
53. Find the best location of an optical data input (Section 4.4);
```

Figure 6. Pseudo code for MOCS algorithm

For routing, any optical waveguide cannot cross any other optical waveguide or any detector to avoid inducing significant power loss caused by a discontinuity at the intersection.

4.4 Optical Data Input Location

As mentioned earlier, the system designed in this paper is a single clock system. BOSS provides layouts of 1-to-2^x fanout (x>1). The optical data input location is determined at the end of routing through the MOCS (Method of Optical Centroid Searching) algorithm. The x coordinate is same as the last optical centroid and they coordinate is the bottom of the board.

4.5 Local Routing Heuristic

For each optical centroid, the maximum bending radius is different. An example of the first local routing stage is shown in Figure 7.

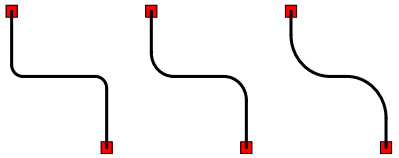


Figure 7. An example layout with different bending radii

Different bending radius causes a length difference between optical data input and detector. This results in signal timing skew. Thereby, bending radii of all waveguides corresponding to the n^{th} stage of recursion are all identical to avoid signal timing skew. The n^{th} stage of recursion in Figure 6 corresponds to a local layout of the optical waveguides from a centroid (*local centroid*) to other centroids (*sub-centroids*) or a set of detectors. For routing from a local centroid to a sub-centroid, the ideal choice is to pick a waveguide layout with the largest bending radius. This minimizes bending losses. However, use of interconnect with different bending radius (see Figure 7) can cause timing skews between the various signal paths. Thus, all waveguides are routed using the smallest bending radius (of the largest for each interconnect) over all the interconnects from the local centroid to all the sub-centroids. This is called the *local routing heuristic*. The pseudo code for local routing heuristic is as follows:

```
Local_routing_heuristic( )
1.  X-Y partitioning (Section 4.2);
2.  Find_optical_centroid( ) (Figure 5);
3.  for (each partition) {
4.      Find the maximal bending radius for the optical
        centroids at each partition;
5.      bending radius = the smallest bending radius
        among the optimal bending radii of each stage;
6.  }
7.  Calculate total loss (Section 3.1 and 3.2);
8.  Calculate delay (Section 3.3);
```

Figure 8. Pseudo code for local routing heuristic

5. RESULTS AND ANALYSIS

5.1 Preliminary Result

The preliminary result for a 4-fanout structure is shown in Figure 9.

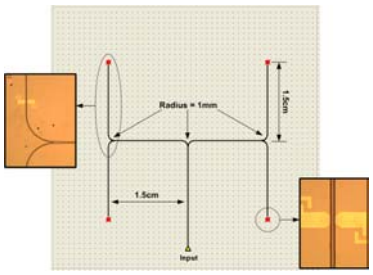
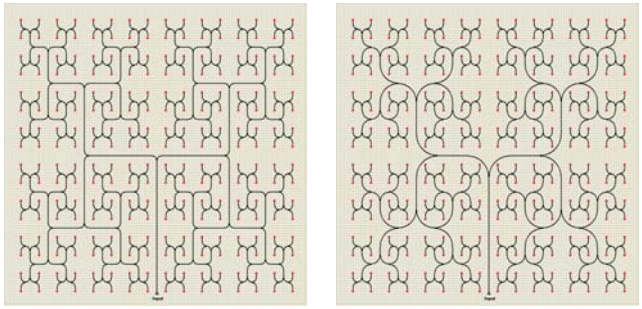


Figure 9. 1-to-4 H-tree structure layout with two enlarged microphotographs of fabrication

This design was designed using BOSS and fabricated. Two microphotographs corresponding to the fabricated Inverted-Metal Semiconductor Metal (I-MSM) photodetectors embedded in the BCB (Benzocyclobutene) polymer waveguide on the SiO_2/Si substrate are also shown in Figure 9. The dimension of the board is $5\times5cm^2$. The bending radii of the optical waveguides are respectively 1mm.

5.2 Symmetric Structure

An H-tree system with fanout of 256 has been designed. Figure 10(a) shows the layout before optimization. The dimension of the board is $10\times10cm^2$ and the bending radius is 1.5mm. The length between detectors is 6mm in the x- and y-directions. The optimized layout of Figure 10(a) is shown in Figure 10(b) through the use of waveguides with different bending radii.



(a) (b)

Figure 10. Symmetric clock routing of fanout 256 (a) before and (b) after optimization

This was carefully designed to avoid waveguide-crossing. The bending radii of each stage from a detector to an optical data input are 1.5, 1.5, 3, 3, 6, 6, 7 and 7mm. The total loss of the longest path from an optical data input to a detector due to changing bending radius is calculated and shown in Figure 11.

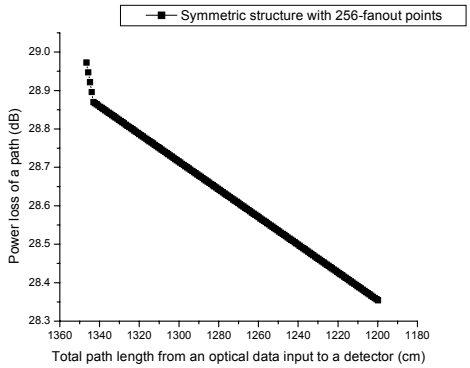


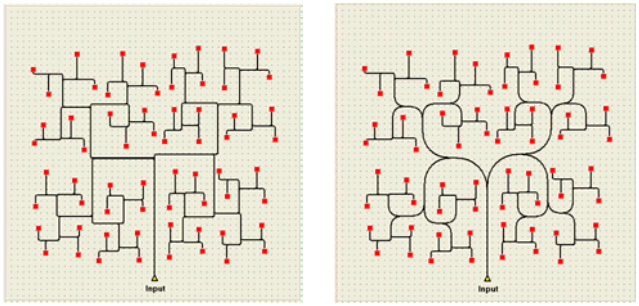
Figure 11. The reduction graph of total optical power loss of the longest path from an optical data input to a photodetector

The total loss includes the bending loss of optical waveguide, the propagation loss and the splitting loss described in Section 3. The maximum power saving after optimization is about 15%.

5.3 Asymmetric Structure

With the new L-shaped optical waveguide, BOSS can design asymmetric structures while finding the best location of the optical data input.

Figure 12 shows an asymmetric clock routing of fanout 64 utilizing the proposed MOCS algorithm (see Section 4.3) with L-shape optical waveguide. The dimension of the board is $5\times5cm^2$. Each bending radius is 200μm. Through the use of different bending radii, the layout of Figure 12(a) is optimized and results in the layout of Figure 12(b).

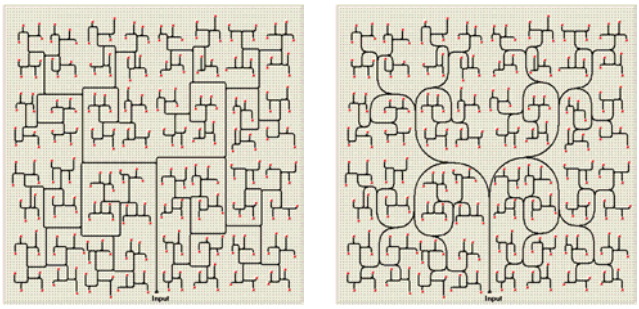


(a) (b)

Figure 12. Asymmetric clock routing of fanout 64 (a) before and (b) after optimization

The bending radii of each stage from a detector to an optical data input are 0.2, 0.2, 1.5, 1.8, 4.2, and 5.0mm.

Another asymmetric clock routing of fanout 256 is designed in Figure 13. The layout is very similar to the H-tree structure. The dimension of the board is $10\times10cm^2$. Each bending radius is 400μm. Figure 13(b) is an optimized version of Figure 13(a) with different bending radii - note that no additional timing skew is introduced in Figure 13(b) as opposed to Figure 13(a).



(a) (b)

Figure 13. Asymmetric clock routing of fanout 256 (a) before and (b) after optimization

The bending radii of each stage from a detector to an optical data input are 0.4, 0.4, 1.5, 1.5, 4.8, 5.4, 10.8 and 11.6mm.

5.4 Optical Power Loss and Signal Timing Skew

Table 1 shows the total power loss along the longest path for each bending stage. As described earlier, the bending loss exceeded 240μm bending is negligible. That is the reason the results don't seem to be affected by the bending loss.

Table 1. Power loss along the longest path for each stage (dB)

Structure \ Stage		1	2	3	4	5	6	7	8
Sym-metric	16	3.82	7.12	10.3	13.9				
	64	3.84	7.12	10.3	13.4	16.5	20.1		
	256	4.58	8.34	11.7	15.0	18.2	21.4	24.4	27.6
Asym-metric	64	3.99	7.90	11.2	14.3	17.4	21.0		
	256	4.61	8.39	11.9	15.2	18.5	21.6	24.6	27.8

Table 2 shows minimum, maximum, average signal timing skew and the maximum time of signal flight along the longest path for different structures.

Table 2. Signal timing skew along the longest path

Structure \ Skew		Minimum (psec)	Maximum (psec)	Average (psec)	Time of flight (psec)
Sym-metric	16	0	0	0	163.91
	64	0	0	0	240.16
	256	0	0	0	599.89
Asym-metric	64	7.5	7.5	1.28	255.82
	256	23.9	26.1	3.48	614.38

The maximum signal timing skew is about 26.1psec when the time of signal flight is 614.38psec. This result implicates that signal timing skew in the simulation structures is negligible (< 4%). For the same structure with electrical interconnections based on Equation (7), the signal timing skew is about 87.43psec.

6. CONCLUSION

We have presented a new approach to optimized clock routing using optical waveguide. The results are very encouraging and show that less than 26.1psec in signal timing skew is obtained for a signal flight time of 614.38psec. This translates that the signal timing skew can be neglected (< 4%). For optical power consumption, about 15% reduction is also obtained over clock nets routed with existing (optical) methods.

7. ACKNOWLEDGMENTS

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