A CMOS Elliptic Low-Pass Switched Capacitor Ladder Filter for Video Communication Using Bilinear Implementation

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ABSTRACT
This paper presents an approach to design of a high frequency switched capacitor filters for video communication networks. In the case of low OSR, using common methods reduces the SNDR and accuracy of the filter. Bilinear implementation techniques are applied to an untried fifth-order elliptic SC filter, and are simulated in a 0.35μm CMOS technology. Cutoff frequency of the filter is 3.6MHz and with bilinear implementation, we achieve 72dB SFDR, 62dB THD and stop band attenuation greater than -30dB. All the capacitors are scaled down in order to reduce the settling time of the amplifiers. The circuit operates with +3V supply and typically dissipates 15 mw when sampled at 18MHz and has full swing about 1.8V.

Categories and Subject Descriptors
B.4.0 [**Hardware**]: Input Output and Data Communication – General.

General Terms
Design.

Keywords
Switched capacitor filter, Video communication filter, bilinear integrator.

1. INTRODUCTION
Switched capacitor (SC) filters have proven their high quality and simplicity. They are now considered as one of the most successful techniques in the making of analog filters in the form of integrated circuits. This success has been obtained entirely in the audio range. Many techniques are available for the exact synthesis of these filters and many circuit techniques exist for single ended and differential filters. Unfortunately, this success has not been extended to high-frequency (HF) applications. At high frequency, many problems have to be studied and solved. The HF application of these filters is very important especially in the design of integrated communication systems.

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This work has met the video communication filter specification. Therefore it provides a very interesting solution to the design of integrated filters in this range with small area and low power consumption. In this case, a low sampling frequency can be chosen as there is no anti-aliasing filter in the receiver section and the smoothing filter is assured by the monitor set [1]. A filter with this specification has been implemented on a chip by Tawfik and Sen [1] with loss-less discrete transformation. They used Leapfrog equations that simplify assigning the capacitors values and used five OTAs for a 5^{th} order filter. The drawback of this method is its single-ended realization, and fully differential realization has some crucial restrictions [1]-[8]. Consequently noise and even harmonics magnitude at the output of these kinds of filters is substantially large. Caniv and Gabriel in [9] established a new method using parallel and series combination of the all-pass filters. This method is insensitive to OTA DC-gain and the existence of all-pass filters permits direct implementation in the z- domain. However extracting the capacitance value is very difficult and a large number of OTA's are required (for example a 5^{th} order filters needs 9 OTA and some buffers). Also single-ended realization is necessary.

In this paper we used bilinear transformation in order to realize a fully differential switched capacitor filter. Bilinear transform is more precise than loss-less discrete transform especially in low OSR schemes. Therefore resultant transfer function in the z-domain is compatible with its ideal transfer function in s-domain. On the other hand, using a fully differential structure reduces noise and even harmonics magnitudes. Also, the required number of OTAs is equal to the filter degree. In section 2 SC implantation based on passive circuit is explained. OTA structure and its specifications are briefly clarified in section 3. Finally simulation results of the proposed switched capacitor filter is presented in section 4.

2. DESIGN METHODOLOGY OF SWITCHED CAPCITOR FILTERS

2.1 Leapfrog Equations and Flow Diagram
A passive circuit for doubly terminated 5^{th} order elliptic low-pass filter is illustrated in Figure 1. Values of L and C are obtained from normalized tables for normalized frequency.

Having the passive circuit of the filter, we are able to write KCL and KVL equations. As seen in Figure 1there are two transmission zeros by C_2 and C_4. Therefore, these capacitors should be changed to parallel capacitors, and then C_1+C_2 are obtained instead of C_1,

C_2+C_3+C_4 instead of C_3 and C_4+C_5 instead of C_5. Also, we should add three voltage controlled current source at node 1, 2 and 3 [1]. These changes are exposed in Figure 2.

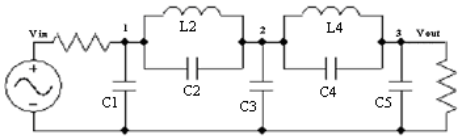


Figure 1. Passive circuit for elliptic low-pass filter

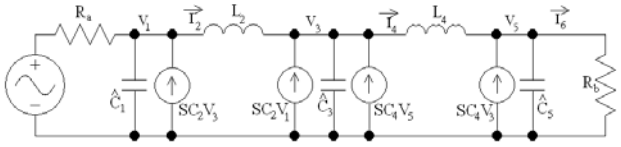


Figure 2. Altered passive circuit of ladder filter

A complete set of loop and node equations involving only integrations is shown below:

$$\hat{V}_{in} = \frac{R}{R_a}(V_{in} - V_1) \quad (1)$$

$$V_1 = \frac{1}{S\hat{C}_1 R_a}\left(\hat{V}_{in} - \hat{V}_2\right) + \frac{C_2}{\hat{C}_1}.V_3 \quad (2)$$

$$\hat{V}_2 = \frac{R}{SL_2}(V_1 - V_3) \quad (3)$$

$$V_3 = \frac{1}{S\hat{C}_3 R}\left(\hat{V}_2 - \hat{V}_4\right) + \frac{C_2}{\hat{C}_3}.V_1 + \frac{C_4}{\hat{C}_3}.V_5 \quad (4)$$

$$\hat{V}_4 = \frac{R}{SL_4}(V_3 - V_5) \quad (5)$$

$$V_5 = \frac{1}{S\hat{C}_5 R}\left(\hat{V}_4 - \hat{V}_6\right) + \frac{C_4}{\hat{C}_5}.V_3 \quad (6)$$

$$\hat{V}_6 = \frac{R}{R_L}V_5 \quad (7)$$

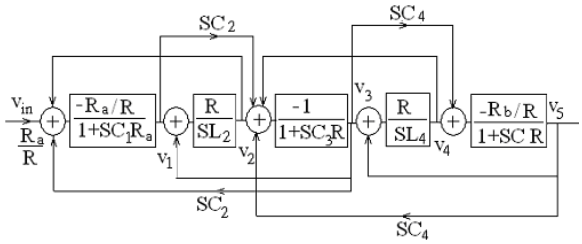


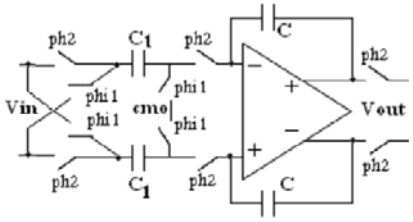
Figure 3. Signal flow diagram of leapfrog ladder filter

The flow diagram which represents these equations is shown in Figure 3. Each node voltage or branch current is defined by the signal paths flowing into it. The factor written next to each arrow, denoting the direction of the path, is the gain for that path. Multiple inputs into a single node are to be considered a summation. In this flow diagram, the nodes which represent currents produce integrations that are bordered by both voltages and currents. Since the actual implementation will use voltage-controlled voltage sources (operational amplifiers) as integrators, it is necessary to transform current nodes to voltage nodes. This is performed by multiplying all current nodes by a scaling resistance R so that the currents Z_i are now represented as the voltages V_i=RZ_i.

In order to maintain the proper relationships between the voltage and current nodes, the gain factors must also be scaled by R.

2.2 Bilinear Ladder Filter Implantation

The structures used in [1]-[6] for loss-less discrete transform don't work properly because they are sensitive to parasitic capacitances. Also, as we know loss-less discrete transform approximation is not sufficiently accurate in cases such as low OSR. In this paper, bilinear realizations of ladder circuits are proposed. First a bilinear integrator is implemented and exposed its equations in z-domain.



$$\frac{V_{out}}{V_{in}} = \frac{C_1}{C}.\frac{(1+z^{-1}}{(1-z^{-1}}$$

Figure 4. Bilinear integrator realization and its z domain equation

In Figure 4 a bilinear integrator with fully differential and parasitic insensitive structure could be realized. So the ladder filter description can be implemented based on integrators. Now S is substituted with $(T/2)(1-z^{-1})/(1+z^{-1})$ in equations (1)–(7). Then we implement the ladder SC filter structure as shown in Figure 11. Equating the s-domain and z-domain equations results the relations between L and C of the passive circuit and Capacitors of SC ladder filter.

3. OPERATIONAL AMPLIFIER

Our filter uses a telescopic fully differential amplifier, and in order to obtain a high enough gain, two fully differential auxiliary operational amplifiers act like a booster.

Contrary to previous booster designs, the booster in this work is a single-stage folded cascode operational amplifier which results in a decrease in noise magnitude and increase in the frequency of the second pole. Large frequency of the second pole results in better frequency response, faster slew rate and lower bias current of boosters which reduces power consumption. Telescopic structure is intrinsically faster, has lower power consumption and lower noise. With clever design the swing problem of the structure can be resolved.

Also choosing a folded cascode configuration for the boosters achieves a better swing. The three CMFB circuits adjust the common mode output voltages for the main Op-Amp and the two boosters. Simulation results confirm that the OTA settles in 9ns with 74dB accuracy. Power consumption of the OTA is approximately 3 mW in full swing (1.8V). In Figure 5 the schematic of the OTA is illustrated.

4. SIMULATION RESULTS

4.1 Frequency Response

Frequency response of this filter is checked with SPICE transient analysis. For finding frequency response of filter, input frequencies

were swept from 100 KHz to 9 MHz in SPICE transient analysis. A MATLAB program fetches every sweep's data and finds the maximum of each sweep. Finally a plot of these maximum values versus frequency is generated as shown in Figure 6.

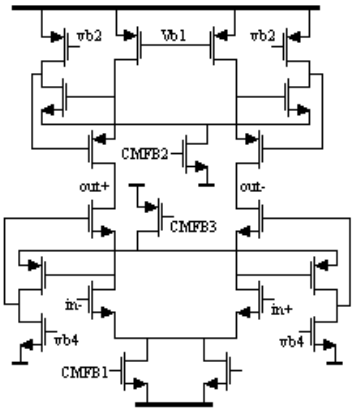


Figure 5. Proposed structure for OTA.

Figure 6. Output amplitude for 0.9V input with frequency swept from 100 KHz to 9 MHz with a step size of 50 KHz.

4.2 Transient Analysis

For checking the linearity of the filter, the filter output is given to MATLAB and FFT is calculated. To have 6 harmonics in the output spectrum, the input frequency is set to $f_{in}=(1/10).(300/1024).f_{sampling}$= 527.343 KHz. Because the cutoff frequency is 3.4MHz and the input frequency is about 527 KHz, we can only see 6 harmonics in the pass band. Transient time step is set to $T_s=1/f_s$=55nsec and a proper start time is chosen. Output voltage of the filter is shown in Figure 7. In details and it can be seen that output amplitude is not continuous, Therefore data must de read at certain intervals at the end of the clock period.

4.3 Spectrum Analysis

Spectrum analysis of the filter is performed with 1024 points FFT. The resulting spectrum is shown in Figure 8. As we see power of the fundamental frequency is 54.2dB and the greatest harmonic has -17.5dB power. So SFDR is equal to 71.7dB and THD = 61.89dB is reported by MATLAB.

4.4 Step Response

A 0.6V step is applied as an input to this filter and the step response of this filter is illustrated in Figure 9. Also the circuit operates silent mode in order to check its ability to settle down to common mode voltage. Therefore, setting the input to zero and plotting the output voltage, results in Figure 10.

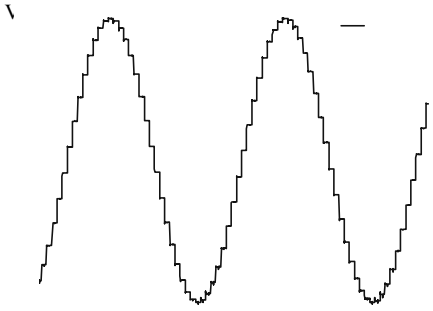


Figure 7. Continuous output of filter 10^{-6} Time

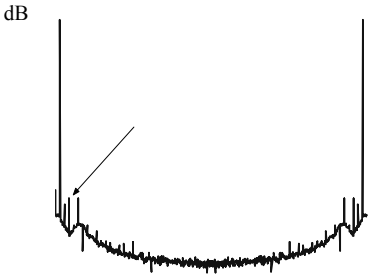


Figure 8. Filter output spectrum in details: SFDR=54.2-(-17.5) =71.7dB

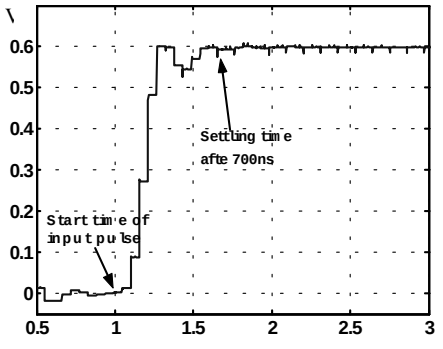


Figure 9. Step response.

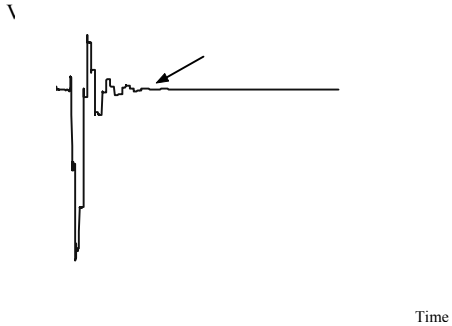


Figure 10. Output of filter with zero input

5. CONCLUSION

We have proposed a fifth order switched capacitor ladder filter with a cutoff frequency of 3.6 MHz and 18 MHz sampling frequency. Design techniques for this filter were also given, such as low sampling frequency, a bilinear transform implementation scheme and an exact synthesis algorithm. We have demonstrated that when bilinear transform and fully differential concept are taken in account, a very precise and linear filter is achieved.

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Table 1

F_{Cutoff}	3.6 MHz
Pass band ripple	<0.1 dB
$F_{attenuation}$	4.5 MHz
Minimum attenuation	35 dB
THD	63dB
SFDR	73dB
Input swing	1.8V
Output swing	1.8V
Technology	CMOS 0.35µm

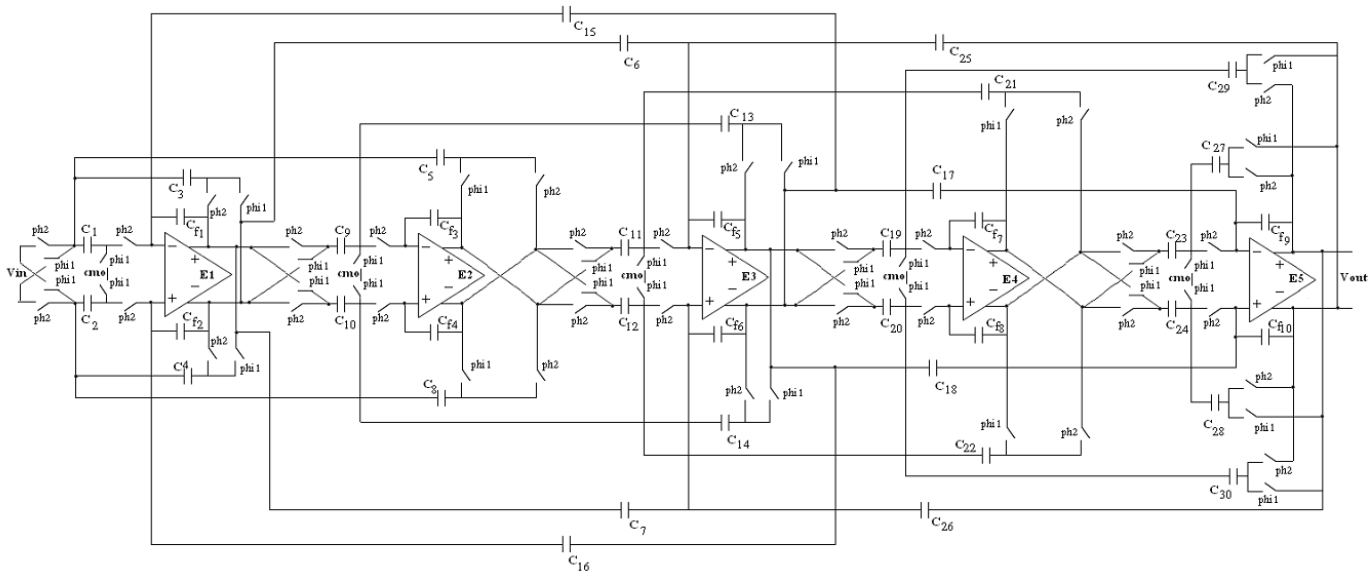

Figure 11. Complete schematic of fully differential switched capacitor ladder filter with bilinear implementation

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