

The 10GHz 4:1 MUX and 1:4 DEMUX implemented via the Gigahertz SiGe FPGA

Jong-Ru Guo*
Rensselaer Polytechnic Institute
110 8th St, Troy NY 12180
1-518-276-2513
guoj@rpi.edu

C. You*, P. F. Curran
Rensselaer Polytechnic Institute
110 8th St, Troy NY 12180

M.Chu, K.Zhou
Rensselaer Polytechnic Institute
110 8th St, Troy NY 12180

J. Diao, A. George
Rensselaer Polytechnic Institute
110 8th St, Troy NY 12180

R. P. Kraft
Rensselaer Polytechnic Institute
110 8th St, Troy NY 12180
1-518-276-2765
kraftr2@rpi.edu

J. F. McDonald
Rensselaer Polytechnic Institute
110 8th St, Troy NY 12180
1-518-276-2919
mcdonald@unix.cie.rpi.edu

ABSTRACT

This paper describes the implementation of a scalable SiGe FPGA that serves as a high speed FPGA test platform. A new configurable block (Basic Cell) has been evolved from the Xilinx 6200 specification, and is designed to perform in the gigahertz range. Two chips, a 4:1 multiplexer and 1:4 demultiplexer, were designed using the IBM SiGe 7HP process. The two designs can process 10 Gbps data streams.

Categories and Subject Descriptors

B.7.1D.3.3 [Integrated Circuit]: Types and Design Styles – *Advanced Technology, Gate Arrays, VLSI (Very Large Scale Integration).*

General Terms

Design

Keywords

FPGA, SiGe, 4:1 MUX, 1:4 DEMUX and 10 GHz.

1. INTRODUCTION

Field programmable gate arrays (FPGAs) are now widely used for the implementation of digital systems. They were first introduced by Xilinx Inc., San Jose, CA, and have demonstrated their versatility in many fields such as networking and digital signal processing (DSP). However, the relatively low operating frequency of CMOS FPGAs has limited the circuits and applications for which they can be used. Due to its excellent high-speed characteristics, Current Mode Logic (CML) is a good candidate for implementing an FPGA running at GHz frequencies. In 2000, the first high speed SiGe FPGA utilizing

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, or republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee.

GLSVLSI'04, April 26-28, 2004, Boston, Massachusetts, USA
Copyright 2004 ACM 1-58113-853-9/04/0004...\$5.00.

CML and running in the GHz range was proposed [1]. However, the large power consumption (71.4 mW) of its building block made it difficult to scale up. In order to alleviate this problem, a modified FPGA structure that has smaller propagation delay and power consumption was proposed in 2002 [2]. This paper mainly focuses on the performance of this FPGA, enhanced by the SiGe process and Current Mode Logic (CML). Sections 2 and 3 briefly describe the SiGe process and fundamental theory of CML. Section 4 describes the proposed FPGA configurable building block (or Basic Cell) and its performance. Measurement results of the first test chip are described in Section 5 and the 4:1 MUX and 1:4 DEMUX implemented by the proposed configurable building block are described also. Lastly, a conclusion is presented and future work is discussed.

2. IBM 120GHz SiGe process

Technical progress in bringing SiGe HBT technology to reality has been exceptionally rapid. The IBM SiGe BiCMOS process has evolved over several generations, resulting in the HBT's cutoff unity current gain frequency approaching 120 GHz (the process that the author used) and is still increasing; a 210 GHz process (8HP) was reported [3]. The excellent high frequency performance of the 120 GHz devices has been demonstrated most recently [4]. With outstanding high frequency characteristics and yield, SiGe logic circuits can be created that operate up to 40 GHz.

3. Current Mode Logic (CML)

Like ECL, CML is a differential logic design methodology that focuses on steering instead of switching currents. It has many similarities to ECL design, such as preventing the transistor from saturating and wide use of emitter coupled differential pairs. The advantages that make CML unique are that it does not require emitter followers at the gate outputs and it can be biased at lower

* Both authors have the equilibrium contribution

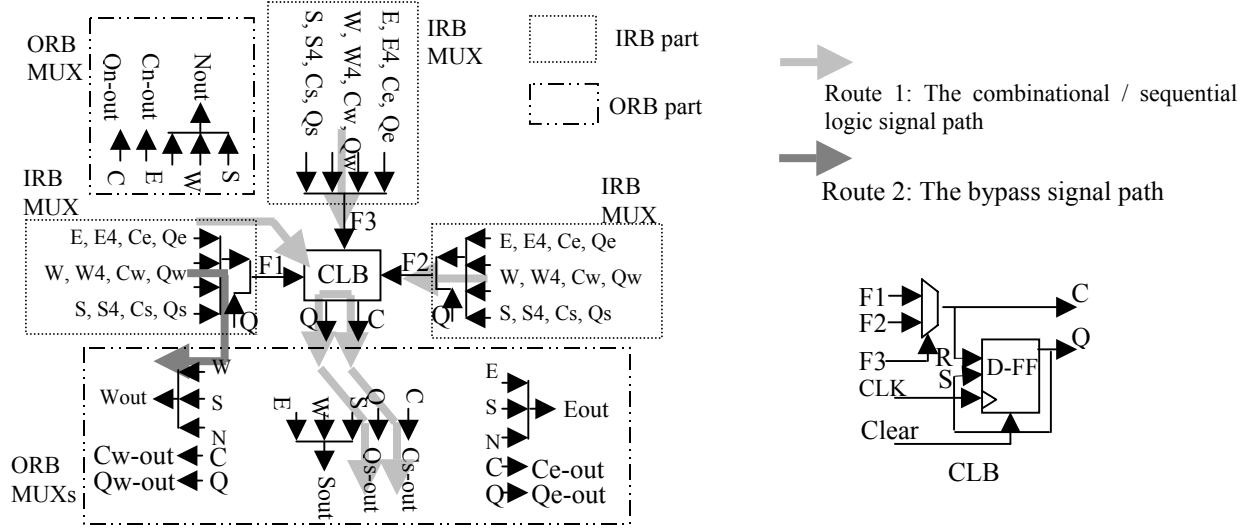


Figure 1. New Basic Cell (left) used in the SiGe FPGA and the CLB (right) in the Basic Cell

	Vcc, Vee	Current trees	Reference current	Power consumption/BC	Tp
Previous design ² [1]	0, -3.4V	30	0.7mA	71.4mW	130 ps (CLB only)
New design ² [2]	0, -2.5V	21	1mA	52.5mW	109 ps (BC)

Table 1. Comparison between the old SiGe FPGA and the new design used in this paper.

	Route	Propagation delay (ps)	Power consumption for the main functions	# of the enabled current trees (Total: 21 in BC)
Combinational logic	1	49ps	28mW	10
Sequential logic	1	109ps	33.6mW	12
Bypass signal	2	8ps	8.4mW	3

Table 2. Propagation delay and power consumption of the combinational logic, sequential logic and signal bypassed case. (AND function).

current levels without appreciably degrading its speed. The reference current is provided at the bottom of the current tree. By properly steering it flowing through the emitter coupled pair transistors and the voltage drop resistors, the desired output voltages are achieved.

4 Basic cell of the SiGe FPGA

Figure 1 shows the building block, or Basic Cell (BC), used in the FPGA core. The BC is composed of CML MUXs for fastest performance. This structure is the same with the one proposed in [2], having three parts: an input routing block (IRB), an output routing block (ORB), and a Configurable Logic Block (CLB). The structure used in this paper has better performance and less power consumption when compared to the first proposed SiGe FPGA. The relevant information is listed in Table 1. The Xilinx 6200 family is known for its limited functionality and other drawbacks, however its open design nature and relatively simple structure make it a good candidate for high speed FPGA testing and novel applications. The author has not precluded other new FPGA architectures. The incoming signals (X, X₄, Cx, Qx)¹ are

routed to the IRB which has three 8:1 MUXs (F1, F2 and F3). After multiplexing, the outputs are routed to the CLB to perform the desired logic function, which is then routed to the ORB (Cx-out², Qx-out², Eout, Wout, Sout and Nout). There are three main types of functions: combinational logic, sequential logic and bypass signals. Input signals of 5 GHz, 2.5 GHz and 1.25 GHz (to F1, F2 and F3) and a 10 GHz clock are fed to the CLB. The signal paths of the combinational/sequential logic and bypass signal are shown as Route 1 and 2 in Figure 5. The propagation delay and simulation results are summarize in Table 2, along with the power consumption of each case. The size of the BC layout is 166 x 162 μm². All connections emulate the structure of Xilinx 6200 so that all of the original functions are maintained.

5.1 Test circuit I: the BC ring oscillator

The first test circuit has been fabricated using the IBM 7HP process. The schematic of this test circuit is composed of four

¹ The x represents the directions that a signal can be routed to.

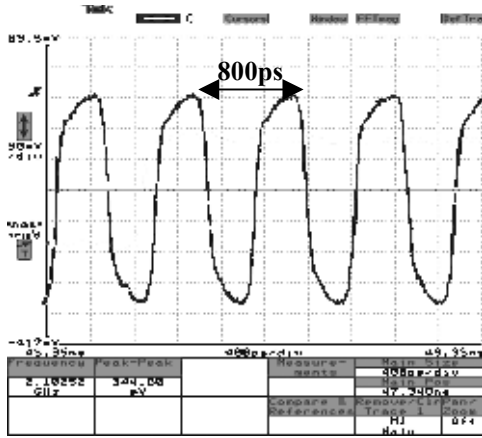


Figure 2. Measured waveform of the fabricated chip.

BCs. Since the differential configuration has been adopted, the first three BCs are programmed to buffers and the last one is programmed to inverter. The oscillator has been measured with the period of 800 ps shown in Figure 2, meaning the new BC has an operating frequency of up to 10 GHz (100 ps).

5.2 Test circuit II: The 4:1 multiplexer

Figure 3 shows the schematic of the 4:1 multiplexer (MUX), which is implemented by three MUX modules as shown in Figure 4. The input of all data streams (CH1 - CH4) are generated by a 2^4-1 pseudorandom bit sequence (PRBS). A 2.5 GHz clock source is connected to the PRBS to generate the desired random test pattern. The first two BC cells in the MUX module are configured to perform D-FF functions that align the timing of the

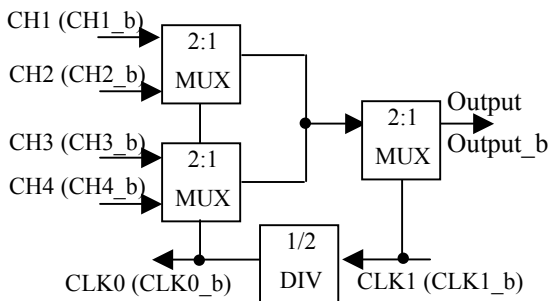


Figure 3. The block diagram of the 4:1 MUX

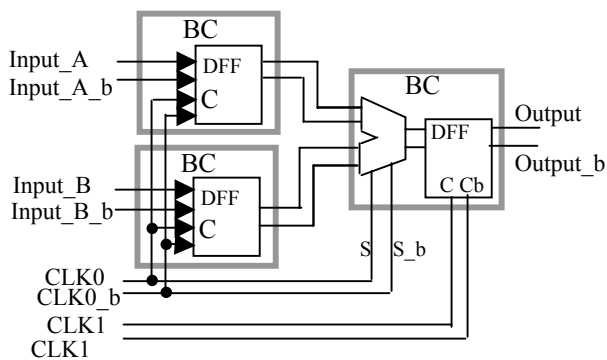


Figure 4. The schematic of the 2:1 MUX module

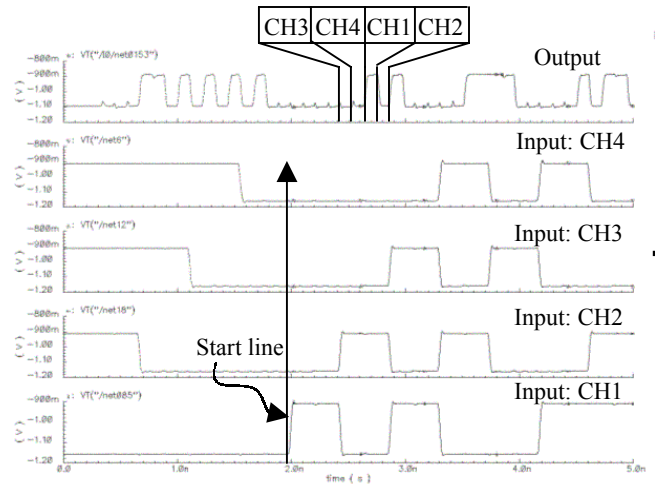


Figure 5. The simulation result of the 4:1 MUX

Inputs: CH1: 1 0 1 0 0 1 1 CH2: 0 0 1 0 1 0 0
 CH3: 0 1 0 1 0 0 1 CH4: 0 0 0 1 0 1 0
 MUX-output: 0010-1000-0011-1100-0001-0110

data streams to the select signal stage (CLK0). The right hand side BC cell is configured to be a multiplexer and D-FF to select different data streams and align timing again. When the select signal (S) is high (S_b is low), the multiplexer selects the Input_A data stream. When S goes low (S_b goes high), the multiplexer selects the Input_B stream. In order to align the timing of the multiplexed data streams, the clock connected to the top of the first stage MUX Module is inverted. Thus its output data stream can be offset by 90 degrees. Then, both outputs of the first stage modules are passed to the last module and multiplexed again. In the 4:1 MUX, the clock signals (CLK1 and CLK1_b) are twice as fast as the clock applied to the previous modules (CLK0 and CLK0_b). Seven BC cells are used to implement this 4:1 MUX. The simulation result of the 4:1 MUX is shown in Figure 5.

5.3 Test circuit III: 1:4 demultiplexer

The schematic of the 1:4 demultiplexer (DEMUX) is shown in Figure 6. The higher speed data stream is latched by the BC cell in the DEMUX module shown in Figure 7 to align with the applied clock. Then the high-speed stream is demultiplexed using

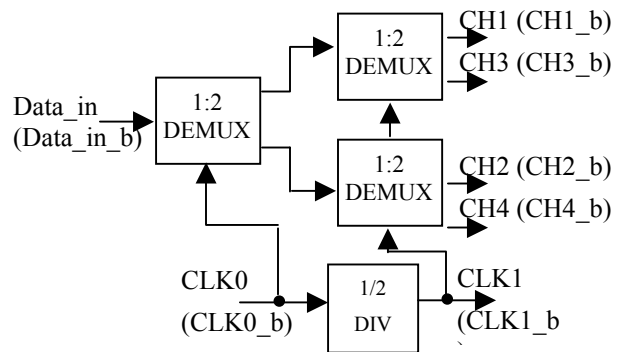


Figure 6. The building blocks of the 1:4 DEMUX.

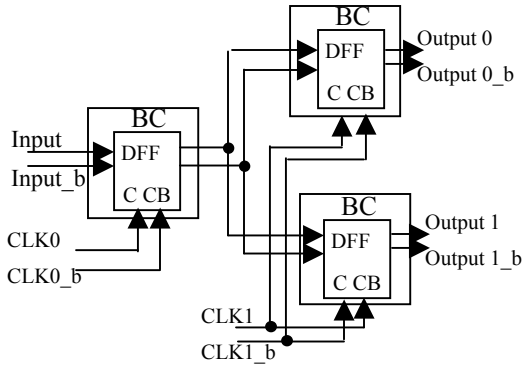


Figure 7. The schematic of the 1:4 DEMUX module

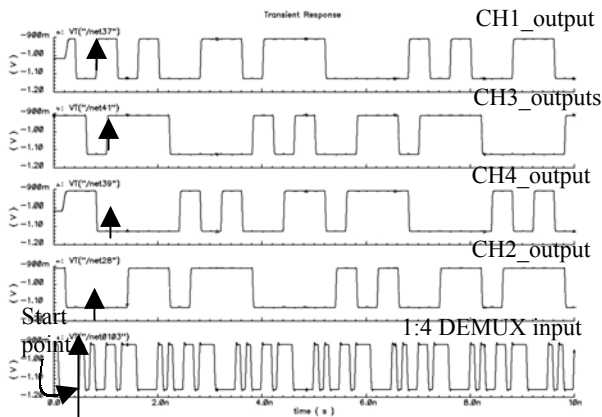


Figure 8. The simulation result of the 1:4 DEMUX.

DEMUX-input: 1010-0110-1110-0001-0100-1101-1100

Outputs: CH1: 1 0 1 0 0 1 1 CH2: 0 1 1 0 1 1 1

CH3: 1 1 1 0 0 0 0 CH4: 0 0 0 1 0 1 0

the rise and fall edges of the applied clock. After aligning two channels in the second stage, the data streams are then passed to a second DEMUX stage to further demultiplex the data streams. The input data stream is generated by the PBRS clocked by a 10 GHz clock for the input test signal. Figure 8 shows the simulation result of the 1:4 DEMUX.

6 Conclusions

The new Basic Cell (BC) has been demonstrated with an operating frequency up to 10 GHz. Also a 4:1 MUX and 1:4 DEMUX have been designed and fabricated to evaluate the performance of the new SiGe FPGA for a localized layout application. The layout of the 4:1 MUX and 1:4 DEMUX are shown in Figure 9 and 10. From the previously described simulation, both circuits can operate with data rates up to 10 GHz.

7. Future work:

The power consumption of the SiGe FPGA is still too high for larger arrays that are capable of supporting more sophisticated digital applications desired for future testing. The focus of the

continued research on the FPGA will be to investigate several methods for further power reduction as well as the realization of potential applications described in previous paragraphs. This will broaden the prospective application field of high-speed SiGe FPGAs.

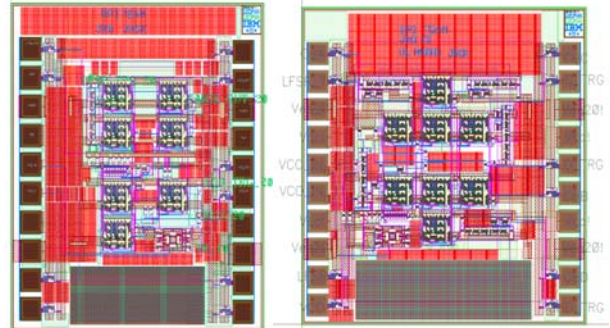


Figure 9. Left: The layout of the 4:1 MUX

Right: The layout of the 1:4 MUX

8. ACKNOWLEDGMENT

The authors would like to thank all the reviewers for their valuable comments. We also like to thank the sponsors for supporting this project.

REFERENCES

- [1] John F. McDonald and Bryan S. Goda, "Reconfigurable FPGA's in the 1-20GHz Bandwidth with HBT BiCMOS", Proceedings of the first NASA/ DoD Workshop on Evolvable Hardware, pp. 188-192.
- [2] J. R. Guo, C. You et al, "A Scalable 2V, 20GHz FPGA using SiGe HBT BiCMOS Technology", International Symposium on Field-Programmable Gate Arrays, 2003, pp.145~ pp.153.
- [3] Greg Freeman et al, "40 Gb/s Circuits Built from a 120 GHz ft SiGe Technology", IEEE Journal of Solid State Circuits, vol. 9. September, 2002, pp. 1106-1114.
- [4] John D. Cressler, "SiGE HBT Technology: A New Contender for Si-Based RF and Microwave Circuit Applications", IEEE Transactions on Microwave Theory and Techniques, VOL. 46, NO. 5, 1998.
- [5] G. Freeman et al, "40 Gb/s Circuits Built From a 120-GHz ft SiGe Technology" IEEE Journal of Solid-State Circuits, Vol. 37, NO. 9, 2002, pp1106-1114.
- [6] K. Ishii et al, "Low-Power 1:16DEMUX and One-Chip CDR With 1:4 DEMUX Using InP-InGaAs Heterojunction Bipolar Transistors", IEEE Journal of Solid-State Circuits, Vol. 37, NO. 9, 2002, pp1146-1151.
- [7] U. Nellore, et al, " Low-Power Fully Integrated 10 Gb/s SONET/SDH Transceiver in 0.13-um CMOS" IEEE Journal of Solid-State Circuits, Vol. 38, NO. 10, 2003, pp1595-1.