Simplified Delay Design Guidelines for On-Chip Global Interconnects

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ABSTRACT
Based on the effective attenuation constant approximation of distributed RLC lines, simplified design guidelines are presented dealing with the line characteristics, termination, and delay estimation of on-chip global interconnects. RC delay models are verified to be still accurate for a wide range of parameters conventionally considered inductive. A new closed-form RLC delay formula is developed when RC models are inadequate. The formula works for both voltage and current-mode signaling and exhibits 10% accuracy of SPICE simulation. This work is suitable for global routing topologies and iterative layout optimization.

Categories and Subject Descriptors
B.7.2 [**Integrated Circuits**]: Design Aids – Simulation.

General Terms
Algorithm, Performance and Design.

Keywords
Global interconnects, effective attenuation constant, delay, RLC, lossy transmission line, first incident switching.

1. INTRODUCTION
Signaling design for high performance VLSI systems has become an increasingly difficult task due to the propagation delay limitation over global interconnects. Unlike local or intermediate interconnects, global interconnects do not scale in length since they communicate signals across a chip [1]. Moreover, global interconnects are typically routed in top metal layers with large cross section to reduce resistance. With increases in signal frequency and signal edge rate, inductance is becoming an important consideration for on-chip signal integrity and timing analysis in global interconnects [2].

A number of criteria and design guidelines have been proposed or used to determine whether or not inductive effects are significant [2-4]. They essentially look at whether line attenuation constant is smaller than one and whether signal rise time is much smaller than line flight time. Although these guidelines are very helpful for using modeling and simulation techniques, they are not suitable for the flow of design and optimization tools because the bounds they give are blur and a large range of parameters are not clarified as suitable for either RC or RLC interconnects delay formula.

For the various closed-form analytical formulas of RLC interconnects, a formula based on first and second moments [5] or a formula based on the damping factor of a two-pole system [6] generally implies the same order of moment information, since the first 2q-1 moments can approximate the response of a lower q-pole model [7]. These formulas are able to include some extent of non-monotonic information as such they are more accurate than the first-moment-based Elmore Delay [8]. However, much higher orders of moments could be needed to model a transfer system with significant inductive effects, i.e. transmission line effects. Therefore, the formulas without moment order higher than two could only be accurate within a very limited range of parameters.

Another analytical formula models RLC interconnects as both RC distributive line and lossy transmission line and chooses the maximum value as the delay [9]. Unfortunately, this maximum criterion is not true all the time and it ignores the grey region which cannot be modeled by either RC or lossy transmission line model [10].

In this paper, the effective attenuation constant of distributive RLC lines is computed and used to derive the simplified delay design guidelines. The idea of effective attenuation constant was introduced in [6]. However, unlike their work, this second-moment-bound constant is not used for delay but only guideline derivation. In the inductive region according to the derived guidelines, a new closed-form delay formula is proposed based on first incident switching. This formula can be applied to both voltage and current-mode signaling design. In the RC region according to the guidelines, RC delay models are verified to be still accurate for RLC interconnects. Also, the guidelines are the first to classify the grey region which cannot be modeled by either RC or lossy transmission line model.

This paper is organized as follows. Section 2 reviews the categories of on-chip interconnects. Section 3 presents the effective attenuation constant. Section 4 provides the derivation of the first incident switching delay model and maximum length

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guideline. The simulation and verification results are shown in section 5, with the conclusion in section 6.

2. CATEGORIES OF ON-CHIP INTERCONNECTS

Modern technologies optimize their metal layers for three different tasks, lowest level metals for local interconnections; midlevel metals typically for functional unit connection; top layer metals for global signaling and power distribution. One good categorization work [2] divides on-chip interconnects into three categories, short, medium and long lines. Even though short and medium lines with very low resistance and very large drivers will also behave inductively, the very high integration density desired on large chip limits the wiring dimensions and driver sizes for these lines. Hence, short and medium lines can still be represented by RC circuits, and the inductance problem is simplified to determine whether or not inductive effects are important on long global lines.

3. EFFECTIVE ATTENUATION CONSTANT

For the RLC interconnect line shown in Figure 1, its transfer function can be written as [11],

$$H(S)=\frac{V_2(S)}{V_1(S)}=\frac{1}{\left[\cosh(\theta h)+\frac{Z_S}{Z_o}\sinh(\theta h)\right]+\frac{1}{Z_L}\left[Z_0\sinh(\theta h)+Z_S\cosh(\theta h)\right]} \tag{1}$$

where $Z_S = R_S$ and $Z_L = \frac{R_L}{1+R_L C_L S}$ are the source and load impedance, h is the line length, $\theta = \sqrt{(R_0+SL_0)SC_0}$ is the propagation constant, and $Z_0 = \sqrt{(R_0+SL_0)/SC_0}$ is the characteristic impedance with R_0, L_0, and C_0 as the distributed line parameters.

This transfer function can be approximated as a two-pole system by expanding cosh and sinh,

$$H(S)\approx\frac{m_0}{1+sb_1+s^2b_2} \tag{2}$$

where $b_1 = a_1m_0$, $b_2 = a_2m_0$, and m_0 serves as the zero moment and indicates the system DC gain,

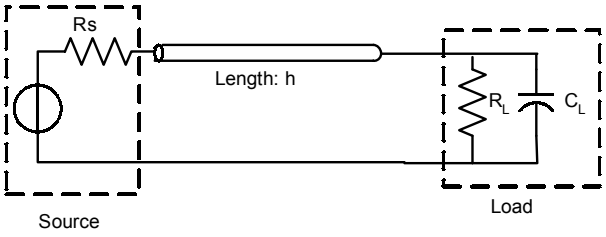


Figure 1. RLC interconnect line with source and load impedance.

$$m_0=\frac{R_L}{R_S+R_T+R_L} \tag{3}$$

$$a_1=R_S(C_T+C_L)+\frac{R_TC_T}{2}+R_TC_L+\frac{R_SR_TC_T+2L_T}{2R_L} \tag{4}$$

$$a_2=\frac{1}{6}R_SR_T^2C_T^2+\frac{1}{2}R_SR_TC_TC_L+\frac{(R_TC_T)^2}{24}+\frac{1}{6}R_T^2C_TC_L+\frac{L_TC_T}{2}+L_TC_L+\frac{\frac{1}{3}R_TL_TC_T+\frac{1}{120}R_T^3C_T^2+\frac{1}{24}R_SR_T^2C_T^2+\frac{1}{2}R_SL_TC_T}{R_L} \tag{5}$$

with $R_T = R_0h$, $C_T = C_0h$, and $L_T = L_0h$ as the line resistance, capacitance and inductance.

The transfer function of a two-pole system can also be expressed as,

$$H(S)=\frac{m_0}{\frac{S^2}{\omega_n^2}+\frac{2\xi_{eff}S}{\omega_n}+1} \tag{6}$$

From (2) and (6),

$$\omega_n=\frac{1}{\sqrt{b_2}} \tag{7}$$

$$\xi_{eff}=2\frac{b_1}{\sqrt{b_2}} \tag{8}$$

By analogy with line attenuation constant $\xi = \frac{Z_0}{2R_0h}$, ξ_{eff} is called as the effective attenuation constant and used as the criterion to determine whether inductance effects are significant. By doing this, the interconnect line and the termination impedance are treated as a whole system. $\xi_{eff} \geq 1$ indicates a RC region and RC delay models [12, 13] are still adequate, while $\xi_{eff} < 1$ indicates a RLC region and RLC delay model is required.

4. MODELING IN RLC REGION

4.1 First Incident Switching Delay Model

In RLC regions, lossy transmission line models become more adequate than distributed RC line models. Since most transmission line analysis is performed in frequency domain, an inverse Laplace transform could be very computation expensive when a transmission line analysis has to span a time interval of several transient times. In this work, instead of deriving a lossy transmission line delay model in frequency domain, a first incident switching delay model is directly obtained in time domain.

The smallest propagation delay on a transmission line is obtained if the first signal arriving at the end of the transmission line has sufficient magnitude to switch the gate. Otherwise, at least one extra round trip time will be needed. For this reason, the closed-form formula in RLC regions is derived based on first incident switching to achieve minimum delay.

A transmission line can be modeled at various points along the line by using circuit models [10]. Similarly, we model a lossy transmission line at points I, X and L shown in Figure 2. For modeling point I,

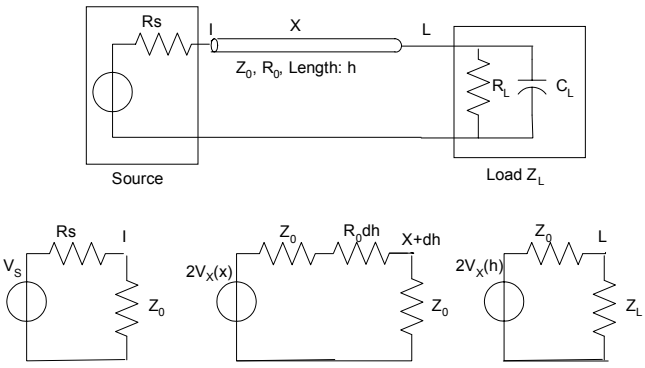


Figure 2. Circuit model for a lossy transmission line.

$$V_i(0) = \frac{Z_0}{Z_0 + R_S} V_S \tag{9}$$

where V_S is the normalized step input voltage and $Z_0 \approx \sqrt{L_0 / C_0}$.

For modeling point X, the voltage at point X + dh would be,

$$V_X(X + dh) = \frac{Z_0}{2Z_0 + R_0 dh} 2V_X(X) \tag{10}$$

When the signal reaches the end of the line, the voltage value can be integrated as,

$$V_X(h) = e^{-R_0 h / 2Z_0} V_i(0) \tag{11}$$

Considering the load capacitance C_L, we assume the initial voltage of the first incident switching at modeling point L is zero and the final voltage is the division of two resistors,

$$V_L = \frac{R_L}{R_L + Z_0} 2V_X(h) \tag{12}$$

Hence, the signal waveform at the load end for the first incident switching can be approximated as,

$$V_{out}(t) = V_L(1 - e^{-t/\tau}) \tag{13}$$

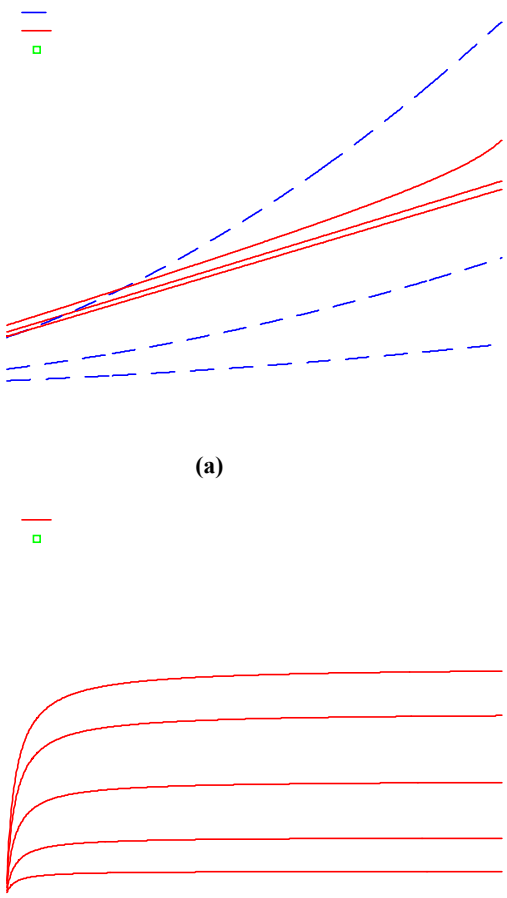
$$\tau = \frac{Z_0 R_L}{Z_0 + R_L} C_L \tag{14}$$

The rise time for the first incident switching waveform is then derived as,

$$t_{FIS} = -\frac{Z_0 R_L}{(Z_0 + R_L) C_L} \ln\left(1 - \frac{vm_0}{\frac{Z_0}{Z_0 + R_S}\frac{R_L}{R_L + Z_0} 2e^{-R_0 h / 2Z_0}}\right) \tag{15}$$

If delay t_v is defined as the time from (t=0) to the time when the normalized voltage reaches threshold v at the end of the line, and $t_f = \sqrt{L_0 C_0 h^2}$ is defined as the line flight time, the final closed-form delay formula is obtained as,

$$t_v = t_f + t_{FIS} \tag{16}$$



(a)

(b)

Figure 3. First incident switching delay model compared to SPICE, (a) delay vs. length at different v, (b) delay vs. R_L at different C_L.

Figure 3(a) compares this first incident switching delay model with SPICE simulation. The results converge very well at different threshold v along the length, while RC model [12] is clearly inadequate. Unlike RC lines, the propagation delay of RLC lines does not change rapidly against the threshold. Figure 3(b) shows the delay change versus load termination R_L and C_L. It is within 10% accuracy of SPICE simulation for a large range of termination change.

4.2 Maximum Length Guideline

Due to the slow RC rise time at 90% - 100% of the final voltage, it will largely increase the propagation delay if the desired output voltage is designed in this region. Therefore, we have

$$V_{out} \le 0.9 V_L \tag{17}$$

Combined with (10-12),

$$h \le \frac{2Z_0}{R_0} \ln \frac{1.8 R_L Z_0}{vm_0 (R_L + Z_0)(R_S + Z_0)} \tag{18}$$

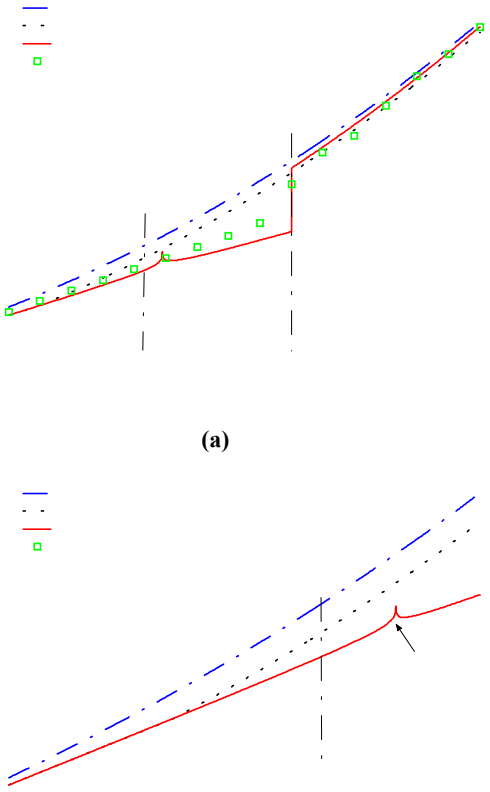
This equation gives the guideline of the maximum usable length for a lossy transmission line if first incident switching is targeted. It consequently avoids the grey region which cannot be modeled by either RC or lossy transmission line model. More discussion on the grey region can be found in section 5, guideline verification.

5. Guideline Verification

The effective attenuation constant guideline (8) and the maximum length guideline (18) indicate the RLC, grey, and RC regions in Figure 4(a), and the RLC and grey regions in Figure 4(b). We use the proposed first incident switching model (16) for RLC region and the RC model [12] for RC region. The results present very good convergence with SPICE simulation in both regions. RC models are found to be still valid on a long inductive line as long as the effective attenuation constant indicates it is in RC region.

The maximum length guideline constrains the failing point of first incident switching in the grey region. Since the failing point determines if one extra round trip time is needed, deviation of line or termination parameters in this region could change propagation delay with a leap as such it causes more severe problems on timing estimation. Hence, although the delay formula in grey region is still theoretically derivable by using inverse Laplace transform or convolution method, the maximum length guideline suggests avoiding to design in this region.

To verify the guidelines proposed in (8) and (18), modeling expectation and SPICE simulation are compared in the range of 5 mm $\le h \le$ 20 mm, 0 Ω $\le R_L \le \infty$, 0 $\le C_L \le$ 1 pF, 0 $\le R_S \le Z_0$, 0 $\le R_0 \le$ 100 Ω.



(a)

(b)

Figure 4. Design guidelines compared to SPICE, (a) RLC, grey and RC regions, (b) RLC and grey regions.

6. CONCLUSIONS

In this paper, simplified design guidelines are presented to optimize line characteristics and termination for the delay design of on-chip global interconnects. RC delay models are verified to be still accurate for a wide range of parameters conventionally considered inductive. A new closed-form RLC delay formula is developed by using first incident switching model. The formula works for both voltage and current-mode signaling and exhibits 10% accuracy of SPICE simulation.

7. ACKNOWLEDGMENTS

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