Reliability-Driven Layout Decompaction for Electromigration Failure Avoidance in Complex Mixed-Signal IC Designs *

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ABSTRACT

The negative effect of electromigration on signal and power line lifetime and functional reliability is an increasingly important problem for the physical design of integrated circuits. We present a new approach that addresses this electromigration issue by considering current density and inhomogeneous current-flow within arbitrarily shaped metallization patterns during physical design. Our proposed methodology is based on a post-route modification of critical layout structures that utilizes current-density data from a previously performed current-density verification. It is especially tailored to overcome the lack of current-flow consideration within existing routing tools. We also present experimental results obtained after successfully integrating our methodology into a commercial IC design flow.

Categories and Subject Descriptors

B7.2 [**Integrated Circuits**]: Design Aids

General Terms

Algorithms, Design, Reliability

Keywords

Physical design, electromigration, interconnect reliability, layout decomposition, compaction, decompaction

1. INTRODUCTION

The damage of interconnect wires and vias due to electromigration is one of the most aggravating reliability problems to cope with in physical design for sub-micron IC metallization patterns. The electromigration failure effect within solid conductors is primarily caused by excessive current-density stress combined with high operating temperatures, large temperature gradients, mechanical stress and a process- and layout-dependent distribution of material transport paths [11, 12]. The flow of electrons interacts with the lattice of the conductor material, thereby removing metal atoms from their lattice positions and driving them into the direction of the current-flow. This causes the creation of material voids as well as hillocks and whiskers, resulting in either a slow drift of circuit parameters, an open circuit or even a short with neighboring wires.

In 1969 Black [2] formulated an empirical relation between mean-time-to-failure and current density, temperature as well as process- and material-dependent properties ("Black's Law"). The mean-time-to-failure also depends on the current wave form as reported in [7, 8]. Our proposed methodology focuses on current density as the driving design constraint for electromigration failure avoidance.

There exist three approaches to address the problem of designing reliable interconnect systems with regard to electromigration. Firstly, while using standard routing tools, a critical net is assigned to an "assumed save" net class. However, this most likely creates a high percentage of over-designed (i.e., route space wasting) net segments without any guarantee of current-density correctness. Secondly, the routing is performed with a current-flow-aware and hence current-density-driven wire planning and routing tool (e.g., [1, 6]). Here, one of the problems is the determination of *segment*-specific current data *prior* to routing.

A third approach introduced in this paper performs a *post*-route cross-section area adjustment of critical interconnect structures within tree-based nets. It utilizes layout-based current-density data for correct wire and via (array) sizing by using any available current-density calculation tool (e.g., [3, 10]). In contrast to published solutions for post-route layout modification of power and ground nets (e.g., [13]), our approach is not restricted to single-layer manhattan-style layouts and, hence, it is applicable to any type of nets, including analog and digital signal nets.

2. OVERVIEW

The design flow of our approach is depicted in Fig. 1. After floorplanning, placement and routing, a verification of current densities is performed in order to identify regions with excessive current-density stress [3]. The terminal current values required for a current-density calculation are obtained from a prior simulation of analog- and mixed-signal circuits or a current estimation within digital circuits [3, 6, 10]. Based on these provided current data, our methodology utilizes a newly introduced design stage – the current-density-driven layout decompaction.

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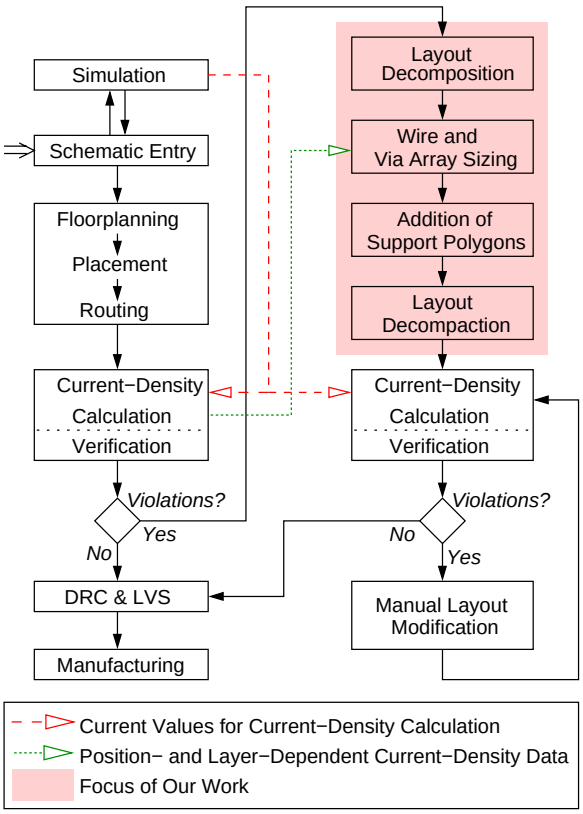

Figure 1: Design flow.

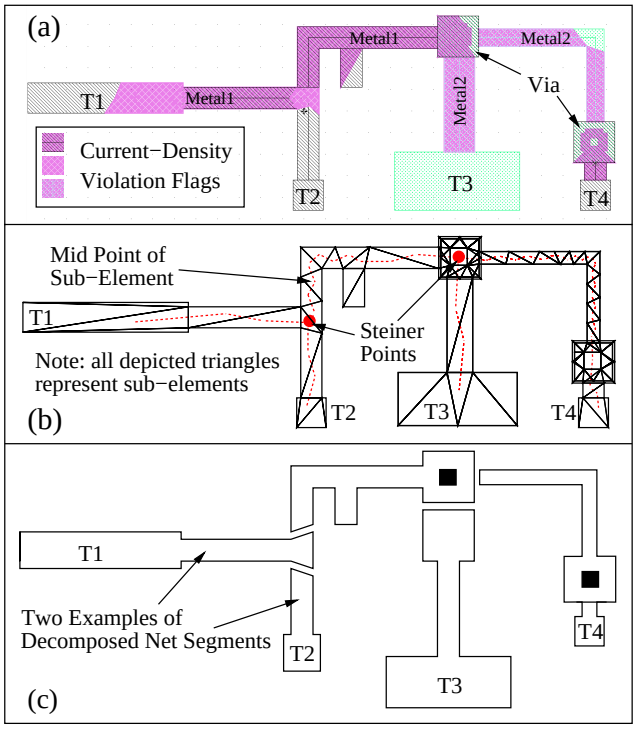

Figure 2: Two layer net layout with four terminals (T1–T4) and visualized current-density violation flags (a). Sub-element creation (b) is done by layout triangulation utilizing Alg. 1 followed by a tree branch extraction and Steiner point determination. The resulting net segments are depicted in Fig. (c).

During layout decomposition (Section 3.1), all segments of a net are identified based on the net topology. A net segment contains only *one* current-source and *one* current-sink, thus it can be treated independently from all other net segments. Therefore, the calculation of the current-density-correct cross-section area of all excessively stressed and hence critical wires and via (arrays) is performed using only *one* worst case current value derived from the supplied current-density data (Section 3.2).

So called "support polygons" are added to critical net terminals and corner layout sections to reduce local current-density stress and to improve the homogeneity of the current-flow (Section 3.3).

The final layout decompaction (Section 3.4) is performed utilizing an appropriate decompaction tool (e.g., [5]). Thereby, all layout structures are subject to decompaction in order to accommodate their previously assigned geometrical decompaction dimensions. In case there are remaining current-density violations, a manual layout modification is applied.

3. DECOMPACTION APPROACH

3.1 Layout Decomposition

Several polygon decomposition algorithms have been published in the literature [4, 9]. These decomposition algorithms require additional guidance points within polygons to mark layout Steiner points. They are also limited to only one routing layer. Our proposed algorithm does not have these limitations (Alg. 1, Fig. 2).

At first, basic layout-based net connectivity information is obtained (Alg. 1, lines 1–2). The layout is dissected afterwards into smaller pieces (so called "sub-elements") using a coarse mesh triangulation of metallization polygon surface points (line 4). All sub-element neighbors are then connected with each other to create a mid-point mesh (lines 5–7). All loops within the mid-point mesh are removed in order to enable a Steiner point detection (lines 8–10). Mid-point connections within net terminals and vias are then reduced to only one commonly shared mid-point (lines 11–15).

Afterwards, net branches not ending in either a via (array) or a net terminal are pruned (line 16). Single- and multi-layer Steiner points are retrieved by a detection of mid-point connections with more than two connecting neighbors [lines 17–18, Fig. 2(b)]. Finally, given the tree of mid-point connecting sub-element neighbors and the previously extracted connectivity information, all net segments can then be obtained easily [line 20, Fig. 2(c)].

3.2 Wire and Via Array Sizing

With a predefined interconnect lifetime and design temperature (i.e., actual working temperature of the chip) T, a net segment is current-density-critical if it contains one or more wires or via (arrays) with a local current density $j_{wire/via}$ fulfilling either

$$j_{wire/via} > j_{max,eq}(T) \tag{1}$$

or

$$j_{wire/via} > j_{max,peak}(T)\ . \tag{2}$$

The terms $j_{max,eq}(T)$ and $j_{max,peak}(T)$ represent the temperature-dependent maximum permissible current density for an equivalent/peak current at design temperature T [8].

The worst case segment current $i_{s,eq/peak}$ used for sizing of critical wires and via (arrays) is derived from a hole- and loop-free segment and from the type of supplied current-density data such as equivalent or peak current density. Hence, $i_{s,eq/peak}$ either represents a worst case equivalent current $i_{s,eq}$ or a worst case peak

Algorithm 1 Algorithm for Net Layout Decomposition

Input: – Set of net metallization polygons S_{Met}.
– Set of single via polygons S_{Via}.
– Location and outline of all net terminals.
Output: – Decomposed net segments.

1: Extract connectivity information from S_{Met} and S_{Via}.
2: Determine via (arrays) from net connectivity information and via polygons in S_{Via}.
3: **for** all metallization polygons $i \in S_{Met}$ **do**
4: Create sub-elements j by coarse mesh triangulation.
5: **for** all created sub-elements j in i **do**
6: Determine the geometrical mid-point of j and connect it with all mid-points of edge sharing neighbors.
7: **end for**
8: **if** mid-point connections create loops **then**
9: Break all loops by removing one mid-point connection within each loop.
10: **end if**
11: Retrieve sub-elements within via (arrays) and net terminals.
12: **for** sub-elements j assigned to either via (array) k or net terminal k **do**
13: Reduce mid-point connections within k to only one commonly shared mid point P_{shared}.
14: Re-connect all outgoing mid-point connections of k to P_{shared}.
15: **end for**
16: Prune all mid-point connection paths not ending in either a via (array) or a net terminal.
17: Retrieve all single-layer Steiner points SP_{SL} [SP_{SL} = mid-points with more than two neighbors].
18: Retrieve all multi-layer Steiner points SP_{ML} [SP_{ML} = Steiner point created by via (array)].
19: **end for**
20: Retrieve all net segments n considering all SP and using extracted net connectivity information.

current $i_{s,peak}$. For a given current-density progression function $j_{wire}(w)$ derived from the provided current-density data, $i_{s,eq/peak}$ is determined using wire width w_s, and the nominal layer height h_{nom}:

$$i_{s,eq/peak} = h_{nom} \cdot \int_{w=0}^{w=w_s} j_{wire}(w) \cdot dw \; . \tag{3}$$

The nominal wire width $w_{nom}(T_{ref})$ is determined under consideration of h_{nom}, and the provided process-dependent terms reference temperature T_{ref} and minimum layer-dependent wire width $w_{min,process}$:

$$w_{nom}(T_{ref}) = \max \begin{cases} w_{min,process} \; , \\ \frac{i_{s,eq}}{j_{max,eq}(T_{ref}) \cdot h_{nom}} \; , \\ \frac{i_{s,peak}}{j_{max,peak}(T_{ref}) \cdot h_{nom}} \; . \end{cases} \tag{4}$$

The determination of the design-temperature-dependent target wire width $w(T)$ used for later decompaction of a critical wire must also consider process-dependent variations of minimum layer height h_{min} and wire width Δw as well as a temperature scaling factor $f(T)$ considering the case $T \neq T_{ref}$, and an etch loss w_{etch}:

$$w(T) = \left(w_{nom}(T_{ref}) \cdot \frac{h_{nom}}{h_{min}} + \Delta w \right) \cdot f(T) + w_{etch} \; . \tag{5}$$

If $T \neq T_{ref}$, a temperature scaling of j in Black's Law [2] is required in order to ensure equal interconnect lifetimes for different design temperatures [2, 11]. Based on Black's Law, a temperature scaling factor $f(T)$ is determined by

$$f(T) = \exp\left(-\frac{E_a}{n \cdot k \cdot T_{ref}} \cdot \left(1 - \frac{T_{ref}}{T} \right) \right) \; , \tag{6}$$

with E_a = activation energy for the electromigration failure process, n = 2 according to [2], and k = Boltzmann constant.

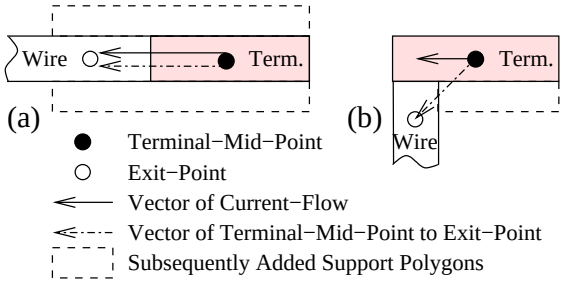

Figure 3: Locations and outlines of added support polygons at net terminals. If the vector of current-flow and the vector of terminal-mid-point to exit-point are parallel, then two support polygons are created (a) otherwise only one support polygon is added (b).

After the determination and assignment of correct wire widths for decompaction, all current-density-critical vias must be adjusted as well in order to meet the current-density constraints. A via (array) is considered to be current-density-critical if it contains at least one single via that encounters excessive current-density stress according to Eqs. (1) and (2). The temperature-dependent number of single vias $n_{via}(T)$ required within a via (array) is determined by

$$n_{via}(T) = \text{ceil}\left(\frac{i_{via\,array}}{i_{single\,via}} \cdot f(T) \cdot g(H) \right) \; , \tag{7}$$

where $i_{via\,array}$ represents the worst case current value the via (array) must carry reliably, $i_{single\,via}$ the current-density-correct current value of a single via, and $f(T)$ of Eq. (6). The term $g(H)$ accounts for inhomogeneous current-flow within the via array and is set to $g(H) = (1.0 - 1.2)$ in case of an "assumed" homogeneous current-flow within the critical via array (e.g., straight connecting wires with a wire width equal to via array width). For wires with a wire width not equal to via array width and for orthogonal connecting wires, $g(H)$ is set to $g(H) = (1.2 - 1.8)$ as determined by our FEM simulations.

3.3 Addition of Support Polygons

Support polygons are added to critical net terminals (triangle and rectangle polygons) and at all critical orthogonal layout corners (triangle polygons) to reduce local current-density stress (Figs. 3, 4).

Depending on the position of the net terminal connecting wire, either one or two support polygons are created and added. The current-flow vector obtained from the given current-density data and the position of the connecting wire are both used to determine whether one or two support polygons are required. Two polygons are added if the current-flow vector and the terminal-mid-point to exit-point vector are parallel [Fig. 3(a)]. Otherwise, only one polygon is added at the edge towards the attached wire [Fig. 3(b)].

3.4 Layout Decompaction

Prior to the final decompaction step, the relative positions of all segment-connecting Steiner points are fixated in order to preserve the net topology during the subsequent layout modification step. This is required to ensure the validity of i_{eq} and i_{peak} in Eq. (4).

The final layout decompaction with cross-section area adjustment can be performed with any decompaction tool capable of (1) simultaneous compaction *and* decompaction of layout structures such as wires, polygons and via (arrays), (2) preserving the net topology during layout compaction and decompaction, and (3) considering additional design constraints (such as matching or timing constraints). The final result of the current-density-correct layout decompaction of the example in Fig. 2(a) is depicted in Fig. 4.

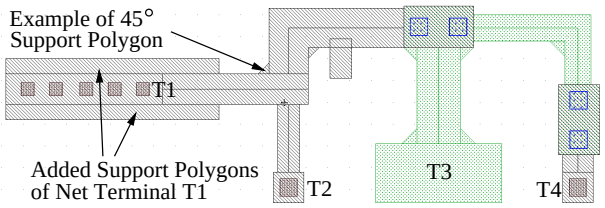

Figure 4: Final layout result from Fig. 2(a) after wire and via sizing and subsequent decompaction. Two support polygons were added at net terminal T1. Several 45° support polygons were inserted at critical layout corners to reduce local current-density stress.

4. RESULTS

The described algorithms were implemented in about 20,000 lines of C++ and vendor specific code for a commercial IC design framework. The commercial layout compaction tool Cambio-XT [5] was used for layout decompaction. The current-density data was gained from a current-density calculation tool published in [3].

Due to the lack of standard benchmarks, all conducted tests used several analog- and mixed-signal cell layouts from two commercial chip designs of different process technologies. The cells contained an adequate range of regular and highly specialized nets such as ESD protection nets, power and ground nets as well as analog end-stage circuitry (Table 1).

The results gained after the application of our proposed methodology are depicted in Table 2. The number of current-density violations dropped down dramatically for all cells. Violations within net terminals and corners were eliminated in most cases after adding support polygons. The few remaining violations within via (arrays) and wire segments were observed in layout regions with a high degree of inhomogeneous current-flow. They were all eliminated by manual layout modifications.

In Table 2, the decompaction of interconnect structures resulted in an increase of *net* area (i.e., wire and via area) of all considered cells. Specifically, the net area increase of cell G was caused by nets with "inappropriate topologies" created by a current-flow-unaware routing tool. The required insertion of support polygons at net terminals and critical layout corners contributed with about $(8-21)\%$ to the overall net area increase. The *cell* area of cells C, E and F remained constant due to spacious bipolar devices.

With regards to the limitations of our approach, our solution primarily focuses on the fulfillment of current-density constraints. The fulfillment of other (i.e., process-dependent) design constraints has to be maintained by the used layout compaction tool.

Any change of the net topology after a performed current-density calculation would cause the current-density data used in Eq. (3) to become invalid. Hence, the net topology has to be preserved during layout decompaction.

The layout of net terminals cannot be decompacted due to the fixed layout of devices. This type of current-density violation requires a manual modification or an exchange of the affected device.

				Before Layout Decompaction				
	No.	No.	No.	Violation Flags			Area [AU]	
Cell	Dev.	Nets	Poly.	T	V	W	Cell	Net
A	26	6	1,267	0	11	9	18.4	21.4
B	39	8	3,967	4	9	48	6.7	5.1
C	56	11	1,963	2	7	26	30.2	34.7
D	94	20	4,689	2	8	12	19.4	13.1
E	121	24	4,716	3	34	42	73.1	48.7
F	156	45	6,174	3	28	56	80.9	94.6
G	197	29	85,705	9	45	89	179.3	406.2
H	330	42	21,344	4	5	11	97.3	87.8

Table 1: Summary of used test cells (Current-Density Violation Flags: T = terminal, V = via, W = wire, Area: AU = area units).

				After Layout Decompaction				
	Run Time [sec.]			Violation Flags			Area [AU]	
Cell	PO	WS	PA	T	V	W	Cell	Net
A	0.1	0.1	8.1	0	0	1	19.1	25.3
B	0.3	0.1	115.1	0	0	0	7.2	6.4
C	0.2	0.1	28.2	0	1	0	30.2	36.1
D	0.8	0.1	189.6	0	2	1	22.1	16.3
E	0.7	0.1	97.7	1	2	1	73.1	48.7
F	2.4	0.3	214.7	0	1	1	80.9	102.4
G	15.1	0.4	1,670.2	1	8	3	192.2	489.3
H	3.2	0.2	528.9	0	1	1	101.4	92.9

Table 2: Experimental results using a Sun Fire 280R (Time: PO = layout decomposition, WS = wire/via sizing and support polygon addition, PA = layout decompaction, Current-Density Violation Flags: T = terminal, V = via, W = wire, Area: AU = area units).

5. ACKNOWLEDGMENTS

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