Design and Reliability Challenges in Nanometer Technologies

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ABSTRACT

CMOS technology scaling is causing the channel lengths to be sub-wavelength of light. Parameter variation, caused by sub-wavelength lithography, will pose a major challenge for design and reliability of future high performance microprocessors in nanometer technologies. In this paper, we present the impact of these variations on processor functionality, predictability and reliability. We propose design and CAD solutions for variation tolerance. We conclude this paper with soft error rate scaling trends and soft error tolerant circuits for reliability enhancement.

Categories and Subject Descriptors

B.8.1 [**Performance and Reliability**]: reliability, testing and fault-tolerance.

General Terms

Circuits, Variability, Reliability, SEU, SER.

Keywords

Low-power, variation tolerance, leakage tolerance, reliability, soft errors.

1. INTRODUCTION

CMOS technology scaling is causing the channel lengths to be sub-wavelength of light. Sub-wavelength lithography will worsen the parameter variation problem [1, 2]. It will be hard to control 3σ of the critical dimensions within 10%. In this paper, we describe the variation problem and its effect on functionality, predictability and reliability.

Process variations are present within die as well as die to die. Variable device parameters – mainly drive current and subthreshold leakage current – are the major outcomes of process variation. These variations have systematic as well as random components. We present within die variation scaling trends of both types of components. These variations are static – they do not change over time. However, there is also a gradual degradation of device performance over the life span of a product due to stress.

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The impact of variations will lead to functional failures in a microprocessor. As technology scales, several billion transistors may be available on one chip, but as much as 10% of those may have $>6\sigma$ critical dimension variance. Therefore, SRAM cell stability will be a serious design challenge. Multiple SRAM bit failures due to parameter variations may cause functional failures. Future logic circuits may have their own failures also. Fully depleted SOI technologies, in any form, are introduced to reduce sub-threshold leakage, but they will incur the cost of increased variability.

Variations are adversely affecting the reliability of prediction. We present the impact of reduced pipeline depths and increased number of critical paths on the reliability of frequency prediction. Multi-V_t, multi-L_e or multi-T_{ox} technologies offer design parameters to maximize performance for minimum total power. However, they increase the number of critical paths by an order of magnitude, which causes an effective lower mean frequency. Optimal sizing to maximize target frequency and lower power has a reverse effect on achieved mean frequency.

We propose solutions to reduce the impact of parameter variations and to achieve higher frequency bins. Freelance design and layout styles will be history; you will have to follow strict rules of device widths, interconnect pitches, lengths, spacings, etc. These dimensions will change from continuous to discrete. There may be a need for uniform layout styles, such as sea of gates or sea of transistors. There is a need for probabilistic or statistical design flows and tools. The design and CAD techniques need to work with bounded windows of performance and power. EDA community should have a serious focus on variation-tolerant libraries for synthesis and variability-driven tools.

Soft error tolerance will remain a reliability challenge in the future microprocessor systems. Critical charge per node will reduce and the number of nodes per chip will increase with technology scaling. We conclude the paper by presenting our measured scaling trends in memories and sequential logic blocks. Supply voltages for on-chip memories will have a lower limit imposed by system soft error rate specification. We propose some design techniques that achieve significant soft error tolerance with no performance penalty and minimal power penalty.

2. REFERENCES

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