

SPICE Compatible Circuit Models for Partial Reluctance K

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Abstract— We are the first to develop SPICE compatible circuit model for partial reluctance K. It can be combined with any partial reluctance based extraction method to perform RLC simulation directly without the need of inverting partial reluctance matrix back into partial inductance domain or modifying conventional simulator.

To build symmetrical partial reluctance matrix, we also proposed blocked K method based on group concept to cover more magnetic couplings. Both quantitative analysis and experiments demonstrated that the combination of the SPICE compatible circuit model and the blocked K method has the best compromise between accuracy and performance among all SPICE compatible sparsification techniques.

I. INTRODUCTION

With the advance of modern IC technology, the interconnect delay and crosstalk have become bottlenecks in chip performance. It is critical to model interconnect parasitics more accurately for chip signal integrity sign-off. For $0.13\mu\text{m}$ technology and below, the previously prevailing RC model for on-chip interconnects is not accurate enough. The impedance of interconnects is composed of two parts: resistance part R , and inductance part ωL . As the clock frequency increases, the inductance part increases almost linearly with respect to frequency. Meanwhile, the resistance part is reduced due to the adoption of copper technology and the use of wider and thicker interconnects as global wires. Therefore, the inductance effects becomes more and more significant.

However, inductance extraction is difficult due to unknown current return path. Although partial inductance concept [1, 2] can avoid the return path issue, it introduces huge full partial inductance matrices for large complex IC circuits which are impracticable to solve for downstream simulators. shift-truncation method was proposed by Krauter, *et al* [3, 4] to sparsify the partial inductance matrix while preserving circuit stability. However, it need to pick the shell radius large enough to cover the possible return paths.

An alternative approach was proposed by Devgan *et al* based on the idea that the partial reluctance matrix (the inverse partial inductance matrix), has locality similar to capacitance matrix. This locality directly benefits extraction step through enabling window-based extraction, K method[5]. Recently, some other partial reluctance based algorithms were proposed to further improve the efficiency

[6, 7]. However, to fully take advantage of the sparse partial reluctance K matrix in simulation step, modification in conventional simulator is needed, such as KSim [8] or INDUCTWISE [9]. This becomes the major drawback that prevents K-based method being widely adopted [10].

Many effort has been spent investigating SPICE compatible approaches, while still keeping the efficiency of the K method. The double inverse method [11] proposed to invert partial reluctance matrix back into partial inductance domain to perform RLC simulation. However, it sacrifice performance and accuracy through twice matrix inversion and once more sparsification in inverted partial reluctance matrix. Wire duplication method achieved SPICE compatibility with the cost of four times couplings required in the K method and about N dummy inductors and N extra voltage controlled voltage sources for N -conductor system [12].

In this paper, two SPICE compatible circuit models for partial reluctance K were developed for the first time. One is voltage controlled voltage source (VCVS) model, the other is current controlled current source (CCCS) model. Both models are as stable, sparse, and as accurate as the K method. In fact, they are both mathematically equivalent to partial reluctance K. They can be combined with any partial reluctance based extraction method to perform SPICE compatible RLC simulation with minimum extra elements and no coupling increase.

We also proposed blocked K method based on similar group concept as in shared group calculation algorithm [6] to build symmetrical partial reluctance matrix which capture same amount of magnetic coupling information as in wire duplication method. We showed that the blocked K method only contains half of the number of individual mutual terms, and about only one third of self terms compared to the wire duplication method.

Experiment results demonstrated that the combination of VCVS model and blocked K method has the best compromise between accuracy and performance among all SPICE compatible sparsification techniques.

II. SPICE COMPATIBLE CIRCUIT MODELS FOR PARTIAL RELUCTANCE ELEMENT

One of the reason for partial inductance concept being so popular is that partial inductance obeys the same circuit branch equation as inductance does, shown in Eq. (1). Therefore, conventional SPICE can simulate partial in-

ductance element without any modification.

$$s[L]\vec{I} = \vec{V} \quad (1)$$

By definition, partial reluctance matrix K is the inverse of partial inductance matrix L .

$$[K] = [L]^{-1} \quad (2)$$

Consequently, the circuit branch equation for partial reluctance element is again the inverse linear system of partial inductance, shown in Eq. (3).

$$\frac{1}{s}[K]\vec{V} = \vec{I} \quad (3)$$

However, the conventional SPICE does not support partial reluctance element or the above branch equation Eq. (3) directly. This becomes the major road-block to adopt the K method using SPICE. It's important to create a SPICE compatible circuit model without loss efficiency of the K method.

To be compatible with SPICE, we have to manipulate the partial reluctance branch governing equation. Consider the i^{th} row in Eq. (3),

$$\sum_{j=1}^N K_{ij}V_j = sI_i \quad (4)$$

Divided by K_{ii} at both sides of Eq. (4),

$$V_i + \sum_{j=1, j \neq i}^N \frac{K_{ij}}{K_{ii}}V_j = s\frac{1}{K_{ii}}I_i \quad (5)$$

Eq. (5) can be re-written into the following format,

$$V_i = s\frac{1}{K_{ii}}I_i - \sum_{j=1, j \neq i}^N \frac{K_{ij}}{K_{ii}}V_j \quad (6)$$

where $s\frac{1}{K_{ii}}I_i$ represents the voltage drop across the inductor $\frac{1}{K_{ii}}$, and $\sum_{j=1, j \neq i}^N \frac{K_{ij}}{K_{ii}}V_j$ represents a multiple-input voltage controlled voltage source (VCVS).

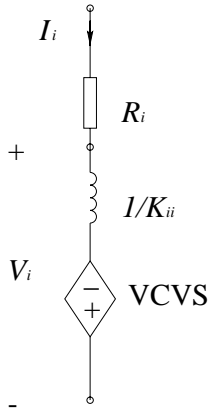


Fig. 1. SPICE compatible partial reluctance circuit model using VCVS

Figure1 shows the modeling of wire i . It's modeled as one resistor, one inductor, and one VCVS in series. The output of this VCVS is controlled by multiple inputs, that is, multiple branch voltages in the modeling of other magnetically coupled wires. Note that, there is no direct inductive couplings among different wire inductors, $\frac{1}{K_{ii}}$. All magnetic couplings among different wires are now represented by VCVSs.

For the optimized window size, wire duplication method introduces about four times couplings required in the K method and an additional $N-2b$ dummy wires where N is the total wire number, and b is the neighbor number [12]. This is about additional N dummy inductors and N extra voltage controlled sources, since $b \ll N$ in most cases. This the price wire duplication method pay for RLC simulation instead of RKC simulation. Let's examine the cost of VCVS models.

The VCVS equivalent circuit model introduces one voltage controlled source for each wire. For N -conductor system, it's additional N controlled sources. The number of couplings in K method is preserved unchanged as the number of inputs for the voltage controlled sources.

If the circuit simulator does not support controlled source with more than one input, we can expand the above multiple-input voltage controlled source into $N-1$ single-input voltage controlled sources in series. However, it is not very efficient in modified nodal analysis (MNA), since each additional node will be associated to an additional unknown node voltage, and each voltage source will be corresponding to an extra unknown current. To minimize the number of unknowns introduced by above VCVS model, we develop another SPICE-compatible model when only single-input controlled source is allowed.

Divided by s at both sides of Eq. (4), we get

$$I_i = \sum_{j=1}^N \frac{1}{s}K_{ij}V_j \quad (7)$$

We can re-write Eq. (7) as

$$I_i = \frac{1}{s}K_{ii}V_i + \sum_{j=1, j \neq i}^N \frac{K_{ij}}{K_{jj}}\left(\frac{1}{s}K_{jj}V_j\right) \quad (8)$$

If we define I_{ii} as the branch current of inductor $\frac{1}{K_{ii}}$, that is,

$$I_{ii} = \frac{1}{s}K_{ii}V_i, \quad i = 1, \dots, N, \quad (9)$$

then Eq. (8) can be represented into similar format as Eq. (6),

$$I_i = \frac{1}{s}K_{ii}V_i + \sum_{j=1, j \neq i}^N \frac{K_{ij}}{K_{jj}}I_{jj} \quad (10)$$

Eq. (10) shows the branch current of wire i is equal to the sum of branch currents of a inductor $\frac{1}{K_{ii}}$ and a current controlled current source (CCCS). This CCCS is controlled by the linear combination of branch currents of other wires. Thus, wire i can be modeled as one resistor, one inductor, and one current controlled current source (CCCS), shown in Figure2. Like previous VCVS model,

these three elements are all supported in general circuit simulator. Therefore, it's another SPICE compatible partial reluctance circuit model.

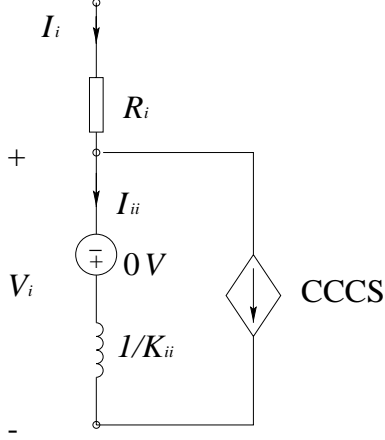


Fig. 2. SPICE compatible partial reluctance circuit model using CCCS

Compared to VCVS partial reluctance circuit model, the CCCS model introduces one extra zero voltage source per wire to serve as the reference current input for the current controlled source. This is to follow the convention rule in Berkeley SPICE and HSPICE that the reference unknown current in controlled source must be the branch current of a voltage source. Therefore, CCCS model introduces N more elements than that in VCVS model, when multiple input control source is allowed. If only single-input control source is allowed, we can expand the multiple-input current controlled current source into $N - 1$ single-input current source in parallel. Compared to VCVS model, this model has the advantage that no extra nodes are needed.

III. BLOCKED K METHOD

In traditional K-based method, if we consider $2b$ neighbor conductors for each active conductor, the window size is $2b + 1$. In total, there are about $b \cdot N$ inductive couplings and N self partial reluctance elements for N conductors system.

As pointed out in wire duplication method, a larger window size (optimal value is $4b$) is always preferred, since it can capture more inductive couplings while introduces minimum dummy elements. With larger windows, fewer groups are needed to model all conductors. Charlie *et al* proposed similar concept, shared group calculation (SGC) algorithm, on traditional K method to speed up partial reluctance extraction since fewer groups means fewer matrix inversion [6]. Physically, SGC algorithm and wire duplication method capture same amount magnetic couplings. To compare fairly, we want to use SGC algorithm as base to compare our SPICE compatible models with wire duplication method. In this section, we want to compare the size of the equivalent circuits among wire duplication

method, VCVS, and CCCS models in detail.

Note that mutual partial inductance between conductor i and conductor j are always identical, e.g. $L_{ij} = L_{ji}$. Unlike partial inductance, mutual partial reluctance K_{ij} may be different from K_{ji} due to different extraction windows. However, the SGC algorithm didn't specify how to build a symmetrical partial reluctance matrix. We propose the following blocked K method to create a symmetrical partial reluctance matrix using larger window.

Assume two adjacent groups of conductors $G^{(i-1)}$ and $G^{(i)}$. Group $G^{(i-1)}$ contains conductors $l_{p-b}, \dots, l_p, \dots, l_{q-1}, \dots, l_{q+b-1}$, where conductors $l_p, \dots, l_{q-1}, q > p$ are active conductors. Group $G^{(i)}$ contains conductors $l_{q-b}, \dots, l_q, \dots, l_{r-1}, \dots, l_{r+b-1}$, where conductors $l_q, \dots, l_r, r > q$ are active conductors. $l_{q-b}, \dots, l_{q+b-1}$ are the overlapped conductors between the two adjacent groups. For simplicity, assume each group has same neighbor number.

- For group i , calculate the partial inductance matrix L^i including all conductors from l_{q-b} to l_{r+b-1} .
- Calculate the small K^i matrix by inverting L^i .
- Fill sub-matrix $K^i(q-b : r-1, q : r-1)$ in whole K matrix at the columns corresponding to conductor l_q to l_{r-1} . Here we use same notation as in [12]: $K^i(m : n, q : r)$ refers to the sub-matrix at the intersection of the row corresponding to conductors l_m to l_n and the columns corresponding to conductors l_q to l_r , in matrix K^i .
- Fill sub-matrix $K^i(q : r-1, q-b : q-1)$ in whole K matrix at the columns corresponding to conductor l_{q-b} to l_{q-1} .
- Repeat above four steps for each group. Note that in the last group, the last b conductors from l_{N-b+1} to l_N are also active conductors.

Following the above blocked K algorithm, we can get a symmetrical sparse partial reluctance matrix K . For simplicity, we assume that all the groups are of the same size B . Same as the wire duplication method, the number of conductors commonly found in two adjacent groups are $2b$. So the number of groups need is $n = \frac{(N-2b)}{(B-2b)}$ [12]. According to above algorithm, each group except the first and last ones, has $(B-2b)(B-b)$ elements for active conductors and $b(B-2b)$ elements for overlapped conductors with previous group, that is combined $B(B-2b)$ elements. The first group will contribute $(B-b)^2$ elements since it has no previous group. The last group contributes $(B-b)B + b(B-b)$ elements, since the last group has $B-b$ active conductors.

So the total number of elements in final K matrix is

$$(n-2) \cdot B(B-2b) + (B-b)^2 + (B+b)(B-b) = N \cdot B.$$

Besides the N self partial reluctance elements, there are $0.5N \cdot (B-1)$ inductive couplings. If we pick $B = 4b$, same as the optimal window size as in wire duplication

method, blocked K method has about two times couplings required in traditional K method, and half of the number of couplings required in wire duplication method.

Since there is no dummy wires in blocked K method, the self partial reluctance number is the same as traditional K method, about one third of branches which are required in wire duplication method.

If apply VCVS model on blocked K method, there will be the half number of couplings and self inductors, and the same number of VCVSs compared to wire duplication method. As for CCCS model applied on blocked K method, there will be the half of the number of couplings and the same number of branches and controlled sources.

IV. EXPERIMENT RESULTS

To verify the accuracy of the above two SPICE compatible circuit models of partial reluctance element, we choose a bus structure consisting of 128 conductors. The driver resistance is 50Ω , and the load capacitance is $30fF$. To exaggerate far away current return path effect, only the 128th conductor is a return wire with no driver resistance. The length of all conductors is 1mm, the cross-section is $1 \times 1\mu m$, and the spacing between conductors is $1\mu m$. Each conductor is broken into five equal segments in order to create a large yet illustrative system matrix.

A 1V 10ps ramp input is applied to the first conductor, and the rest are quiet. The reference results are obtained through full partial inductance matrix, that is including all inductive couplings between every pair of segments. Six different sparsification algorithms are implemented, VCVS model, CCCS model, blocked K method, wire duplication method [12], shift-truncation method [13], and double inverse method [11]. The truncation only method has negative eigenvalues, leading to unstable simulation result, which is not shown here.

The far end node voltage responses of conductor 1 are shown in Figure3 and Figure4. The far end node voltage responses of conductor 4 are shown in Figure5 and Figure6. Out of all the different approaches, only the blocked K method is not SPICE compatible, and is obtained through KSim [8], all other SPICE compatible simulations are performed by Berkeley SPICE. As introduced by Ji, *et al*[8], KSim shares same mathematical engine as Berkeley SPICE, just enhanced to simulate partial reluctance K directly. So the performance gain by blocked K method only results in the partial reluctance algorithm itself, instead of simulation engine.

In wire duplication method, we choose neighbor number as 2, and the optimal window size, which is 8.

To capture same amount of couplings, we implement blocked K method as described in section III, using the same window size and neighbor number as in wire duplication method. In this case, 404,480 of the total 409,600 matrix terms are set to zero (about 98.75% sparse). Both VCVS and CCCS models are then applied on blocked K method. From Figure 3 and Figure 5, we can first observe that both VCVS and CCCS models match exactly with the blocked K method. This is as expected since we have

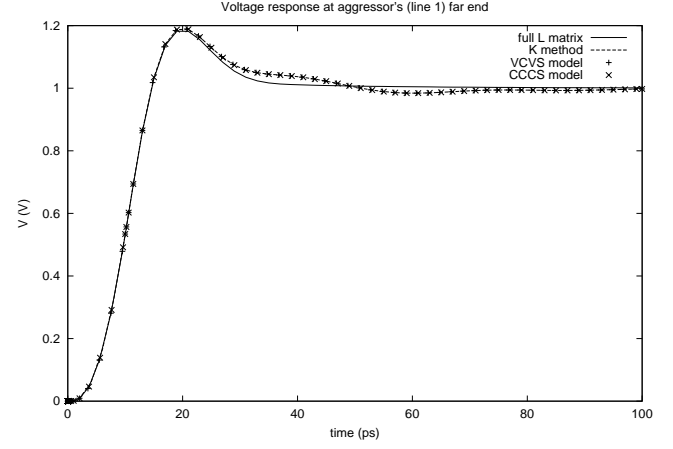


Fig. 3. Voltage response at aggressor's (line 1) far end for proposed blocked K method, VCVS and CCCS models in this paper

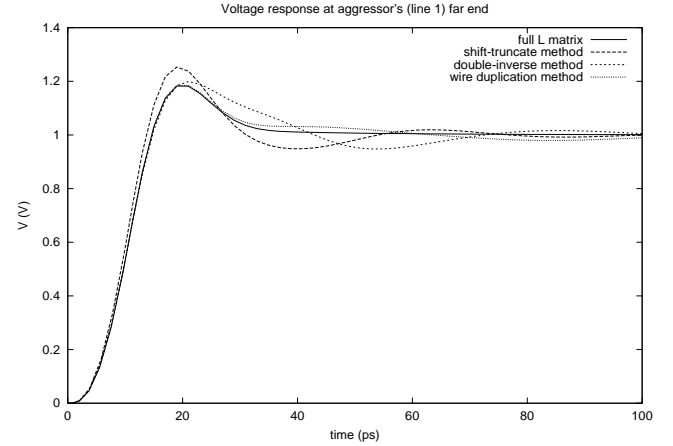


Fig. 4. Voltage response at aggressor's (line 1) far end for previous methods in literatures

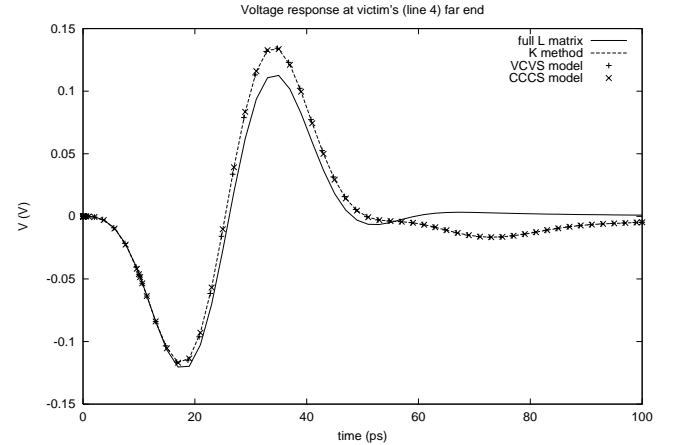


Fig. 5. Voltage response at victim's (line 4) far end for proposed blocked K method, VCVS and CCCS models in this paper

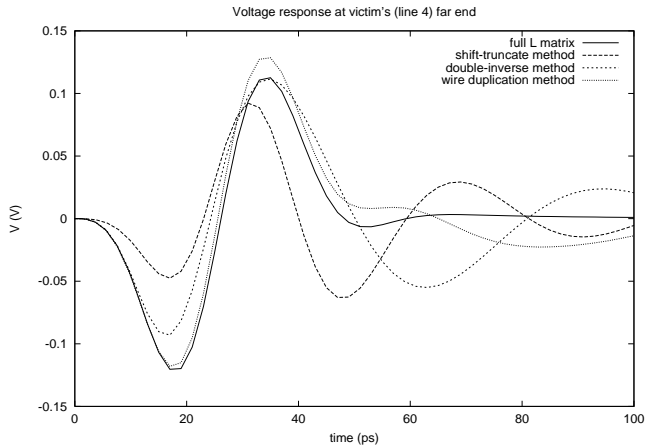


Fig. 6. Voltage response at victim's (line 4) far end for previous methods in literatures

shown both models are mathematically equivalent to K. Secondly, the blocked K method and VCVS/CCCS model are all very close to the corresponding reference results. There is only negligible difference for the aggressor's delay and overshoot, and victim's first undershoot.

We also implemented double inverse method and shift-truncation method. Both approaches have similar number of inductive couplings as in blocked K method, that is about half number of coupling as in wire duplication method. We can see that the waveform of both shift-truncation method and double inverse method deviate significantly from the reference results, especially for victim's far end voltage response, shown in Figure 4 and Figure 6.

The waveforms of wire duplication method are much better than other previous method in the literatures, such as double inverse method and shift-truncation method, since it contains more coupling items. Its waveforms are close to the corresponding reference results, but does not converge to the reference results as fast as the VCVS and CCCS models, even with more coupling items. Note that the blocked K method/VCVS/CCCS model only contain half number of inductive couplings as in wire duplication method with same window size as we analyzed in Section III. Due to more coupling terms, it's not surprisingly shown in below performance table that the wire duplication method is slower compared to all the approaches proposed in this paper, the blocked K method, and the VCVS/CCCS models.

Table 1 shows the simulation time of different approaches. Clearly, the direct partial reluctance element simulation, blocked K method, shows the most speed up compared to other sparsification techniques. However, it requires extra modification in conventional simulators [8, 9].

The performance of CCCS model is similar to wire duplication model. This is not much surprise, since both models have similar circuit system size, which is about $3N$ inductors and voltage/current sources in total. Although CCCS model is a little slower than shift-

Table 1. Run time of different methods

method	CPU time(s)	Speed up
full L matrix	18838.5	1.0x
blocked K method	9.0	2093x
VCVS model	38.2	493x
shift-truncate	107.9	175x
wire duplication method	138.8	136x
CCCS model	140.3	134x
double inverse method	423.8	44x

truncation method under same sparsity condition, it is much more accurate as shown in Figure 3 to and Figure 6.

The VCVS model achieves about 3.6 times speed up compared to wire duplication model, since VCVS model only use N inductors and N voltage sources, which is about N unknowns less than wire duplication model. This advantage will become even greater for larger designs, since simulators always involves super-linear matrix operations. Therefore, in cases where direct partial reluctance simulator is not available, VCVS model shows the best compromise between accuracy and performance. It spends the least amount of time for RLC simulation while maintains exact same accuracy as the K method.

V. CONCLUDING REMARKS

Two SPICE compatible circuit models were developed for the first time for partial reluctance K. Both models are able to construct SPICE compatible circuits out of reluctance net lists with only N or $2N$ extra elements, and no couplings increase needed. They are able to fully utilize the accuracy and sparsity of partial reluctance based extraction method without the need of inverting partial reluctance matrix back to inductance, or modifying conventional SPICE simulators.

To capture more magnetic couplings while preserving symmetry of partial reluctance matrix, we also proposed blocked K method. Detail analysis was performed to determine the advantage of each partial reluctance model.

Both mathematical analysis and experiment results demonstrated that the combination of VCVS model and blocked K method achieved the best accuracy and efficiency as compared to alternative SPICE compatible approaches.

REFERENCES

- [1] E. Rosa, "The self and mutual inductance of linear conductors," in *Bulletin of the National Bureau of Standards*, vol. 4, pp. 301–344, 1908.
- [2] A. Ruehli, "Inductance calculations in a complex integrated circuit environment," *IBM Journal of Research and Development*, vol. 16, pp. 470–481, Sept. 1972.
- [3] B. Krauter and L. Pileggi, "Generating sparse partial inductance matrices with guaranteed stability," in

- [4] Z. He, M. Celik, and L. Pileggi, “SPIE: Sparse partial inductance extraction,” in *Proc. 34th Design Automation Conference*, pp. 137–140, June 1997.
- [5] A. Devgan, H. Ji, and W. Dai, “How to efficiently capture on-chip inductance effect: Introducing a new circuit element K,” in *Proc. IEEE International Conference on Computer Aided Design*, pp. 150–155, Nov. 2000.
- [6] T.-H. Chen, H.-S. Kim, and C. C.-P. Chen, “L extracted? Now what? Introduction to an Inductance-Wise interconnect simulation engine (INDUCTWISE),” *Technical Report, University of Wisconsin-Madison*, 2002.
- [7] H. Zheng and L. Pileggi, “Modeling and analysis of regular symmetrically structured power/ground distribution networks,” in *Proc. Design Automation Conference(DAC)*, pp. 395–398, June 2002.
- [8] H. Ji, A. Devgan, and W. Dai, “KSim: A stable and efficient RKC simulator for capturing on-chip inductance effect,” in *Proc. Asia and South Pacific Design Automation Conference*, pp. 379–384, Jan. 2001.
- [9] T.-H. Chen, C. Luk, H. Kim, and C. C.-P. Chen, “INDUCTWISE: Inductance-wise interconnect simulator and extractor,” in *Proc. IEEE International Conference on Computer Aided Design(ICCAD)*, pp. 215–220, Nov. 2002.
- [10] D. Sitaram, Y. Zheng, and K. Shhepard, “Implicit treatment of substrate and power-ground losses in return-limited inductance extraction,” in *Proc. IEEE International Conference on Computer Aided Design(ICCAD)*, pp. 16–22, Nov. 2002.
- [11] M. Beattie and L. Pileggi, “Efficient inductance extraction via windowing,” in *Proc. Design Automation and Test in Europe Conference*, pp. 430–436, Mar. 2001.
- [12] G. Zhong, C.-K. Koh, and K. Roy, “On-chip interconnect modeling by wire duplication,” in *Proc. IEEE International Conference on Computer Aided Design(ICCAD)*, pp. 341–346, Nov. 2002.
- [13] M. Beattie, L. Alatan, and L. Pileggi, “Equipotential shells for efficient partial inductance extraction,” in *Proc. IEDM’98*, Dec. 1998.