A Dynamic Element Matching Circuit for Multi-bit Delta-Sigma Modulators

Ryozo Katoh, Shin-ya Kobayashi, and Takao Waho

Department of Electrical and Electronics Engineering
Sophia University
7-1 Kiocho, Chiyoda-ku, Tokyo 102-8554, Japan
e-mail: {ryozo, waho}@sscd.ee.sophia.ac.jp

Abstract—

A 30k-gate dynamic element matching circuit for bandpass ΔΣ modulators with a 4-bit quantizer is designed by using 0.35-μm CMOS technology. Second-order bandpass mismatch-shaping algorithm improves the signal-to-noise ratio by ∼30dB (∼5 bit). The core circuit area and the estimated operation speed were 1.44 mm^2 and 20 MHz, respectively.

I. Introduction

Conventional ΔΣ modulators (DSMs) use a 1-bit quantizer. By increasing the oversampling ratios (OSRs), *i. e.* the ratio of the sampling rate to the Nyquist rate, and /or the loop-filter order, the signal-to-noise ratio (SNR) has been improved. An alternative approach to improve the SNR, is to use a multi-bit or multi-level quantizer. Since the sampling frequency is not necessarily high, the multi-bit scheme is attractive for higher-frequency applications. A drawback is that the SNR suffers from the nonlinearity of the internal digital-to-analog converter (DAC), since the feedback signal from the DAC is directly added to the input.

To overcome this problem, dynamic element matching (DEM) technique was proposed [1], where the DAC unit elements are randomly selected so that mismatch errors are smeared out. There are several reports of DEM-based DSMs, which include a lowpass DSM with a sampling frequency f_s of 20MHz using BiDWA architecture [2] and that using a tree structure (f_s = 5MHz) [3]. Although a bandpass DSM was also presented, f_s remains as low as 0.5MHz [4]. We have designed a 20-MHz DEM circuit for bandpass DSMs based on vector feedback architecture.

II. Operation Principle

A typical fourth-order bandpass ΔΣ modulator is shown in Fig. 1, where DEM follows the 16-level (4-bit) quantizer. It is assumed that the DEM input is a 16-bit thermometer-code vector v and its output is a 16-bit selecting vector sv to actuate 16 unit current elements in the DAC. The output is determined by the mismatch-shaping algorithm [4]. The DAC nonlinearity *de* stemming from the mismatch in the unit current elements is suppressed by the following formula: $DV(z) = v(z)+H(z)(se(z)\cdot de)$,

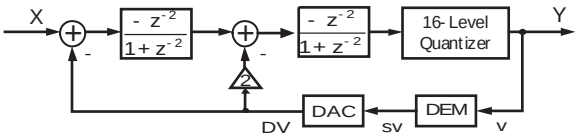

Fig. 1. Fourth-order bandpass ΔΣ modulator with dynamic element matching technique.

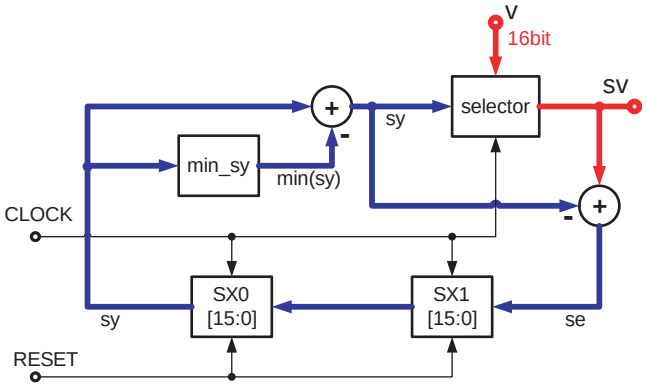

Fig. 2. DEM block diagram.

where $H(z) = 1 + z^{-2}$. Figure 2 shows the present implementation of the DEM. Two registers, SX0 and SX1, were used to obtain the delay z^{-2}. The 16-bit selector sorts the sy components in the descendent order, and outputs the sy port numbers representing the top v components. For example, if v is equal to 5, or 0000000000011111 in the thermometer code, the output is 0000010100010101, where five 1's exist.

III. Results

Figure 3 shows the timing chart obtained for the present DEM circuit. This is a simulation result using a back-annotated file, and shows that the present circuit can operate at a frequency of 20MHz. It should be noted that the each output bit turns on in a random order as the input increases. Since this is a bandpass circuit, it is not straightforward to see that the function is appropriate. By carrying out MATLAB simulations based

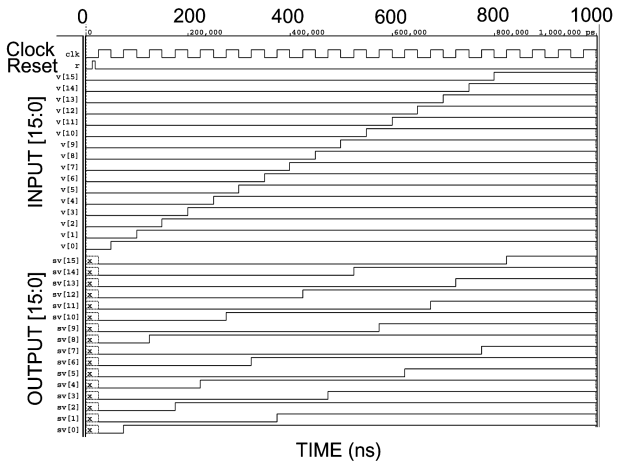

Fig. 3. Timing chart.

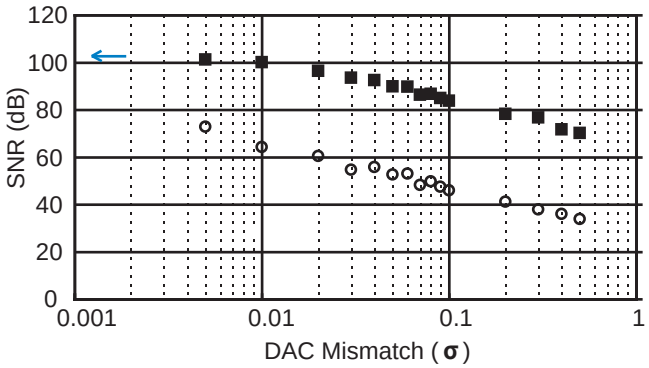

Fig. 4. Estimated SNR as a function of the DAC mismatch. Closed and open plots represent the SNR with and without DEM, respectively. The arrow indicates the SNR value without the mismatch.

on the present DEM circuit design, we have confirmed the bandpass-type mismatch-shaping characteristic. The SNR of the total DSM system shown in Fig. 1 is also calculated by assuming an OSR of 64. The result is shown in Fig. 4. Although the SNR decreases with the increase in the DAC mismatch, it is shown that the present DEM circuit is effective to improve the SNR by $\sim$ 30dB ($\sim$ 5bit). The chip photograph is depicted in Fig. 5, and the performance is summarized in Table 1.

Acknowledgements

The LSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.

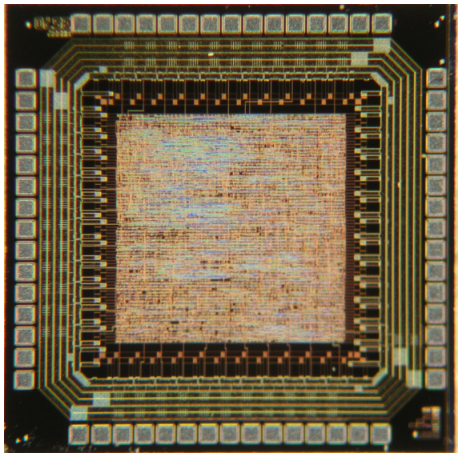

Fig. 5. Fabricated chip micrograph.

TABLE I
Summary

Technology	0.35μm CMOS
Chip size	2.45 x 2.45 mm^2
	1.44 mm^2 (Core)
Input	16-bit thermometer code
Output	16-bit selecting signal
Supply voltage	3.3 V
Gate count	$\sim$ 30,000
Clock frequency	20 MHz
Power dissipation	14 mW

References

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