

# A Performance Comparison of PLLs for Clock Generation Using Ring Oscillator VCO and LC Oscillator in a Digital CMOS Process

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**Abstract**— This paper describes a performance comparison of two PLLs for clock generation using a ring oscillator based VCO and an LC oscillator based VCO. We fabricate two 1.6GHz PLLs in a 0.18  $\mu\text{m}$  digital CMOS process and compare their performances based on the measurement results. We also predicts major performances of PLLs in the future such as jitter, power consumption and chip area, based on a qualitative evaluation in an analytic way.

## I. INTRODUCTION

Phase-Locked Loops (PLLs) are widely used for clock generation in high-speed digital systems. Voltage-Controlled Oscillator (VCO) is a key component of PLLs and we have two choices: a voltage-controlled ring oscillator (ringVCO) and a voltage-controlled LC oscillator (LCVCO). A ringVCO has been considered to be a better choice, because of its low power consumption, small chip area and wide tunable frequency range. Recent increase in clock speed and the latest multi-GHz serial link circuits, however, requires rigid jitter performance. It is getting harder to satisfy the design requirements using a simple ringVCO. In contrast, an LCVCO is superior to a ringVCO in terms of noise characteristics such as phase noise and jitter [1].

In this work we fabricate two 1.6GHz PLLs using a basic ringVCO and a basic LCVCO, and compare their performances based on the measurement results. This paper also discusses the performance prediction of clock generation PLLs in an analytic way.

## II. PLL ARCHITECTURE

The PLL architecture under our study is shown in Fig.1. It is composed of five major blocks: a phase-frequency detector(PFD), a charge pump, a second order loop filter, a voltage-controlled oscillator(VCO) and a divider. All the components including the loop filter and the output buffer are integrated.

The designed ringVCO and LCVCO are shown in Fig. 2 and Fig. 3 respectively. The ringVCO is five-stage differential inverters. The LCVCO is an NMOS cross-coupled differential oscillator composed of two square-shaped spiral inductor and a differential diode varactor.

## III. EXPERIMENTAL RESULTS

We fabricated and measured two clock generation PLLs in a 0.18  $\mu\text{m}$  digital CMOS process. Supply voltage is set to 1.8V. The operational frequency is 1.6GHz and the oscillation amplitude is controlled to be 400mV. PLL reference frequency of 25MHz is given by a crystal oscillator. We compare their performances; area, power consumption, tunable frequency range, spectrum, jitter and phase noise.

Figure 4 shows the output spectrums of two 1.6GHz PLLs. We can see that LCPLL spectrum is much sharper. Die pho-

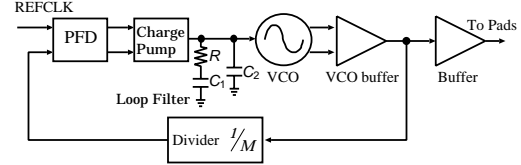


Fig. 1. PLL Architecture

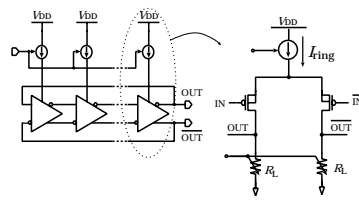


Fig. 2. Differential Ring Oscillator

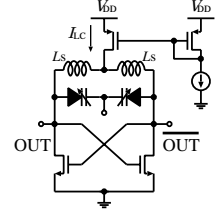


Fig. 3. Differential LC Oscillator

tographs of two PLLs with the same scale ratio are also shown in Fig. 4. Table I lists the measured performances of two fabricated PLLs. In comparison with the LCPLL, the ringPLL has a tenfold tunable frequency range, a 1/4 core chip area and a 1/2 power consumption. In the noise characteristics, however, the LCPLL indicates better performances. Jitter is reduced by 2/3, and phase noise at 1MHz offset decreases by 50dB/Hz compared with the ringPLL.

## IV. PERFORMANCE COMPARISON IN THE FUTURE

ITRS roadmap [2] forecasts that the operating frequency will be over 5GHz in 2008 and near 15GHz in 2014. In this section, we predict major performances of both PLLs such as jitter, power consumption and chip area with a qualitative discussion by an analytical approach.

We use the minimum channel length  $L$  of the device and the same  $W/L$  ratio at every technology node. The number of inverter stage in ringVCO is unchanged. The ratio of oscillation voltage amplitude and supply voltage ( $V_{DD}$ ) is kept unchanged. We assume the  $Q$  value of spiral inductor is constant in every technology node, which we consider to be conservative. Our prediction uses  $V_{DD}$  and  $f_0$  in Table II that are indicated by ITRS roadmap [2].

We predict the jitter characteristic ((jitter  $J$ )/(oscillation period  $T_0$ )) of both VCOs. First, we examine  $J_{ring}/T_0$  of

TABLE I  
THE MEASURED PERFORMANCES OF TWO PLLS (OUT  
FREQUENCY=1.6GHz).

	Ring PLL	LC PLL
Technology	0.18 $\mu\text{m}$ digital CMOS, 5LM, 1.8V	
Frequency Range	400MHz - 1.8GHz	1.49GHz - 1.64GHz
Power Consumption	10.4mW	22.1mW
PkPk/RMS jitter	91ps/15.9ps	29ps/3.6ps
Phase Noise@1MHz	-65dBc/Hz	-113dBc/Hz
Core Chip Area	0.07mm <sup>2</sup>	0.26mm <sup>2</sup>

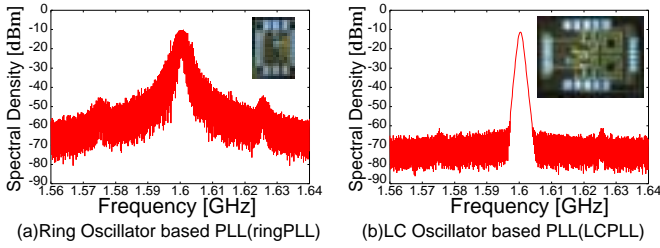


Fig. 4. Output spectrums of two 1.6GHz PLLs and die photographs of two PLLs with the same scale ratio. LCPLL spectrum is much sharper and ringPLL area is much smaller.

ringVCO, which is expressed as [1, 3]

$$\frac{J_{\text{ring}}}{T_0} = \sqrt{\frac{8N}{3\eta} \cdot \frac{kT}{P_{\text{ring}}} \cdot \left( \frac{V_{\text{DD}}}{V_{\text{char}}} + \frac{V_{\text{DD}}}{R_L I_{\text{ring}}} \right) \cdot f_0}, \quad (1)$$

where  $f_0$  is the oscillation frequency,  $N$  is the number of inverter stage,  $P_{\text{ring}}$  is the power consumption of ringVCO,  $I_{\text{ring}}$  is the tail current of each inverter and  $R_L$  is the load resistance. Parameter  $\eta$  is a constant that represents the proportional relation between rise time and delay time of inverters,  $k$  is the Boltzmann constant and  $T$  is the temperature.  $V_{\text{char}}$  is the characteristic voltage of the device, which is proportional to  $L$  [1].

In our evaluation,  $N$ ,  $\eta$ ,  $k$  and  $T$  are constant in every technology node.  $L$  and  $V_{\text{DD}}$  have a proportional relation roughly, ITRS predicts. Therefore,  $V_{\text{DD}}/V_{\text{char}}$  is constant.  $V_{\text{DD}}/R_L I_{\text{ring}}$  is also constant, since  $R_L I_{\text{ring}}$  expresses oscillation amplitude. The unknown parameter left is  $P_{\text{ring}}$ . We evaluate the trend of  $P_{\text{ring}}$ .

$P_{\text{ring}}$  is expressed as the product of  $N$ ,  $I_{\text{ring}}$  and  $V_{\text{DD}}$ .  $I_{\text{ring}}$  is proportional to the product of  $f_0$  and  $q_{\text{max}}$ , where  $q_{\text{max}}$  is the charge stored in each node during a cycle. Parameter  $q_{\text{max}}$  is proportional to the device channel width  $W$ , so  $I_{\text{ring}}$  will be roughly unchanged in the future. Therefore  $P_{\text{ring}}$  is proportional to  $V_{\text{DD}}$ . Consequently,  $J_{\text{ring}}/T_0$  can be expressed as

$$\frac{J_{\text{ring}}}{T_0} \propto \sqrt{f_0/V_{\text{DD}}}. \quad (2)$$

Next,  $J_{\text{LC}}/T_0$  of LCVCO is examined.  $J_{\text{LC}}/T_0$  is expressed as [4]

$$\frac{J_{\text{LC}}}{T_0} = \sqrt{\frac{FkTr_{\text{eq}}}{V_{\text{osc}}^2 Q_T^2}} \cdot f_0, \quad (3)$$

where  $V_{\text{osc}}$  is the oscillation amplitude and  $r_{\text{eq}}$  is the loss ingredient of the LC resonator, which is expressed as  $r_{\text{eq}} = 2\pi f_0 Q_T L_s$ .  $Q_T$  is the quality factor of the LC resonator, which is roughly equal to the quality factor of the spiral inductor.  $F$  is the differential oscillator Leeson's noise factor [4], which is almost constant in every technology node, since we assume  $V_{\text{osc}}/V_{\text{DD}}$  is fixed in every technology node. Parameters  $k$  and  $T$  are also constant. Therefore, when we design LCVCO keeping  $f_0 L_s/V_{\text{DD}}$  constant,  $J_{\text{LC}}/T_0$  can be expressed as

$$\frac{J_{\text{LC}}}{T_0} \propto \sqrt{f_0/V_{\text{DD}}}. \quad (4)$$

From Eq. (2), Eq. (4) and Table II, jitter characteristics of both VCOs are inversely proportional to technology advance. Figure 5 shows how jitter characteristics (jitter/period) get worse

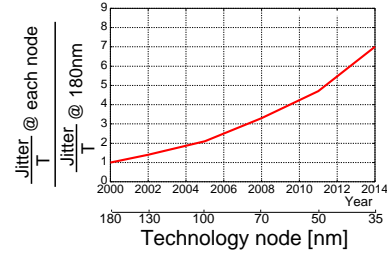


Fig. 5. Jitter characteristic degradation.

TABLE II  
DEVICE PARAMETERS USED FOR OUR FUTURE PREDICTION AND  
PREDICTED POWER CONSUMPTION AND CHIP AREA OF THE FUTURE PLLS.

Year	Meas.	2002	2005	2008	2011	2014
Tech Node[nm]	180	130	100	70	50	35
$V_{\text{DD}}$ [V]	1.8	1.2	0.9	0.6	0.5	0.3
$f_0$ [GHz]	1.6	2.1	3.5	6	10	13.5
$P_{\text{ring}}$ [mW]	3.4	1.1	0.88	0.47	0.50	0.15
$P_{\text{LC}}$ [mW]	7.2	4.7	3.2	2.5	2.6	2.0
ringPLL Area[mm <sup>2</sup> ]	0.070	0.025	0.018	0.015	0.010	0.007
LCPLL Area[mm <sup>2</sup> ]	0.260	0.12	0.10	0.067	0.036	0.024

as technology advance. The jitter characteristic at technology node 180nm is set to 1. Jitter characteristic in 2014 becomes seven times worse than now.

As well as above jitter evaluation, we evaluate power consumption and chip area of both PLLs. According to our prediction, power consumption of both PLLs decreases proportional to the supply voltage  $V_{\text{DD}}$ . Chip area decreases proportional to the technology node. We design circuits in the future using the transistor model [5] based on the ITRS roadmap [2] and evaluate power consumption and chip area of both PLLs. The results are shown in Table II. We can see power consumption and chip area of both PLLs decrease almost proportional to the technology node.

## V. CONCLUSION

This paper compares the performance of two clock generation PLLs, a ring oscillator based PLL and an LC oscillator based PLL with the design experiment and with the qualitative evaluation. Our measurement results show that in chip area, power consumption and tunable frequency range, a ringPLL is superior to an LCPLL, but as for phase noise and jitter, an LCPLL is far excellent. According to our prediction, the relative performance difference between ringPLL and LCPLL will be almost constant in the future. Power consumption and chip area of both PLLs will decrease proportional to the technology node. However, noise characteristics will get worse inversely proportional to the technology node.

## Acknowledge

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## REFERENCES

- [1] A. Hajimiri and T. H. Lee, "The Design of Low Noise Oscillators," Kluwer Academic Publishers, 1999.
- [2] "International Technology Roadmap for Semiconductors 1999," SIA, Sematech Inc., 1999.
- [3] K. Kundert, "Modeling Jitter in PLL-based Frequency Synthesizers," <http://www.designers-guide.com>
- [4] J. J. Rael and A. A. Abidi, "Physical Processes of Phase Noise in Differential LC Oscillators," *Proc. CICC*, pp. 569–572, 2000.
- [5] "Standard SPICE model based on ITRS'99," [http://lowpower.iis.u-tokyo.ac.jp/ina/index\\_e.html](http://lowpower.iis.u-tokyo.ac.jp/ina/index_e.html)