

A High Efficiency 0.5W BTL Class-D Audio Amplifier with RWDM Technique

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Abstract A novel class-D amplifier comprises a Rectangular Wave Delta Modulator (RWDM), bridged tied load (BTL) output gate-driver and low-pass filter. The rectangular wave delta modulator has a multiple inputs floating-gate hysteresis comparator and a feedback integrator formed by the L - R low-pass filter. This integrated amplifier has a flat frequency response with ± 0.3 dB up to 20 kHz, deliver up to 0.5 Watts with 97% power efficiency, and a total harmonic distortion of less than 1% over power and frequency range.

1. Introduction

Another common method of generating the output signal in class-D amplifier is to make use of a delta modulation scheme [4]. A modulated rectangular wave is produced whose average value tracks that of the input signal as well. Rectangular wave delta modulation (RWDM) has become an established alternative to PWM audio applications for providing a sinusoidal output voltage with a low harmonic content and ease of control of comparator output voltage [5,6]. In this paper a class-D amplifier based on the RWDM technique is proposed. The proposed RWDM scheme of class-D amplifier, as depicted in Fig. 1(b), comprises only a hysteresis comparator, gate-driving circuits and a feedback integrator formed by the L - R low-pass filter. Basically RWDM is analogous to PWM except the input signal is compared with the feedback signal that is essentially the integrated signal of RWDM by a low-pass filter. Unlike the conventional PWM class-D amplifier, proposed RWDM scheme of class-D amplifier does not require an external triangular-waveform oscillator. This benefits the design to achieve smaller chip area, lower cost and simpler application circuits.

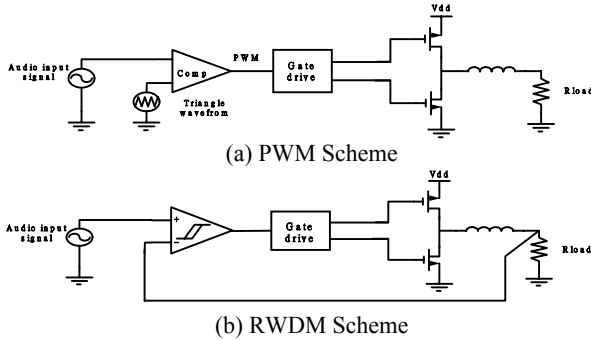


Fig. 1. Illustrations of class-D amplifier in (a) PWM scheme and (b) RWDM scheme.

The class-D amplifier based on the RWDM scheme, except for the inductor and the speaker load, could be verified and implemented into a single-chip by UMC 0.5 μ m CMOS process. The proposed RWDM class-D integrated amplifier is well-suited as a monolithic chip for battery-powered portable consumer electronic applications.

2. Principles of RWDM Technique

The principle of operation of the RWDM technique can be described with the aid of block diagram shown in Fig. 2. The audio input signal denoted as $V_i(t)$ is compared with the feedback signal or a carrier signal $V_c(t)$, obtained by integrating the modulated signal $V_m(t)$, to produce an error signal $Er(t)$. According to the sign and preset magnitude of $Er(t)$, the

modulated output signal $V_m(t)$ has two possible values $\pm V_s$, whereas the time duration between two successive levels is determined by the slope of audio input signal $V_i(t)$. It can be seen that the feedback signal $V_c(t)$ tracks the audio input signal $V_i(t)$ within the upper and lower boundary levels $\pm \Delta V$. From the modulator-operating principles, it can be observed that the RWDM output signal is decided by the integrator in the feedback path. Assuming that the modulator-switching frequency is high enough so that a small portion of the audio input sine wave is approximated by a straight line, the time duration for one complete cycle at the modulator output is given by [4]

$$T = \frac{4\Delta V S_c}{S_c^2 - S_i^2(t)|_{AC}} \quad (1)$$

Where

- $S_i(t)$ = instantaneous slope of the audio input signal between points A and C ,
- $S_i(t)|_{AC}$ = slope of the reference signal between points A and C ,
- $\pm \Delta V$ = value of the hysteresis window, and
- $S_c(t)$ = slope of the carrier wave.

The switching frequency of the modulator output is obtained from (1) as

$$f = \frac{1}{T} = \frac{S_c}{4\Delta V} \left[1 - \left(\frac{S_i(t)}{S_c} \right)^2 \right] \quad (2)$$

For an input sinusoidal waveform, $V_i \sin \omega t$, the instantaneous slope of the audio input signal is given by

$$S_i(t) = \omega V_i \cos \omega t \quad (3)$$

And the modulator output switching frequency is obtained as

$$f = \frac{S_i}{4\Delta V} \left[1 - \left(\frac{\omega V_i}{S_c} \right)^2 \cos^2 \omega t \right] \quad (4)$$

Equation (4) shows the following:

- 1) The modulator switching frequency reaches a maximum value of $(S_c/4\Delta V)$ at $\omega t = k(\pi/2)$, where k is an odd number, resulting in an inherent minimum pulse width at the modulator output. Thus, no special effort is needed to provide minimum pulse width duration in the class-D amplifier.
- 2) The modulator switching frequency has a minimum value of $(S_c/4\Delta V)[1 - (\omega V_i/S_c)^2]$, resulting in a maximum pulse at the modulator output.
- 3) The average switching frequency of the modulator is obtained by averaging the modulator instantaneous switching frequency over several cycles of the audio input signal and is given by

$$F_{avg} = \frac{S_c}{4\Delta V} \left[1 - \frac{\omega^2 V_i^2}{2 \times S_c^2} \right] \quad (5)$$

Since the switching power loss in the class-D amplifier depends on the average switching frequency of the modulator, (5) shows that the efficiency of RWDM class-D amplifier can be optimized by selecting appropriate values of the modulator parameters. From the operating principle of the RWDM, it can be seen that

the modulator parameters that affect the frequency spectrum of the modulator output and hence the class-D amplifier output voltage are

- 1) The hysteresis bandwidth ΔV , is controlled directly by the trip voltage of hysteresis comparator.
- 2) The integrator gain S_c , is controlled by the time constant of the integrator in the feedback path.
- 3) The amplitude of the audio input signal V_i .

As a hysteresis behavior in the comparator, $V_c(t)$ can track the amplitude of $V_i(t)$ within the $\pm\Delta V$ boundary as shown in Fig. 2. Also the feedback signal $V_c(t)$ is the integrated signal of RWDM from a low-pass filter at the output, loading conditions from the loads are taken into account to control the RWDM signal and then to control the output power.

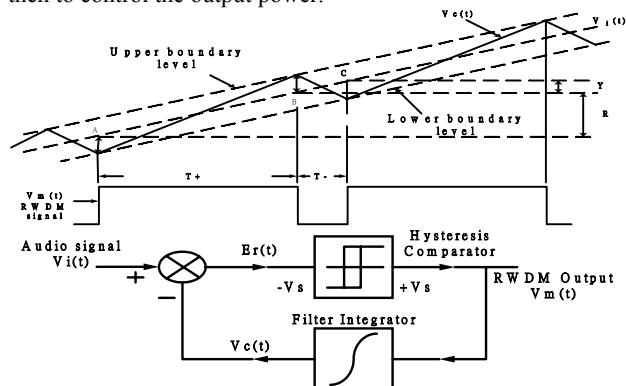


Fig. 2. Block diagram of the RWDM technique.

3. Design Principles

Fig. 3 shows the comprehensive configuration of a Bridge Tied Load (BTL) class-D amplifier based on the RWDM technique. It is basically a fully differential version of the proposed RWDM scheme shown in Fig. 1(b). By using the BTL configuration, the maximum audio output voltage swing can be double those of the half-bridge configuration in Fig. 1(b). The audio input signal is directly connected to the input of the hysteresis comparator, which is ultimately a high impedance of an input MOSFET hence the loading effect of the signal source will not occur. The switching range of a hysteresis comparator is extended to control the amount of output ripple and switching frequency of the class-D amplifier. With the fitted hysteresis loop, the comparator can produce the output RWDM signal containing only logic low or high that is then integrated by the resistor-inductor L - R network.

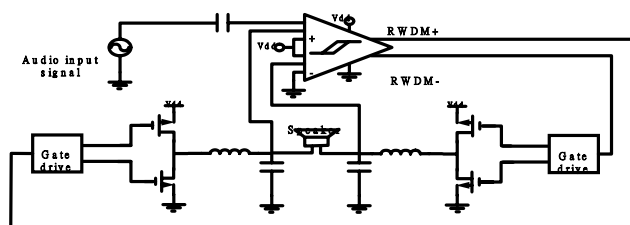


Fig. 3 The BTL configuration of class-D amplifier.

An illustration of a rail-to-rail hysteresis comparator [7] is shown in Fig. 4, where it is seen that the hysteresis is provided from two positive feedback paths produced by M_{10} and M_{11} . The positive feedback occurs only when the current ratio of I_{D10}/I_{D3} or I_{D11}/I_{D4} is greater than unity. If these current ratios increase further, the positive feedback current will increase as well. It expands the positive and negative trip point voltage hence a wider hysteresis is formed and can be controlled. This tunable hysteresis enables the comparator process a wide-range input signal. As represented particular wide-range input the comparator will compare the input signal with the saw-tooth-like feedback signal from the output in the following cycle. This characteristic allows the feedback signal at the gate of M_2 to

track the amplitude of the input signal at the gate of M_1 effectively between V_{DD} and ground. Since one of the input gates of both M_1 and M_2 are connected to V_{DD} , so both FG MOSs of M_1 and M_2 are ensured to be turned on at all levels of the input signal. It enables the hysteresis comparator to perform the rail-to-rail feature in a lower supply voltage.

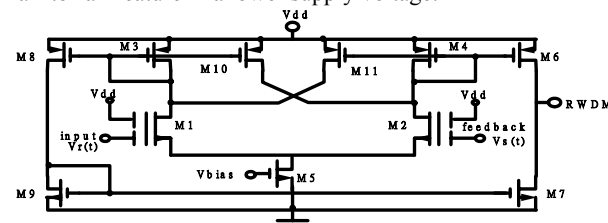


Fig. 4. A rail-to-rail input hysteresis comparator.

4. Preliminary Results

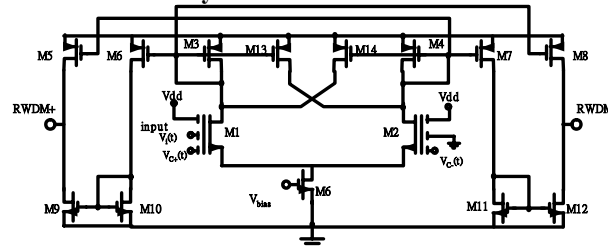


Fig. 5 A wide-range fully differential comparator.

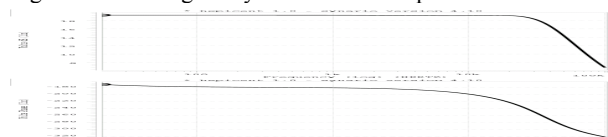


Fig. 6 Frequency response (magnitude/phase) of the amplifier.

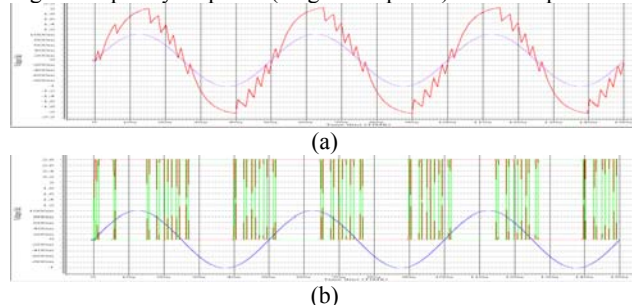


Fig. 7 (a) The output voltage signal and (b) RWDM output signal are compared with input audio waveforms of 1 V, 20 kHz.

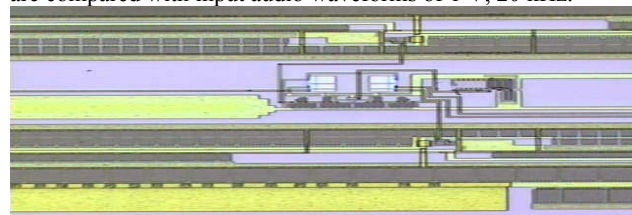


Fig. 8 A micrograph of 0.5W RWDM class-D amplifier IC.

Table I
Summaries of RWDM Class-D IC Major Specifications

Class-D Audio IC Specifications	Performance
Power Supply	2.8 V
Speaker Load	8 Ω
Gain	20dB
Static Power Dissipation	68.6 μ W
Max Output Swing	5.4 V
Max Output Power /channel	0.5 W
THD+N (1 kHz)	< 0.6%
Efficiency	97%