RF Design Methodologies bridging System-IC-Module Design

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Abstract - There has been a long-standing need to link the RF design domains into a connected, common design environment. Such a methodology is possible through implementing system-level behavioral models with different levels of abstraction that can be modeled or co-simulated at the IC circuit level. At module or board design, it is possible to link and simulate multiple chips with board-level components and parastics in an RFIC design environment.

With today's more complex IC designs that are heading toward nanometer-scaled semiconductor processes, there is a desire to further understand the many subtle physical IC characteristics, such as layout and substrate parasitics, RF transistor models, IR drops, electromigration, elctromagnetics, and modeling of on-chip spiral inductors. Designers have entered into an era where they could benefit from a balance between analog, digital, and DSP design all in a fast and automated RFIC design environment.

This paper presents RF design methodologies that can bridge between system, IC, and module design, providing an efficient, thorough design flow using advanced EDA tools.

I. Introduction

Today, one of the biggest obstacles in RF design is the interoperability between RF design domains as illustrated in Fig. 1. Simply, EDA tools for system, IC, and module, or package design do not link well with each other. This is because many tools were not developed together, and over the years became point-tools never migrating towards a complete homogenous design solution. Ideally, RF circuit designers would like to see one set of integrated EDA tools from system exploration to final module verification. Not having an integrated toolset has created barriers and confusion on how to best approach designing across the different disciplines. Adding to the problem, designs are becoming larger and more complex. Adding this with multiple chips in modules, with all the board-level components together, makes it difficult to achieve first-pass results without some manual effort and guessing. Often, it is an iterative design process with multiple passes because it is hard to anticipate all the interoperability problems and subtle circuit effects. This paper addresses some of the major issues facing RFIC design and EDA tool interoperability today with proposed solutions.

Descriptions of EDA tools mentioned at end of paper

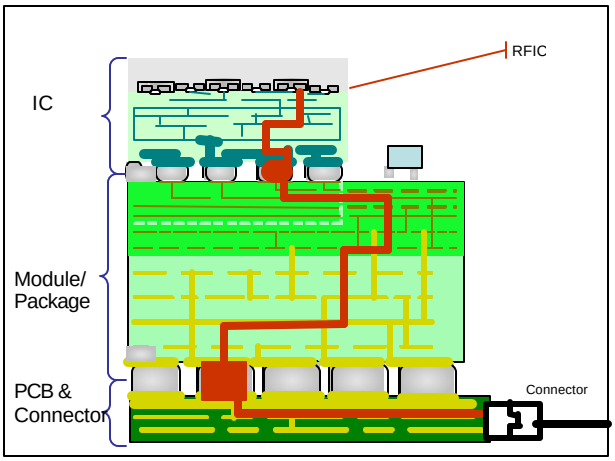

Fig. 1. Illustration showing that RF design crosses multiple design domains requiring EDA interoperability between domains.

II. System Design

From an RFIC designer's perspective, there needs to be a higher level of simulation and analysis iterating between IC and system design to preview circuit behavior in an application. The same is true for module and board-level design. Links between design domains are becoming possible with behavioral modeling and co-simulation. However, there is still no common EDA module design environment bridging RF system, IC, package, PCB, and prototype testing [1]. Within a few years, this gap is expected to close.

Wireless system design is done in a variety of ways. For well understood applications and small designs, the RF system design is sometimes skipped, or taken as an optional step, not linked back to IC or module design. This is a risky decision when a system is large and complex. For larger digital systems, a Digital Signal Processing (DSP) methodology is used and is effectively done with tools like SystemC, C/C++, and SPW. These tools are fast and efficient and can directly synthesize the RTL for a digital chip. This capability has been around for years. For analog and RF circuits, there is limited synthesis and it is mostly a manual effort to transfer a system architectural design to the IC world. However, system tools like SPW, Ptolemy, and others can create levels of abstraction that bridge the two

domains with behavioral modeling. But, translating models takes some work and requires a good understanding of modeling and the system itself. Co-simulation is the other option where system and IC simulators run separately by coordinating the simulation with handshakes.

System Architectural Modeling

System top-level architectural design is usually the starting point that establishes reference testbenches using synchronous data flow models. If done right, system design should be a foundation for the IC and module design that follow. System C, C/C++, spreadsheets, SPW, or Ptolemy are used to develop architectural models. Wireless signal sources and stimulus generators (e.g. CDMA, GSM, WLAN, Bluetooth, or custom-created ones), channel models, air interfaces and measurement blocks can simplify creating testbenches. In reality, module design with its package, passive components and ICs represent the system. Through behavioral models, system stimulus and measurement blocks can be exported from system to IC design. Measurement blocks from system level tests, such as eye diagrams, BER (Bit Error Rate) calculations, constellation diagrams, EVM (Error Vector Magnitude) plots can be recreated and used in IC design testbenches as shown in Fig. 2. These can then be correlated to IC specifications for circuit design. It is also possible to co-simulate from both domains system-level blocks with actual transistor-level views. This allows the preview of transistor-level performance in a complete system setting. Tools such as Ptolemy simulating in the RFDE (ADS running in Cadence) can make this possible. Also, with Ptolemy in ADS, it will be possible to push board-level testbenches up to RFDE and do time and frequency domain simulations. SPW (system design) and AMS Designer (analog mixed signal IC design) make it possible to do transient co-simulations. With transistor-level results, it is further possible to create accurate behavioral models and co-simulate these with system design.

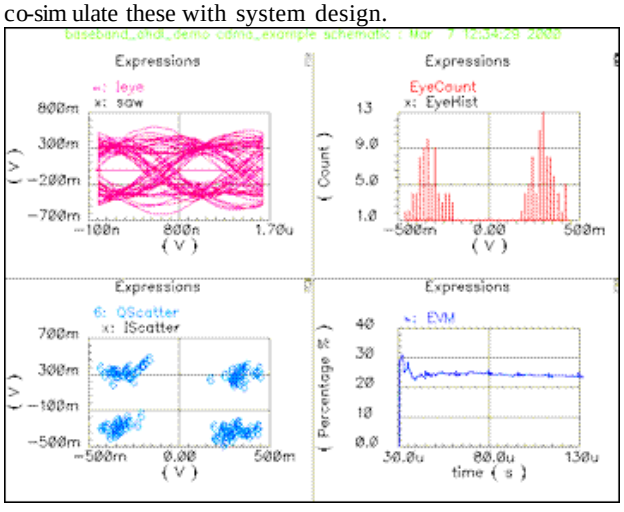

Fig. 2. Receiver system modeling: Eye, I/Q scatter, and EVM plots.

In IC design, using system testbenches, it is further possible to create more accurate behavioral models with Verilog, VHDL, Verilog-A/AMS, VHDL-AMS and C/C++. Board-level parasitics and discrete models in the form of S-parameter files allow a further ability to predict transistor-level behaviors at the system level. It is useful to examine LNA, mixer, filter and VCO performances for distortion as shown for a direct conversion receiver in Fig. 3. However, running system-like simulations, such as BER in IC design will require long transient simulations because it is only statistically accurate with thousands of cycles. For a large circuit this will take a long time and will take much longer if the circuit has difficulty converging. Noise specifications can be drawn from these results.

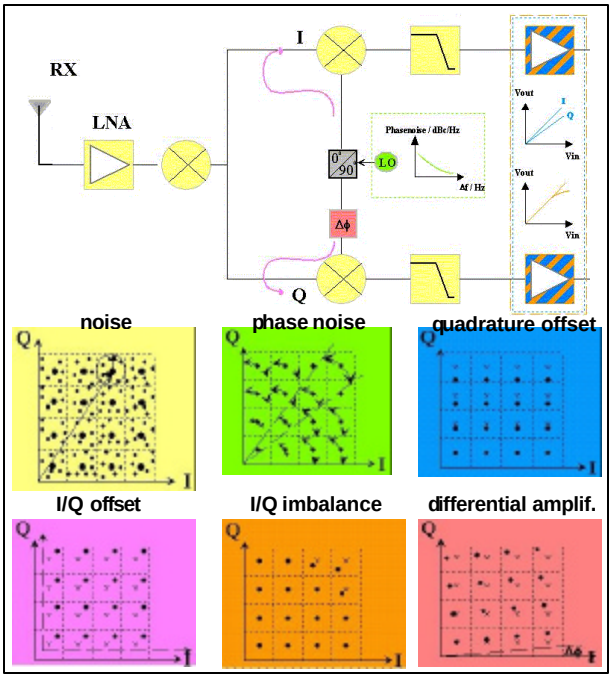

Fig. 3. RF behavioral models can capture non-ideal distortion effects in constellation plots of a direct conversion receiver.

III. IC Design

It is widely known that RFIC design is more productive if it is done in a top-down hierarchical manner. If a complete design hierarchy is mirrored from system to IC design, it allows co-simulations and multiple levels of abstraction to run forming a modeling bridge to system design. After verifying the design at the circuit level, layout and parasitic resimulation can follow. This approach is the basis of an accurate and efficient design methodology as shown in Fig. 4. The design methodology can be further enhanced and truly seamless if both system and IC design are in the same environment. Many engineers understand the value of top-down design, however it is not always practiced due to the perception that extra steps and cost are required that

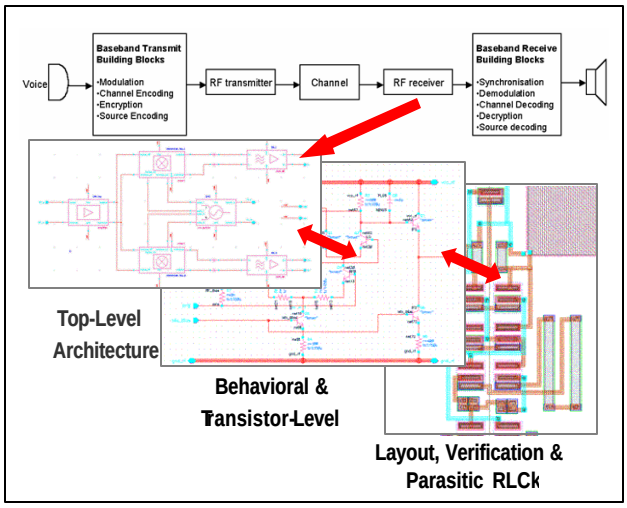

Fig. 4. RFIC design flow steps for a wireless communication system.

bottom-up methodology worked well in the past is sufficient for future designs. However, as complexity increases, this traditional design style will not likely be adequate and actually increase design time.

Once an IC specification is set and a semiconductor technology selected, chip floorplanning is done and there are automated analog mixed signal tools that can assist in the task. Nearly all designs done today are hierarchical, which helps use multiple levels of abstraction in simulation. This makes it easy to manage the design, especially when changes are required. RFIC design consists mostly of circuits that translate frequency, such as a receiver or transmitter. Traditionally, level-diagram analysis using spreadsheets has been used for design. The gain, linearity, and noise per stage are calculated to fit an overall budget. This is still an effective process and used often today but can be automated with behavioral models and later commingled with transistor-level, parasitic extracted-levels and fitted behavioral models to simulate in a top-down to bottom-up fashion as shown in Fig 5.

Many new circuits today are based on older designs, readapted, and improved. This is an evolutionary technique, leapfrogging a proven design into something new. How design reuse libraries are managed is important for productivity. Fitted behavioral models created from transistor-level results are very helpful in a re-use library strategy by providing a fast and accurate way to start a new design. The one drawback is that it takes planning and foresight to create and manage reuse. But, it can add a level of automation that will pay for itself over time.

A new RFIC design environment was developed with consideration to link system design and module design as shown in Fig 6. By itself, the RFIC design flow is comprehensive, including the most advanced set of tools and methodology to provide a fast and accurate flow. It is seamless from schematic capture to final verification.

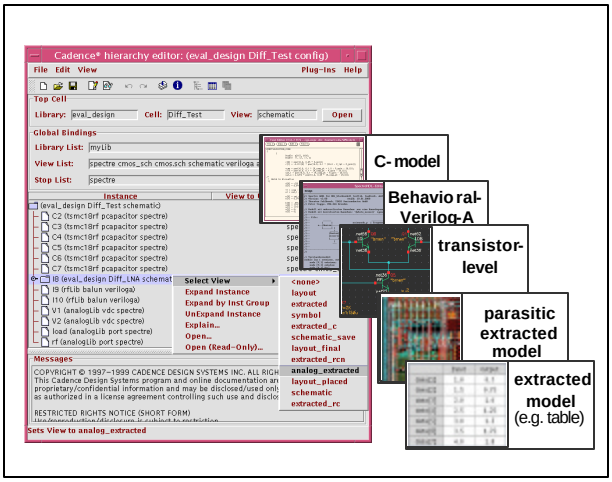

Fig. 5. Using a top-down to bottom-up design methodology.

An RFIC specification-driven design environment, which is tailored to the way a designer need to work, can combine the convergence and capacity of Cadence's Spectre and SpectreRF with Agilent's RFDE (ADS in Cadence) to provide the best time-domain and frequency-domain simulation solutions available.

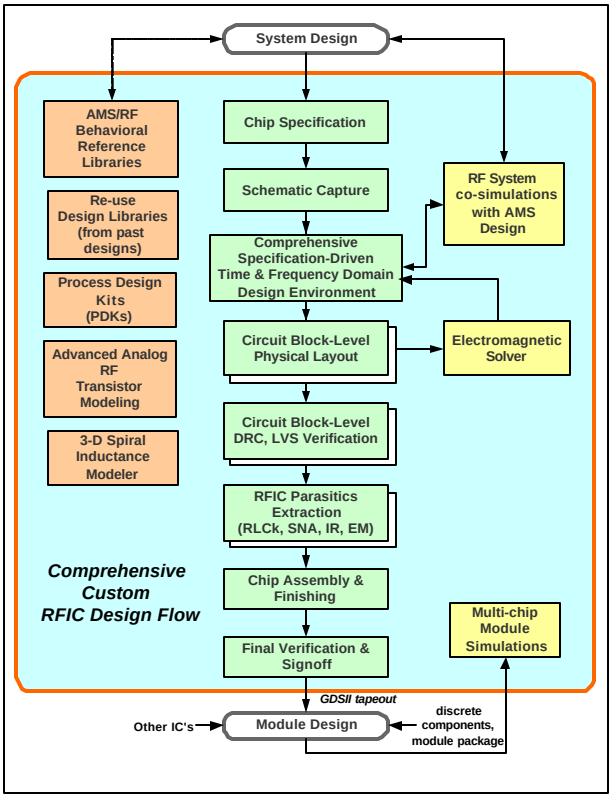

Fig. 6. Example of a comprehensive RFIC design flow bridging system, IC, and module design.

Tied with this is a full mixed signal simulator to do

top-level verifications and co-simulate with system models. Co-simulation is also possible with Ptolemy within RFDE.

Process Design Kits (PDKs)

Process Design Kits (PDKs) provide an essential link between the RFIC designer and the foundry. PDKs are fundamental to design productivity and essential to a seamless design flow. It binds together all the tools from schematic capture, simulations, physical layout, physical verification and parasitic extraction. The PDK is unique and is specific to the attributes of a particular semiconductor process. But, all PDKs are similar in appearance having libraries, cell, views and device categories. Most devices are parameterized and scalable; this is especially true for MOS devices. Layout can be connectivity-driven because the PDK links the device cells and schematic to layout in an automated fashion. For precision analog and RF circuits, there is layout connectivity from the schematic but it is necessary to have assisted compaction and routing to complete the layout. For analog and RF layout, much care and some hand crafting of the layout is required. Also associated with PDKs are device models and extraction rulefiles for DRC, LVS and parasitic extraction.

Specification-driven Design Environment

After schematic capture, all the simulations occur and must complement the way a designer thinks and needs to work. At this stage of the design process it is critical to foster common work practices and unify design reuse. It is rare for companies to have well defined IP disciplined design reuse practices that are used across the entire organization. Design reuse is often hit-or-miss. The Cadence specification-driven design environment (called VSdE, formerly Aptivia) is new and a design documentation and verification environment that unifies design reuse practices; it at is the heart of the design flow. A good simulation capability is important because RF design has to deal with a complex set of analog and RF simulations. RF design requires not only AC and transient simulations, it also requires simulations of harmonic behavior as well. Typically, RF simulators should have the standard SPICE-like capabilities of other analog simulators (transient, DC, and AC), but also the capabilities of S-parameters, harmonic balance (HB), envelope following and convolution. Standard wireless testbenches, especially with system co-simulation capabilities, add an extra dimension that allows for rapid setup and complete circuit verification within the system.

The availability of system level testbenches is important for functional verification of designs in order to preview distortion effects from transistor-level circuit blocks back to the system testbench since the distortion due to single tones and modulated signals are not the same. Also, co-simulations can bring board-level testbenches back to be simulated with IC's. This is especially important for previewing board-level frequency-domain effects with a harmonic simulation.

A specification-driven simulation environment allows for an automated way to simulate an established set of tests similar to batch processing. This would include running batch simulations to verify the specification limits; over corners with variations of supply voltage, temperature, and process parameters, as well as, Monte Carlo analysis, generated fitted behavioral models, generation of design review documentation and creation of a design archive.

RFIC Transistor Modeling

High frequency simulations for RFIC design often require additional modeling beyond the standard Gummel-Poon for bipolar, or BSIM3V3 for MOS. Additional RF subcircuits models are required that model the substrate and terminal RLCk (Resistance, Inductance, Capacitance, and mutual inductance) effects as shown in Fig. 7. This presents extra overhead when simulating RFIC designs. Often, these modeling subcircuits are used on a selective basis only. Of special importance, there is an interest in addressing more detailed inductance and capacitive coupling in transistor models. This allows simulations to come closer to the real frequency characteristics. It is possible to use transistor models with subcircuits to model frequencies into several GHz. For RF MOS transistors, this has been done with BSIM3v3, BSIM4 and BSIMSOI models. The standard BSIM3v3 models do not model gate resistance, lead inductance or substrate resistance. It has been shown that the resistance on the gate electrode influences the input reflection (S11) and the substrate resistance affects output reflection (S22). BSIM4 models include gate resistance, but, like BSIM3v3, lacks complete the scalability, especially for substrate resistance, needed for RF design. With some dedicated work, the Rgate, Rs, Rd and the substrate network can be scalable to device W and device finger number. A scalable model is needed for optimizing the design and the designer should realize the scaling is not linear [5].

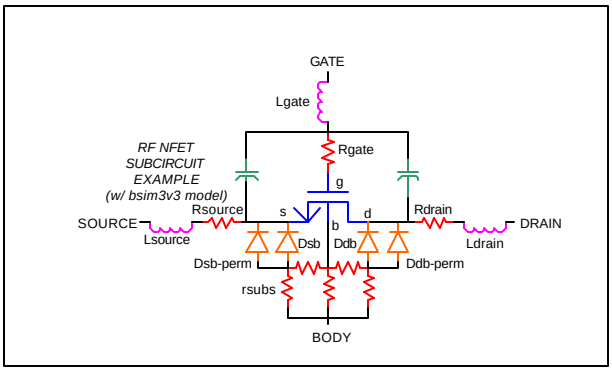

Fig. 7. Example of RF NMOS BSIM3v3 subcircuit model

Passive devices in RFIC

Today, RFIC circuits commonly incorporate passive components such as spiral inductors and transformers on-chip for filters, gain-boost, and balun transformers. The trend is to move as many passive components on-chip as possible. With design architectures such as zero-IF or low-IF receivers this is possible. This reduces the overall cost of a wireless system by eliminating expensive filter components such as surface acoustic wave (SAW) filters which are commonly used in traditional heterodyne architectures.

Over the last several years, the trend has been to integrate more passive components and it is now common to see the RFIC die area dominated by passive devices. With the advanced semiconductor processes today, whether it is SiGe BiCMOS or CMOS, there are 5-6 metal layers with dielectrics, plus a number of parameterized inductor shapes and geometries available. Multiple metal stacks are becoming common and allow for more creative inductive elements. While making those devices involves simply designing shapes on a layout carefully without violating design rules, these devices are used in a rather conservative fashion and sometimes reluctantly, due to the severe lack of reliable and silicon-proven models. As a result, silicon tests are required to iterate towards a solution. This is often a time consuming process that requires experience in sizing and placing inductors. As a consequence, there is a great deal of reluctance in the design community to use devices such as transformers which are really commingled inductors that are mutually coupled.

Multiple inductors with large areas present another problem. The inductance and Q of an inductor is strongly affected by mutual coupling from other inductors and metal traces nearby. Without knowing how close to place inductors, it is necessary to guess the best spacing. Closer spacing saves die area, but runs the risk of upsetting the L and Qmax causing a stability and oscillation problem in the circuit. On the other hand, spacing too far apart wastes die area. The typical on-chip inductor is 1 to 5nH which, if well targeted, has a Q of around 10. A typical size is 300um x 300um, easily making it the largest device on-chip. An example of optimized spiral inductors in a LNA design is shown in Fig. 8.

Since 1990, there has been intense and extensive research on silicon passive device modeling in hopes of generating accurate models quickly and even optimizing certain restricted devices [6]. Those efforts only result in limited success largely because in order to make the algorithm and tool interactive, they rely on quasi-static approximation [7]. The quasi-static method uses lumped elements to approximate the electromagnetic behavior of the device. A model can be as simple as several essential elements such as in a simple p i model; it can also become extremely complicated in order to approximate the skin effects, substrate loss, reduction of inductance by eddy current, etc. The complexity can quickly grow out of control when one wants to model the strongly coupled transformer. The typical use of these quasi-static methods is to develop a set of models that are well characterized against measurement. While such models may not easily extend to different processes, they offer somewhat acceptable predictability for designers to quickly generate similar passive devices.

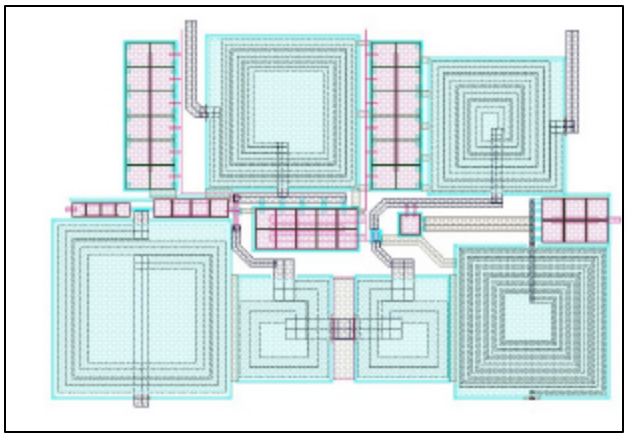

Fig. 8. Optimized LNA design for L and Qmax with 6 closely spaced spiral inductors. *Courtesy Helic S.A., Athens, Greece*

The general consensus is that true 3D electromagnetic (EM) simulation provides the best accuracy to simulate high frequency effects, such as skin, substrate effects and resonant frequency. 2.5D EM analysis takes advantage of the planar structure to make the simulation more efficient, yet its lack of good treatment of conductor thickness makes it prone to errors especially for specially formulated silicon processes. 3D EM analysis eliminates such restriction, but its prohibitively long simulation time makes it less appealing.

One should not take for granted that EM simulation is automatically better than quasi-static methods. While the basic principles of EM simulation are universal, the accuracy of results heavily depends on the input data that are fed into the EM simulator. Narrowing down the input data range to make the EM simulator more predictable is a procedure called “calibration” in which EM results are compared to measurement and input data are adjusted to make the results more comparable. An accelerated version of EM tool is thus desirable in order to make this procedure more efficient.

In the near future, fully capable fast 3-D EM solutions will be available that will make it possible to accurately model inductance in a much shorter time. This is possible by understanding and simplifying the models in a switchable fashion in areas where simulation time is significant but there is little contribution to an overall effect. An overhaul of traditional EM methods is required and indeed feasible.

An IC spiral inductance modeler is needed early in the design process before physical layout. A designer requires this information during schematic capture so he can preview the various styles of inductors and check on the L and Q rolloff. A well-developed PDK with parameterized commonly-used inductor cells can facilitate this preview. This capability reassures the designer that the design is ready to go into physical layout. This saves time iterating the design at layout. Even before layout, the designer can also review mutual inductance effects from nearby inductors. This will allow previewing different layout scenarios. The hope is that the inductor is well targeted early in the design phase before layout. This may save having to change the design during final chip verification. Inductor changes and re-positioning at final check can seriously impact the design cycle time.

Other passive components, such as resistors, capacitors and varactor all need to be modeled. The model must predict reasonable Q at high frequencies. To design without considering this finite Q will result in unrealistic simulation. Scalable models can still be extracted after on wafer measurement of the test structure.

PDK is also very important when the final RFIC layout must go through physical verification, such as DRC, LVS and parasitic extraction/simulation. A well-designed PDK must include the capability to simulate the RF mutual couplings among passive devices and interconnects, including the substrate coupling effects. When PDK does not have this capability, it is the designer's responsibility to ensure the subtle coupling and noise issues are well addressed in the design phase.

Physical Layout Parasitics & Substrate Noise

Layout parsitics are probably one of the most important aspects to be included in RFIC circuit simulations. Without parasitics, the simulations will be wrong. It is possible to selectively extract different combinations of parsitics: R, C, RC, RCL and RCLk (k represents mutual inductance). For analog design, extracting RCs works well to provide accurate results to silicon. But for analog RF, that is not good enough. High frequency design must account for inductive effects, including mutual inductive effects as well. In a RFIC flow, there are electromagnetic extraction tools for specialized purposes. For full chip RLCk parasitics, Cadence's AssuraRF can be used. AssuraRF, which is a quasi-static solver, is faster than the conventional full wave EM solvers and has shown to give good accuracy to silicon. Through Assura's unique process rulefiles, it is possible to do full RCLk extraction and resimulation in a reasonable timeframe if a parasitic reduction technique is used. For transient verification, a fast SPICE simulator such as Cadence's Ultrasim can be used.

Substrate noise is another important effect for RFIC design. An RF circuit often has sensitive inputs, such as the LNA input of a direct conversion receiver that if coupled with noise from other parts of the circuit could cause DC offsets resulting in anomalous performance. Cadence Substrate Noise Analysis (SNA), can accurately model the substrate RC mesh, and then, by adding noise stimulus from other parts of the circuit, especially digital circuits, VCOs and drivers can simulate the effects of these noise sources coupling through the substrate. This has been shown to be a very effective and important tool for RFIC receiver design to consider.

IV. RF Modules

RF module, or System-in-Package (SiP) design, is important today because it provides the most cost effective solution for RF packaged solutions as shown in Figs. 9 & 10. Monolithic SoC design, while important for variety of AMS applications, does not offer the performance or cost advantage for RF module design. Development time of SoC large chips is often longer, costly and does not necessarily have optimum circuit solutions. Module design is flexible and can combine a variety of optimized components and chips into one system. Multiple ICs can be CMOS, SiGe BiCMOS, and GaAS. Also, it is possible to stack die on top of each other, saving space and providing a smaller footprint. This has also shown to have good yields and is the most effective solution for RF systems. Today, most modules use a LTCC (Low Temperature Co-fired Ceramic) substrate. This allows for smaller geometries (line width, via sizes, etc.) and embedded components such as baluns, inductors, filters and capacitors [9].

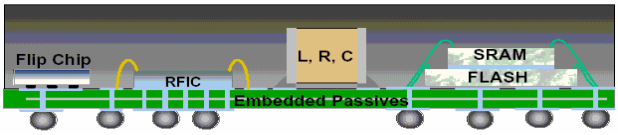

Fig. 9. RFIC in a complete System-in-Package (SiP)

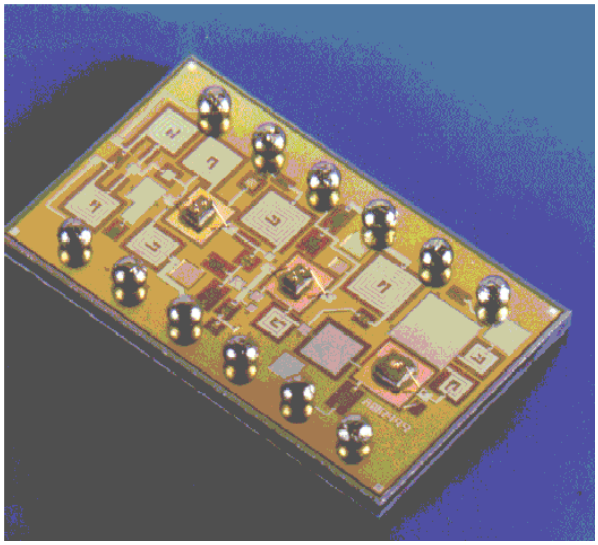

Fig. 10. System-in-Package (SiP) module

SiP and IC design sharing common schematics

The basis of a good module design is to use a common schematic capture environment with IC design and to link to advance package tools, such as the Cadence Advanced Package Designer (APD). This allows simulations to run in the IC environment with a combination of Spectre/SpectreRF or RFDE, or other simulators. Discrete component synthesis can also be done with board-level components like off-chip inductors and transformers. For more complex structures, EM solvers such as APE (3D), Momentum (2.5D), or HFSS (3D) solvers can be used to extract s-parameters, or netlists and then simulate in a common environment. The SiP design flow is shown in Fig. 11. Essentially, APD is linked back to the RFIC design environment for common schematics, shared libraries, and some simulations. For more package related simulations, these are export back to APD for those analyses.

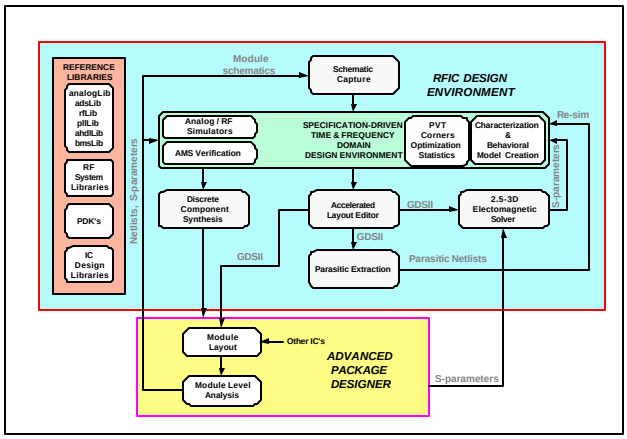

Fig. 11. System in Package (SiP) Design Flow

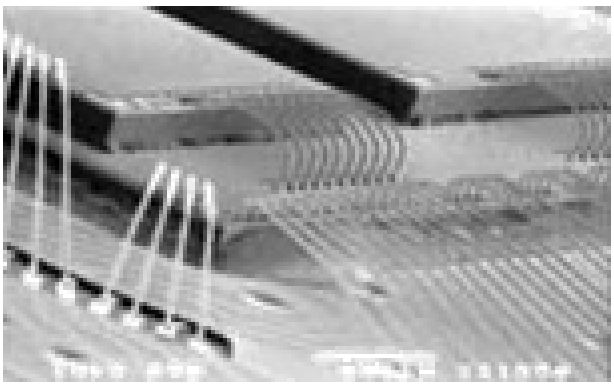

Fig 12. Module "stacked die" design

Along with SiP modules, "stacked die" offers similar opportunities and can be combined in a SiP module as shown in Fig. 12. This accomplishes a similar concept but by combining different chips and stacking them together.

V. Advanced Custom Design

The design ideas presented here can be assisted by the Advanced Custom Design (ACD) methodology in the Cadence Virtuoso custom design platform as shown in Fig. 13. Within this methodology, there are six design flows: Analog Mixed Signal, RFIC, System-IC, Custom Digital, Memory & Arrays, Chip Integration, and Silicon Accuracy. The RFIC flow as discussed in this paper is fundamentally connected to the System-IC flow and is based upon the Chip Integration and Analog Mixed Signal flows.

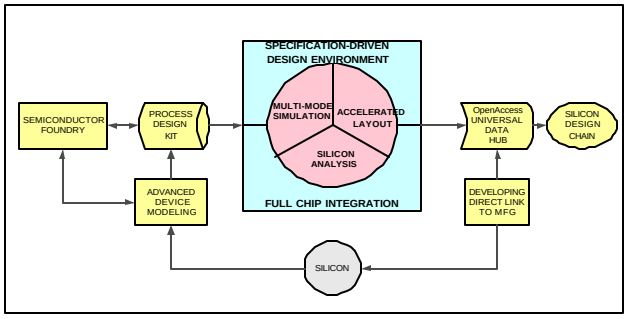

Fig. 13 – Example of a custom design platform: a fast and accurate complete AMS/RF design methodology

The key concepts of the platform on which the flows are based are: silicon accuracy, managing design collateral, fast top-down design, silicon-accurate bottom-up design, and mixed-level continuous design evolution. It supports what is called "meet-in-the-middle" approach as shown in Fig. 14.

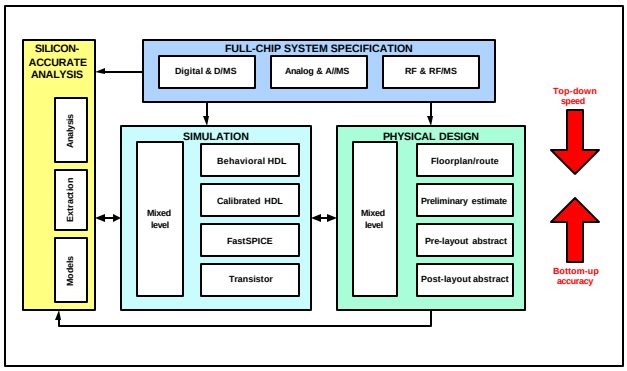

Fig. 14. The meet-in-the-middle approach

VI. Summary and Conclusion

While EDA interoperability has improved over the years and there are workable solutions for RF design across the system, IC and module design domains, further effort is needed to make a seamless design environment a reality. With interoperability initiatives such as *OpenAccess* (common database), such a design environment will likely become a reality in the near future.

It has been shown that through connecting the design domains *behavioral modeling* and a *common design environment* can significantly bridge the interoperability issues. However, changing the old habits of system, IC and module designers may be more difficult. They need incentives to change their work practices to work closer together and use common tools. However, until a wider adoption of behavioral modeling in IC design is accepted, the progress toward this goal will take some time. Larger and more complex designs should help make this transition and foster change.

Even with interoperability solved, there are still issues to solve within each design domain, such as extracting parasitics in the IC domain and better RF inductor and transistor modeling. Without question, accurately capturing and including parasitics in simulation is the number one issue for RFIC designers. Without accurately including parasitics in simulations, you might as well assume your results will be wrong.

Module design, while cheaper than large chip SoC design, has similar issues such as accurate device synthesis and simulation of the complete system. Multi-chip simulations with board-level components, while possible, can make it difficult for a simulator to converge on a result.

Acknowledgements

I wish to thank Jinsong Zhao of Lorentz Solution, Inc. who provided insight into the issues of electromagnetic analysis and RFIC transistor and inductor modeling.

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Descriptions of EDA tools mentioned:

SystemC	Broadly supported C++ open source language and simulator for modeling electronic design
Agilent Technologies	
ADS	Advanced Design System (RF design environment)
Ptolemy	System data flow simulator in ADS
RFDE	ADS running inside Cadence environment
Momentum	2.5D electromagnetic field solver
Ansoft Corporation	
HFSS	3D electromagnetic field solver
Cadence Design Systems, Inc.	
AMS Designer	Analog mixed signal environment & simulator
Spectre	Full featured analog SPICE-like simulator
SpectreRF	RF extension to Spectre
AssuraRCX	RC parasitic extraction
AssuraRF	RLCk parasitic extraction
SNA	Substrate Noise Analysis
APD	Advanced Package Designer
APE	Advanced Package Engineer (3D EM solver)
VSdE	Virtuoso Specification-driven Environment
CoWare	
SPW	Signal Processing Worksystem (system design)