# MOSFET Modeling for RF-CMOS Design

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**Abstract— Requirement for an accurate RF-MOSFET model is increasing as the trend to higher operation speed continues. This paper addresses observed phenomena obstructing circuit performance in the RF operating regime. The origin of the phenomena as well as their modeling will be discussed.**

## I. Introduction

Though the RF MOSFET circuit is becoming realistic, the RF-circuit simulation is still a challenge due to many reasons. One important reason is the lack of model accuracy required for the simulation [1]. Demand for accurate prediction of non-linear device characteristics is also tough due to deficiency of sufficient knowledge including measurements. Another serious reason is that appropriate tools for RF designs are still lagging behind the demand [2]. A lot of progress has been made to catch up the requirements in both the modeling aspect and providing simulation tools. Here our discussion focuses on the modeling aspect.

## II. Model Requirements

Accurate circuit simulation is becoming more serious due to two ongoing fabrication-technology developments, namely, the down scaling of MOSFETs into the sub-100nm regime and system integration with many functions on a single chip, which are prerequisite for RF circuits. To assist in the development, the most important issue is to guarantee sufficient simulation accuracy and applicability for any advanced technology. Under high-frequency operation, non-linear phenomena such as distortion as well as carreir response delay become serious for reliable circuit performance prediction. Here all such device phenomena are demonstrated to be determined by carrier dynamics, which are in principle observed in the $I$-$V$ characteristics [3]. Thus, the importance of the accurate parameter extraction will be emphasized for accurate circuit simulation.

A better circuit model has less model parameters, without compromising accuracy. The model parameters should be connected to device parameters and should be measurable independently. To realize this concept model development trends to follow the device physics, namely to describe device performances with the potential distribution along the channel instead of applied voltages conventionally done d [4, 5, 6]. The self-consistent charge-based model with the surface-potential description will be demonstrated to offer the basis for successful performing the foreseeable challenges. Modeling approach will be discussed mainly with HiSIM (Hiroshima-university STARC IGFET Model), the MOSFET model developed according to this concept for the first time [7].

## III. Modeled Phenomena

Here phenomena to be modeled and their modeling approaches are described in three groups:

(A) Modeling of Basic MOSFET Characteristics
(B) Large-Signal Analysis
(C) Samll-Signal Analysis

The group (A) includes normal DC and AC characteristics of MOSFET, requires intensive model parameter extraction. The group (B) focuses on carrier dynamics under high-frequency operation in the time domain, which is often transormed to the frequency domain with the harmonic balance analysis. The most efforts are given for deriving the analytical description suitable for circuit simulation without sacrificing simulation expense. The group (C) is the special case of the group (B). The modeling is done with an equivalent circuit model, which requires extraction of the elements included in the circuit. It will be shown that the accurate modeling of DC characteristics and their parameter extraction is a key for the simplified equivalent circuit model.

### *A. Modeling of Basic MOSFET Characteristics*

Requirements for the modeling is that all measured $I$-$V$ characteristics have to be well reproduced. Their derivatives are also sensitive for RF applications [8]. Fig. 1 shows an equivalent circuit of MOSFETs including basic device elements to be considered. To derive anayltical description for the potential distribution along the channel induced by applied voltages, we introduce two approximations. One is the charge-sheet approximation assum-

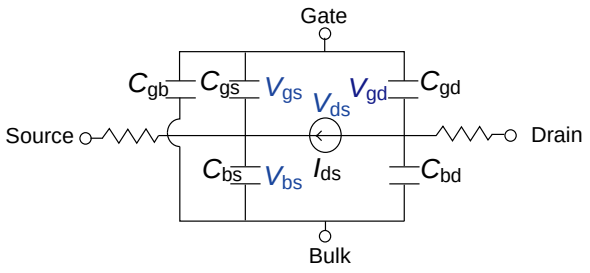


Fig. 1. Basic equivalent circuit of a MOSFET.

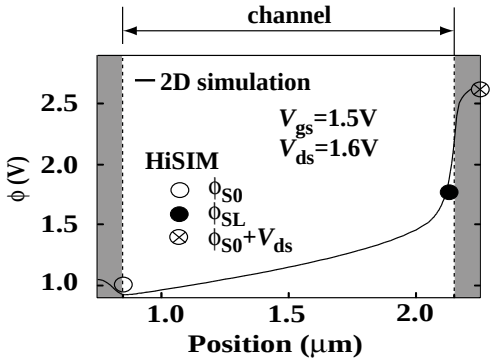


Fig. 2. Simulated surface-potential distribution along the channel with the 2D simulator MEDICI [13] under the saturation condition. Calculated surface potentials by HiSIM at the source side $\phi_{S0}$ and at the drain side $\phi_{SL}$ are also depicted.

ing zero thickness of the inversion charge, and the other is the gradual-channel approximation assuming smooth potential increase along the channel [9, 10]. These approximations allow to derive an analytical formulation for all device performances as a function of surface potentials at the source side $\phi_{S0}$ and the drain side $\phi_{SL}$ [11]. The surface potentials are obtained by solving the Poisson equation iteratively. In spite of the iteration the calculation time is not longer than with BSIM3v3 [12]. Fig. 2 compares the surface potential calculated by HiSIM with those of the 2D device simulator MEDICI [13], solving all device equations numerically. These values are very sensitive to device parameters such as the bulk impurity concentration. Calculated charges on the MOSFET nodes are shown in Fig. 3. These charges are origin of all device characteristics. By integrating the channel charge $Q_I$ with the velocity $v$ derives the current equation and their derivatives yield capacitances as depicted in Fig. 4.

The gradual-channel approximation is only valid for the non-saturative region. Beyond $\phi_{SL}$ the potentail increases steeply (see Fig. 2), forming the pinch-off condition. The model beyond the pinch-off point is depicted schematically in Fig. 5 [14]. Here an unknown value is the surface potential value at the junction between the channel and the drain contact $\phi(\Delta L)$. Unfortunately we cannot solve both the pinch-off length $\Delta L$ and $\phi(\Delta L)$ at the same time. The parameter $CLM1$ is introduced to determined the potential value in HiSIM [15]

$$\phi_S(\Delta L) = (1 - CLM1)\phi_{SL} + CLM1(\phi_{S0} + V_{ds}) \quad (1)$$

which is dependent on the junction condition, and is fitted to measured channel conductance $g_{\rm ds}$. Beyond the pinch-off region it is practically treated that the channel is shortened by $\Delta L$, as refered as the channel-length modulation. The whole potential distribution from $\phi_{S0}$ to $\phi_{S0} + V_{\rm ds}$ via $\phi_{SL}$ and $\phi(\Delta L)$ is the measure applied in the modeling.

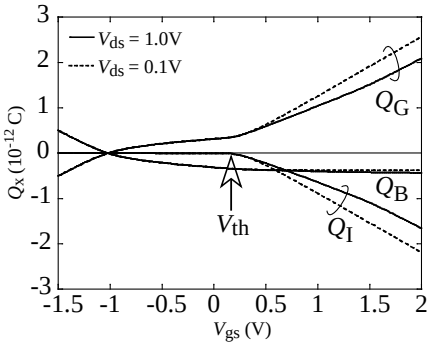


Fig. 3. Calculated charges induced in the gate ($Q_G$), in the bulk ($Q_B$), and in the inversion layer ($Q_I$) as a function of the gate voltage $V_{gs}$.

### A.1 *I-V* Characterisitcs & Their Derivatives

The final drain current ($I_{\rm ds}$) is written as

$$\begin{aligned} I_{\rm ds} = \frac{W_{\rm eff}}{L_{\rm eff}}\frac{\mu}{\beta}\Bigg\{ & C_{\rm ox}(\beta V'_G + 1)(\phi_{SL} - \phi_{S0}) \\ & - \frac{\beta}{2}C_{\rm ox}({\phi_{SL}}^2 - {\phi_{S0}}^2) \\ & - \frac{2}{3}\sqrt{\frac{2\epsilon_{\rm Si}qN_{\rm sub}}{\beta}}\Big[\big\{\beta(\phi_{SL} - V_{\rm bs}) - 1\big\}^{\frac{3}{2}} \\ & - \big\{\beta(\phi_{S0} - V_{\rm bs}) - 1\big\}^{\frac{3}{2}}\Big] \\ & + \sqrt{\frac{2\epsilon_{\rm Si}qN_{\rm sub}}{\beta}}\Big[\big\{\beta(\phi_{SL} - V_{\rm bs}) - 1\big\}^{\frac{1}{2}} \\ & - \big\{\beta(\phi_{S0} - V_{\rm bs}) - 1\big\}^{\frac{1}{2}}\Big]\Bigg\} \quad (2) \end{aligned}$$

$$V'_G = V_{gs} - V_{fb} + \Delta V_{th} \quad (3)$$

where $W_{\rm eff}$ , $L_{\rm eff}$, $\mu$, $\beta$, $C_{\rm ox}$, $\epsilon_{\rm Si}$, $q$, and $N_{\rm sub}$ are the channel width, the channel length, the carrier mobility, the inverse of the thermal voltage, the gate capacitance, the silicon permittivity, the electron charge, and the bulk impurity concentration. The $V'_G$ includes the flat-band voltage ($V_{fb}$) and the short-channel effect

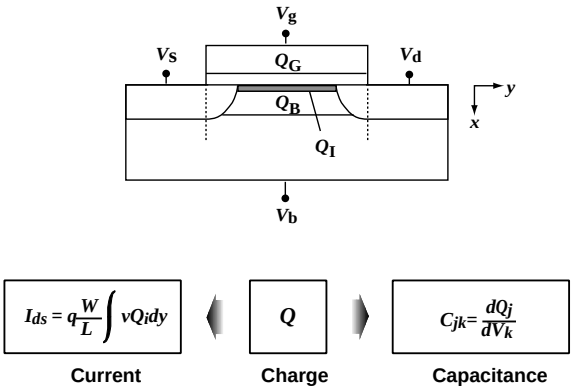


Fig. 4. Concept of the charge-based model.

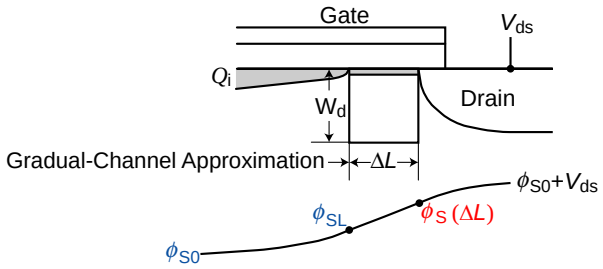


Fig. 5. Schematics depicting correlations among physical quantities in the pinch-off region.

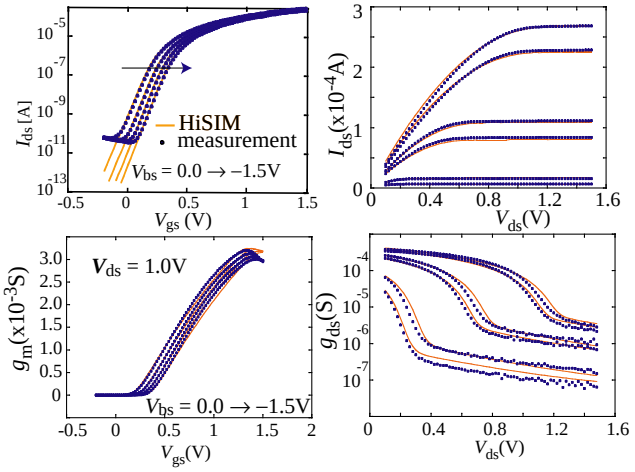


Fig. 6. Comparison of calculated $I$-$V$ characteristics and their drivatives with measurements. The gate length is fixed to 10$\mu$m.

($\Delta V_{th}$) discussed ib the next paragraph. If $\phi_{S0} = 2\Phi_B$ and $\phi_{SL} = 2\Phi_B + V_{\rm ds}$ are assumed, the $I_{\rm ds}$ equation reduces to the conventional description as a function of applied voltages. Calculated $I_{\rm ds}$ and their derivatives are shown in Fig. 6 in comparison with measurements. Since the surface potential description includes both the drift and diffusion contributions, the natural transition from the subthreshold region to the inverison region is achieved. In the subthreshold region, where the diffusion contribution dominates, the device parameters mostly determine the device characteristics. Under the inversion condition, where the drift component becomes important, the carrier mobility governs the characteristics.

**[Short-Channel & Reverse-SC Effect]**

The short-channel effect is caused by the lateral electric field increase along the channel. The Gauss law leads to the relation [16]

$$E_x + W_d \frac{dE_y}{dy} = -\frac{Q_s}{\epsilon_{\rm Si}} \tag{4}$$

where $y$ is the direction parallel to the channel, $E_y$ is the lateral electric field, and $Q_S = (Q_B + Q_I)$ is the total charge density induced in the substrate. $W_d$ is the depletion-layer thickness. For preserving the same amount of $Q_S$, fulfilling threshold condition, smaller vertical fields ($E_x$) are sufficient due to the additional contribution of the $E_y$ gradient. As the gate length $L_{\rm gate}$ reduces, the $dE_y/dy$ contribution increases. This is observed as a threshold voltage ($V_{\rm th}$) reduction. Thus the magnitude of $dE_y/dy$ is extracted from the $V_{\rm th}$ shift in comparison to a long-channel device, $\Delta V_{\rm th,SC}$. The surface-potential based model does in particular not require a $V_{\rm th}$ parameter in the MOSFET descriptions. For consistency, $\Delta V_{\rm th,SC}$ is included in the Poisson equation to calculate the surface potential change due to the short-channel effect.

In Fig. 7, the $V_{\rm th}$-$L_{\rm gate}$ characteristics shows $V_{\rm th}$ increases as $L_{\rm gate}$ is reduced. One important origin of the reverse-short-channel effect is the pocket implantation as shown in Fig. 8a. We assume a linearly changing lateral pocket profile along the channel as shown in Fig. 8b [17]. The $V_{\rm th}$ description is derived by determing the threshold condition from the entire carrier concentration in the channel analytically. Length of extention into the channel ($L_p$) and maximum concentration of the pocket profile ($N_{\rm subp}$) are extracted from the measured $V_{\rm th}$-$L_{\rm gate}$ dependence. Calculated $V_{\rm th}$ values are compared with measurement in Fig. 7. It has to be stressed that the impurity concentration is the model parameter, which influences all device characteristics such as the mobility through the surface potential values.

**[Mobility Model]**

The low-field carrier mobility is described by the following expression with three independent contributions [18]

$$\frac{1}{\mu} = \frac{1}{\mu_{Clmb}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} \tag{5}$$

$$\mu_{Clmb} = MUECB0 + MUECB1 \frac{Q_i}{q \times 10^{11}} \tag{6}$$

$$\mu_{ph} = \frac{MUEPH1}{(T/300{\rm K})^{MUETMP} \times E_{eff}^{MUEPH0}} \tag{7}$$

$$\mu_{sr} = \frac{MUESR1}{E_{eff}^{MUESR0}} \tag{8}$$

where $\mu_{Clmb}$, $\mu_{ph}$, and $\mu_{sr}$ are the mobility degradation due to the Coulomb scattering, the phonon scattering, and the surface roughness scattering, respectively. $MUECB0$, $MUECB1$, $MUEPH0$, $MUEPH1$, $MUESR1$, and $MUESR0$ are model parameters. The effective electric field $E_{eff}$ is descibed as

$$E_{\rm eff} = \frac{1}{\epsilon_{\rm Si}}(Q_b + \eta Q_i) \tag{9}$$

where $\eta$ is 1/2 for electrons and 1/3 for holes for normal MOSFETs. $MUEPH0$=0.3 and $MUESR0$=2.0 are known as the mobility universality [19]. Fig. 9 demonstrates that the extracted low field mobility preserves the universality, which is the proof of correct calculation of the charges $Q_b$ and $Q_i$ determining the effective electric field [20].

The high field mobility has been developed by Caughey and Thomas empirically as [21]

$$\mu = \frac{\mu_0}{\left(1 + \left(\frac{\mu_0 E_y}{V_{\rm sat}}\right)^{BB}\right)^{\frac{1}{BB}}} \tag{10}$$

where $V_{sat}$ is the maximum velocity, and has been measured $6.5\times10^6$cm/s [22]. However, the value exceeds with reduced $L_{\rm gate}$, called the velocity overshoot.

**[Quantum & Poly-Depletion Effects]**

The main phenomenon of the quantum-mechanical effect is the repulsion of the carrier-density peak into the substrate away from the surface. This can be modeled phenomenologically by increase of the effective-oxide thickness. Resulting effective oxide thickness is written [23]

$$\begin{aligned} T_{\rm ox,eff} &= T_{\rm ox} + \Delta T_{\rm ox} \\ &= T_{\rm ox} + \alpha\left(Q_{\rm b} + \frac{11}{32}Q_{\rm i}\right)^{-\frac{1}{3}} \\ \alpha &= \left(\frac{48\pi m_{\rm e} q}{\epsilon_{\rm Si}\hbar^2}\right)^{-\frac{1}{3}} = 3.5\times10^{-10}({\rm C\,cm})^{\frac{1}{3}} \end{aligned} \tag{11}$$

Here $\alpha$ is treated as a parameter due to the approximations applied to derive the equation. The extracted $\Delta T_{\rm ox}$ is compared with exact calculation solving the Poisson equation together with the Schoeredinger equation in Fig. 10. It has to be emphasized that $\Delta T_{\rm ox}$ is dependent on the gate voltage $V_{\rm gs}$.

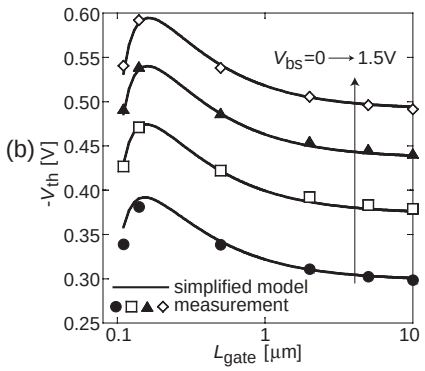


Fig. 7. Pocket implanted threshold voltage $V_{th}$-$L_{gate}$ characteristics. Calculated $V_{th}$ with HiSIM in comparison to measurements.

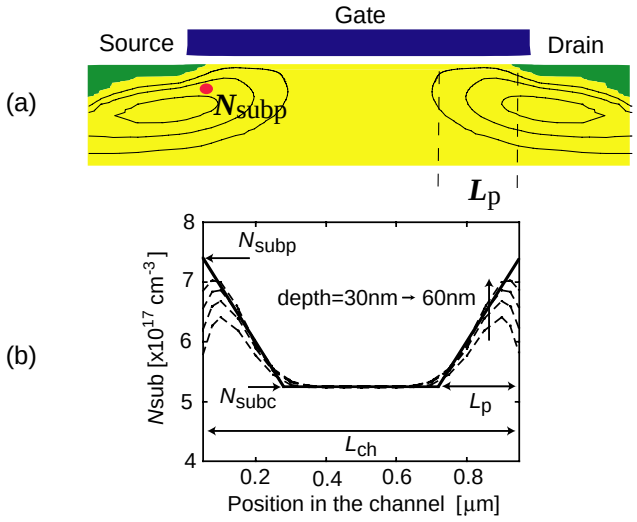


Fig. 8. (a) 2D-pocket profile obtained by the 2D-process simulator to reproduce measured $V_{\rm th}$-$L_{\rm gate}$ characteristics, and (b) its projection. $L_{\rm ch}$ is the channel length and $N_{\rm subc}$ is the substrate concentration.

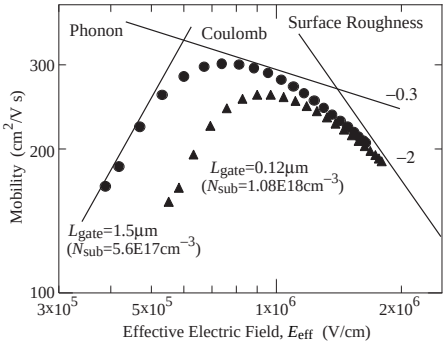


Fig. 9. Extracted low field mobility by HiSIM as a function of effective electric field.

Depletion in the gate poly-Si occurs due to the low impurity-concentration region in the gate-poly silicon at the gate-oxide simultaneously. However, the concentration is much higher than that in the substrate. Therefore the depletion starts after the formulation of the inversion layer in the substrate as shown in Fig. 11. Here one model parameter, namely the impurity concentration in the gate poly-Si $N_{\rm pg}$, is introduced [20].

Model parameters $\alpha$ and $N_{\rm pg}$ are extracted with measured gate capacitacne as a function of $V_{\rm gs}$ as shown in Fgi. 12.

## A.2 Intrinsic and Extrinsic Capacitances

Intrinsic capacitances can be derived directly from the terminal charges as depicted in Fig. 4. Explicit equations as functions of the surface potentials are obtained by de-

riving charges with respect to node voltages. The calculated 9 independent capacitances are shown in Fig. 13. They require no model parameter. In addition to the 9 intrinsic capacitances two important capacitances have to be modeled. One is the overlap capacitances. Especially the voltage dependent overlap capacitance, which are also derived as a function of surface potentials [15], strongly influences the RF performances. For short-channel transistors the gradient of the lateral electric field at the drain induces an additional capacitances $C_{Q_y}$ as shown in Fig. 14 [24]. This lateral-field-induced capacitance is modeled by inclusion of the lateral electric field increase in the pinch-off region shown in Fig. 5.

### A.3 Harmonic Distortion

If the model is consistent and all model parameters are accurately extracted from measurements, other measured quantities should be reproduced without any additional model parameters. The harmonic distortion is one of such object. Fig. 15 demonstrates the proof. The symbols are measurements and dashed lines are calculated result with the parameter set extracted only from measured $I$-$V$ characteristics. The solid lines show the result with tuned molibity value by 3%, which gives unobservable difference in the $I$-$V$ characteristics [25].

### A.4 Noise Characteristics

In RF systems, noise is a major issue obstructing circuit performance, which consists of usually small unwanted signals in a system in a different manner [2]. We focus on the noise induced in device. There are two important noise mechanism to be considered for advanced MOSFETs; the $1/f$ noise and the thermal noise. The origin of the $1/f$ noise has been understood theoretically as the fluctuation in the number of channel carriers due to trapping/detrapping processes at the gate-oxide interface, as well as by the mobility fluctuation. The final description of the noise spectrum density $S_{I_{\rm ds}}$ for the drift-diffusion

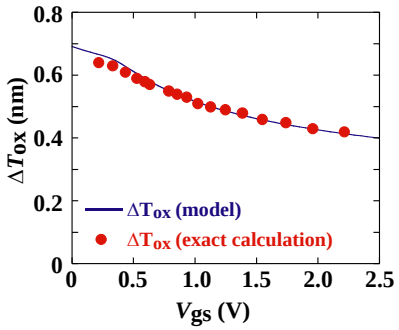


Fig. 10. Comparison of calculated $\Delta T_{\rm ox}$ with exact solution obtained by solving the Schroedinger equation and the Poisson equaion simultaneously.

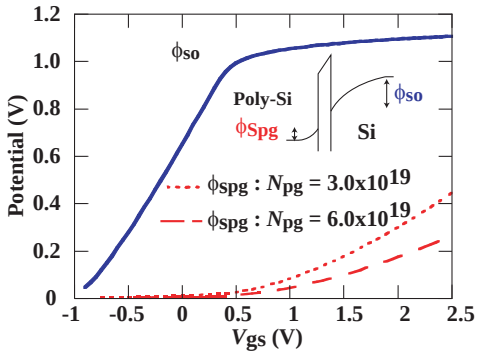


Fig. 11. Simulated surface potential at the source side ($\phi_{S0}$) as a function of the gate voltage $V_{\rm gs}$. The poly-depletion potential $\phi_{spg}$ is also shown for two doping concentration in the poly-Si, $N_{\rm pg}$.

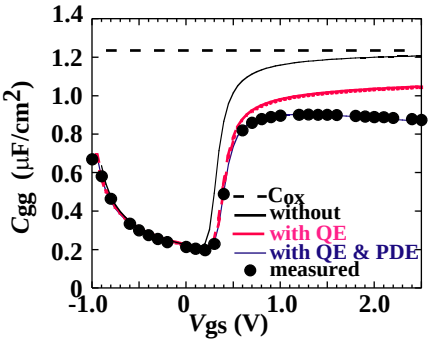


Fig. 12. Comparison of measured and simulated gate capacitance as a function of the gate voltage $V_{\rm gs}$.

model is [26]

$$S_{I_{\rm ds}} = \frac{I_{\rm ds}^2 NFTRP}{\beta f L_{\rm eff} W_{\rm eff}} \left( \frac{1}{Q_{\rm i}/q + N^*} + NFALP \times \mu \right)^2 \quad (12)$$

where $NFALP$ and $NFTRP$ are the contribution of the mobility fluctuation and the ratio of trap density to attenuation coefficient into the gate-oxide, respectively. $N^*$ is written

$$N^* = \frac{C_{\rm ox} + C_{\rm dep} + CIT}{q\beta} \quad (13)$$

where $C_{dep}$ is the depletion capacitance calculated with $\phi_S$, and $CIT$ is the capacitance caused by the trapped carriers, normally fixed to zero. Since the extracted $NFALP$ is usually nearly zero, the $1/f$ is mostly determined by the trap density $NFTRP$ and the carrier density in the channel. Fig. 16 compares calculated $1/f$ noise characteristics with measurements at $f = 100$Hz only with $NFTRP$ as a fitting parameter. Good agreement of the calculated $1/f$ noise to measurement for any applied voltages and any channel lengths demonstrates that the characteristics of the $1/f$ noise is determined mostly by the carrier concentration.

The thermal noise measurement is very severe to achieve accurate result. Only recently accurate measurements have been reported. The model is based on the

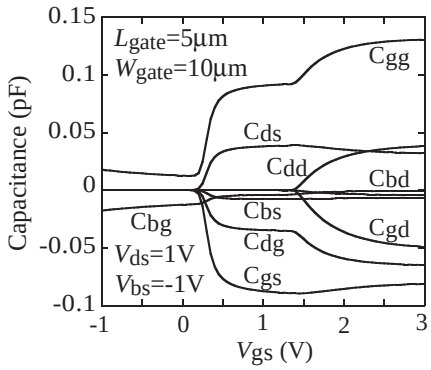


Fig. 13. Calculated 9 independent intrinsic capacitances as a function of the gate voltage $V_{\rm gs}$.

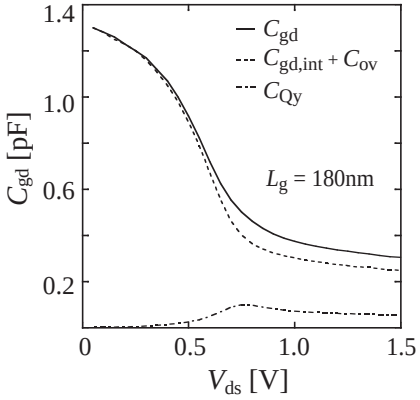


Fig. 14. Calculated lateral-field-induced capacitance, induced in the region where the high lateral electric field occurs [24].

channel conductance as derived by Nyquist [27]

$$S_{I_{\rm ds}} = \frac{4kT}{L_{\rm eff}^2 I_{\rm ds}} \int g_{\rm ds}^2(y)dy = 4kT g_{\rm ds0}\gamma \qquad (14)$$

Here $k$, $L_{\rm eff}$, $g_{\rm ds}(y)$, $g_{\rm ds0}$, $\gamma$ are Boltzmann's constant, channel length, position-dependent channel conductance, channel conductance at $V_{\rm ds} = 0$, and drain-noise coefficient, respectively. It can be seen from the desription, the thermal noise is dependent only on the channel conductance, thus no model parameter is needed again. The origin of the thermal noise enhancement observed for short-channel transistors is explained differently from different authors. HiSIM considers the potential distribution along the channel explicitly, reproducing measurements as shown in Fig. 17 [28]. Simulated noise coefficients are shown in Fig. 18, which justify the modeling approach and proves the consistency of the model. Thus the simulation result demonstrates that the model can be even exploied to predict the thermal nosie without difficult measurements.

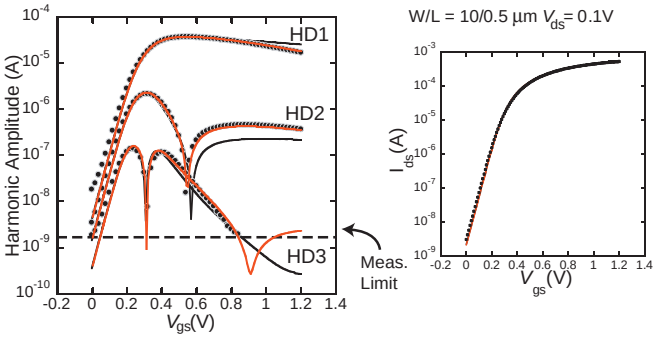


Fig. 15. Comparison of calculated harmonic distortion with measurements (dotted). The thick solid lines are results with a parameter set extracted from measured $I$-$V$ characteristics and the grey lines are with tuned mobility parameter. The difference of the parameter values cannot be seen in the $I$-$V$ characteristics.

### *B. Large-Signal Analysis*

Circuit simulators solve transient characterisitcs of cirucits in the form written as

$$I_a(t) = I_a(0) - \frac{dQ_a}{dt} \qquad (15)$$

derived under the quasi-static approximation, ignoring the carrier transit delay along the channel. $I_a(0)$ denotes the spontaneous current response to the applied voltage on node $a$ without delay. Till now the incorporation of the delay is carried out mostly phenomenologically by segmenting the channel into $n$ pieces, and each segmented MOSFET is recombined as can be seen in Fig. 19. This large-signal non-quasi-static model is shown to give a suitable prediction of the high-frequency behavior of the intrinsic device response [29]. Shortcomings are simulation time and simulation is not straightforward due to the segmentation of the channel. A more exact model have been developed including the real transit time as demonstrated in Fig. 20 [30]. The main effort is given to modify $Q_a$ in Eq. (15) including the carrier transit delay, which even represents the carrier deficit in the channel occurred at the initial stage of the switching-on without sacrificing the increase of the simulation time.

Harmonic balance simulation solves the semiconductor equations in the frequency domain thus enabling large signal sinusoidal simulation. Since the device is non-linear, integer-multiple combination of harmonics to the input frequencies are created. If we once have the accurate non-quasi-static model in the time domain, it can be easily extended to the harmonic balance simulation.

### *C. Small-Signal Analysis*

The small-signal analysis considers the case where input simusoudal voltage variations are sufficiently small so that the small output current variations can be expressed by a linear relation as [8]

$$\Delta I_{\rm ds} = g_{\rm m}\Delta V_{\rm gs} + g_{\rm mb}\Delta V_{\rm bs} + g_{\rm ds}\Delta V_{\rm ds} \qquad (16)$$

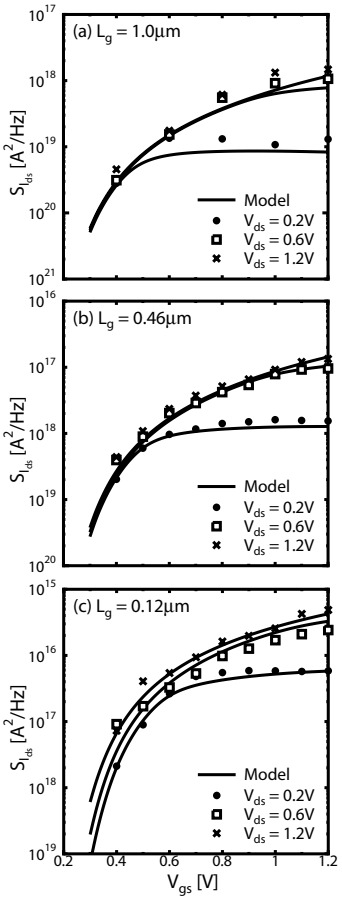


Fig. 16. Calculated $1/f$ noise characteristics in comparison with measurements. Only the trap density $NFTRP$ is the model parameter, valid for all gate lengths [26].

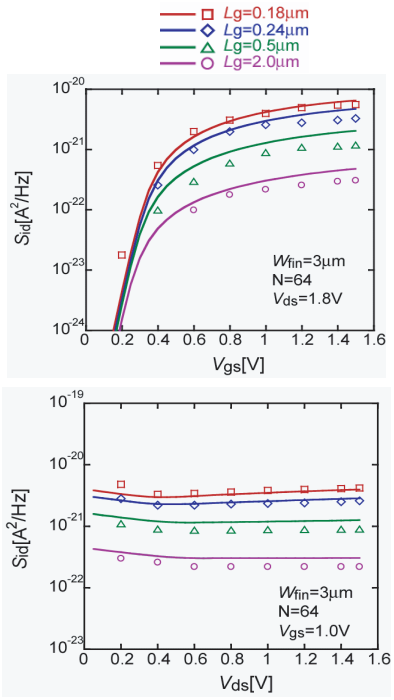


Fig. 17. Calculated thermal noise in comparison with measurements. For the calculation model parameters extracted only from measured $I$-$V$ characteristics are used [28].

where conductances $g$s' are derivatives of $I_{ds}$ with respect to corresponding node voltages. The small-signal analysis investigates the high frequency characteristics. The characterization is done with two $y$ parameters, the admittance matrix representing the carrier response. Calculated $y$ parameters are compared with measurements in Fig. 21. The calculations done with the QS model show clear deviations in the high-frequency regime. To improve the simulation accuracy caused by the non-quasi-static effect, additional elements are introduced in the equivalent circuit as shown in Fig. 22. The high Elmore resistance at the drain side $R_{gd}$ describes the carrier delay [31], and the bulk resistance $R_b$ describes the extrinsic capacitive coupling [32]. Calculation reuslts with the improved equivalent circuit are included in Fig. 21. Fig. 23 demonstrates the non-quasi-static contribtuon on the $y$-parameter values, where the external contributions are excluded [33]. The result shows that the non-quasi-static contribution is larger in the real part of the intrinsic $y$ parameters than the imaginary part. The non-quasi-static model is strongly required beyond the frequency of 1/3 of the cut-off frequency.

## IV. Summary and Conclusions

Observed phenomena obstructing RF-circuit application of MOSFETs and their modeling are discussed. Modeling based on the surface potential description preserves self-consistency among models of different device characteristics. Thus the conventional parameter extraction from measured $I$-$V$ characteristics results in accurate simulation results up to 1/3 of the cut-off frequency.

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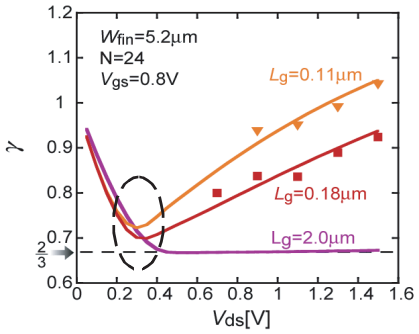


Fig. 18. Calculated thermal noise coefficients $\gamma$ and measurements as a function of the drain voltage $V_{ds}$ for various gate lengths $L_g$ [28].

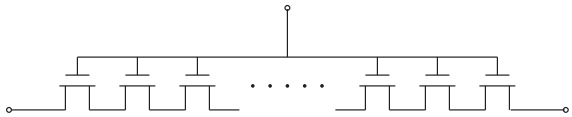

Fig. 19. Schematic of the channel segmentation model to describe the carrier delay in the channel.

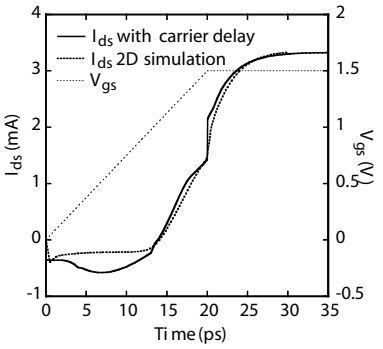


Fig. 20. Comparison of a calculated transient $I_{ds}$ behavior to a 2D simulation result under high switching operation [30].

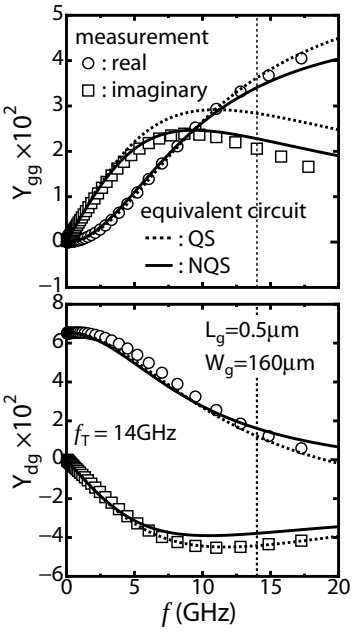


Fig. 21. Measured (open symbols) and calculated $y$ parameters with the non-quasi-static model (solid curves) and the quasi-static model (dashed curves) for the gate length of 0.5$\mu$m. The vertical dotted lines denote the cut-off frequency of the device studied.


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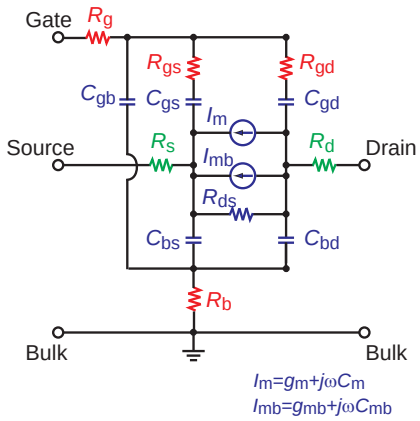


Fig. 22. Improved equivalent circuit for high-frequency applications. The Elmore resistances $R_{gs}$ & $R_{gd}$ and the bulk resistance $R_b$ are introduced.

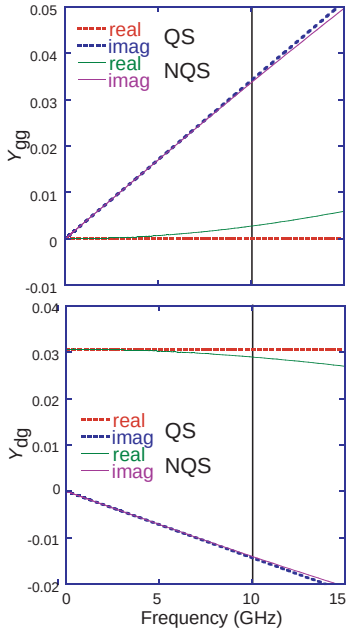


Fig. 23. Comparison of calculated intrinsic $y$ parameter values with the quasi-static model and the non-quasi-static model. The vertical solid lines denote the cut-off frequency.


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