Open Architecture Test System: not why but when!

Srimat Chakradhar
NEC Laboratories America, Princeton, NJ 08540

Abstract

Due to rapidly escalating semiconductor manufacturing test costs, leading consumers (chip manufacturers) are urging the ATE industry to identify new test systems and business models that can significantly lower test costs. We examine the shifting consumer needs and identify attributes of a test system that can effectively meet the requirements of the consumer. Open test systems have the potential to reduce test costs, but they also result in seismic changes in the ATE industry. We discuss the effect of these changes on consumers, incumbent ATE vendors and new entrants. We conclude that benefits of open test systems are now visible within leading ATE vendors, but an industry-wide open test system is necessary to realize meaningful cost reductions for the semiconductor chip manufacturer.

1 Introduction

Fabrication of chips involves a series of complicated electro-mechanical, lithographic and thermal steps. Like any other manufacturing process, chip fabrication can and does introduce physical defects into the manufactured product, the chip. Automatic test equipment (ATE) is used to test electronic chips, boards, devices and systems. The intent here is to ensure that *every* manufactured chip is free from manufacturing defects as opposed to *design verification* that attempts to uncover design errors introduced in the chip design phase.

1.1 Escalating test costs

For the past few decades, the semiconductor industry has managed every eighteen months to double the number of transistors in cutting edge ICs *without correspondingly increasing the cost of the chips.* For microprocessors, this periodic doubling translates into a roughly 100% increase in performance every year and a half, at no additional cost. Today, introduction of copper interconnects, submicron (0.13 micron and smaller) device geometries, and 300mm wafers ensure increased performance, functionality and significant yield improvements for chip manufacturers and their customers who incorporate these complex chips into myriad array of communications, computing and consumer products. *However, over the same period, the cost of testing a chip has largely remained steady.* Test costs now account for an increasingly larger proportion of the total chip cost. These complex chips place an increased pressure on the test process, forcing ATE suppliers to contend with higher research and development costs, increasingly complex manufacturing processes, novel hard-to-detect defect mechanisms, and rapidly shrinking market windows. If we continue to employ traditional test techniques to new emerging processing platforms, then within a few years, the chasm between test costs and design costs is expected to widen, with the cost of testing a transistor being estimated as 10 times the cost of fabrication [1].

Test costs consist of two components: (1) a non-recurring, one-time design cost of introducing design-for-test structures into the target design, followed by automatic or manual generation of test stimulus, and (2) a recurring cost that is incurred on *every* manufactured chip. In high volume chips, this cost easily overshadows the non-recurring component. During test application, test stimulus is delivered to every chip and the test responses are observed carefully to screen manufacturing defects. However, the two components are related. Clever design-for-test structures introduced in the chip design phase can drastically reduce test application time for each chip.

1.2 Shift in Consumer values

The use of ATE has steadily proliferated into the electronic manufacturing arena of consumer electronics, automotives, telecommunications, information technology, and medical equipment. Powerful market drivers, such as, the rise in internet-related communications, networking devices, digital signal processors, and microprocessors, have fuelled an explosive growth in the semiconductor industry. This industry, consisting of primarily the chip manufacturers, has been, and continues to be the largest end-use market for ATEs. In 2000, the telecom industry and information technology accounted for 72% of the ATE market, the consumer industry contributed 11%, automotive industry accounted for about 7% [2]. North America was responsible for 46% of the ATE market, with Asia Pacific and Europe contributing 37% and 12% respectively [2].

The cost of testing complex ICs and SOCs has reached the point where leading consumers (chip manufacturers), such as Intel Corporation, are telling test-equipment vendors in no uncertain terms that they no longer can continue business as usual. Test systems are too expensive, there are too many (often, incompatible) models offered by multiple vendors, and all the systems have proprietary architectures. Intel even outlined the architectural requirements for an open test platform and helped establish the Semiconductor Test Consortium [3] to lower test costs. Clearly, the consumer now values new metrics. The initial performance-dominated, proprietary test architecture phase of the ATE industry is giving way to a new era in which other factors, such as test system cost, scalability, technology-specific customization and instrument interoperability are features that customers are willing to reward with a premium. ATE industry players who recognize the shift in value proposition and introduce new products and services that may not be very high-performance solutions but offer other benefits like simpler, more general, more convenient and less expensive test solutions will emerge as industry leaders.

2 Open Test Systems

What are the specific attributes of a test system that can effectively address the shifting consumer values and lead to significant reduction in test costs? We discuss the major attributes and the anticipated benefits.

Design diversity: Chips range from simple consumer-product logic controllers to multimillion-transistor SOCs and multi-chip modules incorporating multiple technologies: digital, mixed-signal, analog and RF. Today, specialized test equipment is necessary for each technology, and trained test engineers who are intimately familiar with the test intricacies and idiosyncracies of each technology are indispensable. A single test system must support a wide range of applications from pure digital to SOCs with a wide variety of analog components.

Test diversity: The test architecture must support a wide range of applicability: from low-cost largely DFT-based (design for test) structural test platforms [4] to largely functional test-based platforms or any flavor in between. The DFT methodology enables cost-effective testing of large-volume commodity items with very short life cycles, like SOC devices. Some of these devices are on the shelf for only six months before becoming obsolete. Also, commodity large-volume consumer-oriented applications typically use a well-characterized manufacturing process, and DFT testing may be adequate. For very high-end leading-edge designs, functional and delay testing are more important. Therefore, a test platform that can be customized to have just enough capability for a specific target device under test is attractive.

Customer diversity: ATE industry caters to a broad array of semiconductor chip manufacturers: integrated device manufactuers (IDMs) to 'fab-lite' to 'fabless' companies and many flavors in between. Roughly, the semiconductor market has two sections: companies that design components, and companies that manufacture and assemble these components. Fabless refers to the business methodology of outsourcing the manufacturing of silicon wafers. These companies focus on the design, development and marketing of their products and form alliances with silicon wafer manufacturers, or foundries. The fabless model is an attractive and popular option for many semiconductor companies. By adopting a fabless business strategy, a company can focus time and resources on the design of innovative chips, while avoiding the high cost of building, operating, and upgrading a manufacturing facility. The implications on the ATE industry are clear. The test architecture must support a wide range of customer business models. Proprietary, high capital cost test systems are beyond the reach of most fabless companies. Scalable, build-as-you-go plug-and-play systems can effectively meet the needs of a diverse customer base.

Longevity and scalability: The test system is expected to enjoy a lifetime of more than ten years, without risking obsolescence. Therefore, an important objective is to devise an architecture framework that (1) protects and extends ATE investments, (2) allows continuing innovation and advancement in test technology to keep pace with dramatic advances in semiconductor processes and devices. Such an architecture allows the consumer to buy only what they need today yet upgrade the system to meet future needs. This requires that test functions that will change as technology requirements change be identified. For example, data flow, power management, alarm and error-handling strategy, and test parallelism aspects do not usually change with technology [7]. However, pattern rate, pin count, or edge-placement accuracy requirements do change with technology. This separation of functions helps to extend the test architecture with performance upgrades, as and when necessary, without the need for retooling. Nevertheless, the ability to scale entails some software and hardware overhead.

Open architecture: A test system consists of several parts: hardware, software and interfaces. In an open architecture, all parts of the test system are well documented and the parts are available on a non-compete and non-discriminatory basis from any ATE vendor. For example, the Semiconductor Test Open Architecture initiative's charter is to publish the architecture, provide training programs and workshops to ensure it is truly open, to identify requirements, develop solutions, define and manage validation procedures to ensure full vendor interoperability [3]. An open architecture allows configuration flexibility along the lines of a PC to greatly extend the lifetime and dramatically lower the cost of the test system.

A well designed open architecture results in compelling benefits to the consumer: the semiconductor industry. However, the specific components of a test system that must be made open to ensure the longevity and success of an open architecture are not always clear. Should we make open the test socket, the tester architecture, the tester language, EDA software, and so forth? For example, test data implementation can use XML, a license-free, platform independent standard, and test methods can be implemented using Java, an open and platform independent interpretive/compiled language [5]. This new representation for test program structure forms the basis of the new software architecture that is implemented in a new tester from NPTest [6]. A test system has many components and it is certainly possible to make all components open. However, there is a tradeoff between openness, cost and usability of the test system. Identification of a few major sub-systems that hold the promise of significantly reducing the overall costs, without adversely affecting the extensibility or application range of the test system is critical but not always easy [7].

3 Open systems change the ATE game

An Open Test System, like any other system, consists of several components. Different components will be made by different ATE vendors using very different production and business models. Truly open, interoperable test architecture allows chip manufacturers to implement flexible ATE solutions that meet the diverse test needs in a cost effective manner. Overall, such a system changes the dynamics of the ATE industry.

Expanded user-base: Open systems enhance compatibility and interoperability and generate greater value for the users by making the consumer base larger. They make it easier for consumers to share test information with other consumers as well as ATE manufacturers, and promote test reuse in SOCs that use common IP components. Today, some chip manufacturers do make their own ATE, using off-the-shelf, rack-and-stack components. However, this has been the exception, rather than the rule, especially in today's increasingly fabless chip industry. Going forward, Integrated Device Manufactuers (IDMs), particularly those that follow a fab-lite business model, may find this option attractive.

Changing nature of competition: ATE vendors must now focus not only on their competitors, but also on their collaborators. Forming alliances, cultivating long-term partners and ensuring compatibility are critical business decisions. The history of Microsoft-Intel partnership is a good example of the complex dynamics that arise in assembling information systems. Neither software or hardware is of much value without the other. They are valuable only because they work together as a system. In contrast, Apple Computer pursued a less successful strategy of producing both hardware and software platform of the computer system.

Move to component competition: The locus of competition shifts from systems to components. Specialists tend to thrive in the mix-and-match environment created by open interface, hardware

and software standards. Generalists and system integrators usually thrive in the absence of compatibility. Open architecture facilitates sharing of R&D effort of all ATE vendors and advanced modules can be brought to market much quicker.

Reduced technology risk and lock-in: Open systems reduce the technology risk faced by chip manufacturers. With competing proprietary architectures, battle to win market share can undermine consumer confidence. As each ATE vendor strives to convince consumers that it will be winner, consumers may take the easy way out: sit on the sidelines and use older technology that is available and stable. Today, lock-in to proprietary test architectures is common place. However, inteoperability in open systems lowers switching costs and consumers can largely avoid lock-in.

Competition on price: Open systems shift competition away from features toward price. This is because features are common across all brands. Depending on how open the system is, the harder it is for ATE vendors to differentiate their product and still be in compliance with the open architecture.

Interconnection problem: Instrument vendors are inherently vulnerable to competitors who manage, update and control the open test architecture. This is similar to the case where Netscape's browser (a component in a larger system)had to work within its chief competitor's (Microsoft) operating system infrastructure.

4 Open wars

Today, the $3 Billion to $5 Billion ATE industry is being served by a large (40 to 50) number of different architectures. In some cases, different systems produced by the same vendor are often incompatible. This has caused an unhealthy market fragmentation. Every one of these architectures is solving the same set of problems, in a marginally different but not necessarily better way. Each of these architectures is proprietary, each requires its own development effort from users, including different software development, tooling and training. They all employ two or more tiers to cater to different markets. In some cases, instrument options are not reusable across tiers!

Today, the Open Test System concept is being embraced, *not across the ATE industry, but within each of the major ATE companies.* This is a step in the right direction. However, it is not adequate to realize the full benefits of a single, industry-wide open system. For example, an intra-company open system does not reduce consumer uncertainity. If a single ATE vendor supplies a variety of testers for the wide range of devices produced by a semiconductor vendor, then the chip maker is at risk. We briefly examine the "open" systems of a few major ATE vendors to highlight the intra-company convergence to a single, open, extendable platform. In 2001, Advantest [8] and Teradyne [9] were the market leaders with about 23% apiece, market share. Agilent [10] placed third with a 17% share [2].

Advantest: Its T2000 Series [8] test platform, based on the OPENSTAR open architecture put forth by the Semiconductor Test Consortium [3], supports diverse test scenarios (including high-speed device test, at-speed test, DFT-test, and engineering test conducted in laboratory settings) and chip variety (wide range of chips with microprocessors, microcontrollers and RF devices). It is also designed to meet the needs of a broad array of customers from integrated device manufacturers (IDMs) to fabless companies. This is possible because the platform provides an array of interchangeable modules that adapt to changing device requirements. The T2000 Series utilizes a Windows 2000-based operating system, while users can employ either C++ or the OPENSTAR Test Programming Language (OTPL) [3] for their test programs. Recently, the company integrated a new technology into the open architecture platform, thereby highlighting the plug-and-play nature of the platform. The new technology (CertiMAXTM card technology) significantly simplifies the process of functional validation, debug, characterization and manufacturing test by allowing design data to be used directly for validation and manufacturing test without requiring vector or timing translation. Rush to consolidation of internal products around one, company-wide open platform is evident.

Agilent: Its 93000 Series platform is suitable for SOCs that include analog blocks, memory, third party cores as well as proprietary cores and glue logic. Test techniques supported range from at-speed functional vectors to BIST and hierarchical scan to mixed signal test. Data rates of 2.5 Gbps, supported at any pin, ease testing of high-speed computer buses and communication interfaces. The platform is specifically designed to provide not only high performance but also increased investment protection and lower financial risk by extending the useful lifetime of the test system. Again, chip and design diversity is supported by a single company-wide, open, flexible and scalable platform. The platform recognizes the benefit of longevity and scalability of the test system.

Credence: Supporting up to 1,024 pins, its Octet platform [11] can be configured with diverse digital capabilities and a comprehensive suite of analog instrumentation for a wide range of SOC devices in the computer, communications and consumer market. The platform also features a fully integrated design-to-production test-software suite, including test-development software and virtual test and debug tools. Octet's test-program, load-board, and docking compatibility with Credence's Quartet Series is an example of interoperability that enables customers to leverage existing Credence resources to quickly ramp-up for high-volume production.

LTX: Fusion HF, LTX's debut into the SOC testing segment, was based on the Fusion platform [12] that has up to 1024 channels for testing logic, embedded memory and mixed-signal components of an SOC. LTX followed it up with the release of Fusion CX, a lower-pincount, high-performance mixed signal tester for use in the wireless RF, automotive and consumer mixed-signal markets. This expands the range of devices that the single Fusion platform can be used for to advanced SOCs with mixed-signal components. Instrument extensions that focus on digital sub-systems in an SOC (VX III) and on test challenges presented by high-speed serial applications (PCI Express, SONET, SERDES etc.) have also been released. These instrument options seamlessly integrate into the scalable, single-platform Fusion test system.

NPTest: Its Sapphire NP platform [6] is built around the company's NPower open architecture and the Extendable Test Operating System (XTOS) software. The internal bus structure, (NPower Isochronous Fabric Interface) supports data transfer rates of up to 800 Mbytes/second. The platform can be modified, scaled and reconfigured to support up to 5,000 pins and pin-speeds of up to 6.4 Gbps. The tester is positioned as an open platform supporting functional, structural and design-for-test applications. Just like the other competitors, the Sapphire platform supports the entire range of semiconductors: high-performance automotive devices, chip sets, communications ICs, controllers, graphics ICs, microprocessors and system-on-chip products.

Teradyne: Its FLEX platform [9] addresses test, chip and customer diversity. FLEX spans test requirements from conventional DFT and structural test to standard analog and mixed-signal to complex SOC. FLEX's SOC Tester-Per-Pin Architecture delivers over 1000 digital channels, pattern-controlled analog, and high-efficiency concurrent test. Any device pin can connect to any instrument, each with its own independent timing. Its Integra Flex line was opened up to allow third parties to develop instrumentation options. Again, the test system addresses most of the changes

necessary to react to shifting consumer values, and a company-wide open test system is emerging.

When a device is designed with advanced DFT techniques, significant savings in test hardware can be realized since the primary driver for hardware costs are the functional test requirements of the device. SOCs with a very short life cycle, are on the shelf for only six months before becoming obsolete. Without using a DFT methodology, one can easily spend more time creating tests for SOCs than designing them. Increased use of DFT in SOCs has created a new market. Recognizing this opportunity, new entrants are focusing on low-cost testers that tradeoff test diversity and cost. They perform a subset of test functions. For example, DFT testers validate DFT functions and data [4, 13, 14, 15] but they do not perform functional testing that is the domain of more expensive ATE systems. Boundary scan testers [16] verify that the SOC is in compliance with the IEEE-1149.1 boundary-scan specification. They also analyze the accuracy of the BSDL file description against the actual silicon. This provides chip integrators with an invaluable tool when debugging silicon. Overall, they perform many of the same functions as a full-fledged, scalable ATE system from the leading vendors, at a fraction of the cost.

5 Winners and Losers

We have seen how an open test system changes the fundamental nature of the ATE game. Here, we discuss the effect on the players.

Consumers: Semiconductor chip manufacturers welcome open test systems and standards because they do not have to pick a winner and face the risk of being stranded. Components that seamlessly interconnect into an open framework offer compelling benefits. First, consumers can mix and match components to suit their cost budgets, device characteristics, and time-to-market constraints. Second, consumers are far less likely to become locked into a single ATE vendor. Cost of switching to another ATE vendor is low.

Open systems with plug-and-play ability do have some downsides for the consumer. The main one is loss of variety. The open interfaces may be poorly suited to some consumer's needs and workarounds can be expensive. Open systems that are not quite open are the bane of customers. Since system integration (i.e., integration of the open components from different ATE vendors) is left to customers, this could pose serious problems. For example, consider the PC industry a few years ago when customers where not quite sure exactly which video cards would work with which sound cards. The PC maker added value by making sure that components in the system worked together. The founder of a leading ATE vendor estimates that consumers may see the cost of test equipment coming down from 2% to 1.5% of their sales, but the consumer can end up spending 10 or 20 times that cost in trying to make everything work [17].

Incumbents: Cooperation has not been a key undertaking of the leading ATE companies in the past. A major reason is that the costs of switching from one ATE vendor to another are substantial, and consumers are locked-in to a vendor. With each of the leaders now pursuing their own open test system, they can ensure continued consumer lock-in, while enjoying the cost benefits of an intra-company open test system. However, this situation is unlikely to persist. Market fragmentation due to more than 40 to 50 test architectures serving the $5 Billion ATE market will force significant consolidation in the ATE industry. Leaders are looking at new ways to pursue the open systems concept, and yet keep the costs down. They are pursuing options ranging from assembly of test systems in mainland China [9] to outsourcing of manufacturing [12]. Incumbents are also considering providing applications support service [12]to provide further value to the consumer. The chances of an open, industry wide platform being established are good because a major consumer (Intel) is working closely with the ATE vendor industry.

A key issue for the incumbents is the management and upgrade of the industry-wide open test system. The open system has to evolve over time to meet the shifting needs of the consumer. Who will be in charge of setting the direction, or will multiple, incompatible versions of open systems arise? Also, without a sponsor, it is unclear who will invest resources to make necessary improvements and changes to evolve the open system. An industry-wide consortium can assume the responsibility of managing the open test system.

New entrants: Due to the change in the ATE game, second-tier companies who supply specialized equipment into one or more open platforms established by the market leaders are emerging. These companies can substantially cut into the revenue of the ATE industry incumbents. Product quality certification assumes significant importance. Third-party instrument suppliers, as well as system integrators who use these instruments will benefit from establishment of independent, quality assurance certification standards. The new entrants are additional participants in the open test system, and they will breed some overhead. However, an open interface will permit smooth handoff of test information throughout the chip manufacturing process that is increasingly diffused among designers, contract manufacturers, and test houses.

6 Conclusions

The move to industry-wide open test systems has begun. As a first step, major ATE vendors are consolidating their offerings into a vendor-specific, open architecture platform. However, significant test cost reductions can accrue only from an industry-wide consolidation behind a few open test architectures. There is considerable optimism that an industry-wide open test architecture will emerge within a few years because leading consumers like Intel are collaborating actively with ATE vendors to establish a consortium that will define and manage the growth of an open test system [3].

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