A High Efficiency 0.5W BTL Class-D Audio Amplifier with RWDM Technique

Simon C. Li
Advanced Technology & Integrated System Laboratory
National Yunlin University of Science and Technology
Seaman@yuntech.edu.tw

Vincent Chia-Chang Lin
Etrend Electronics, Inc.
http://www.etrend.com.tw

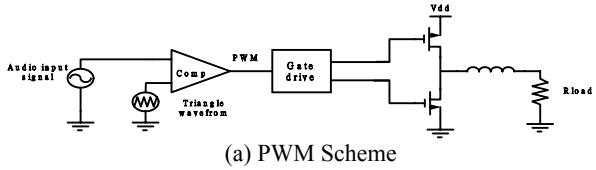
Abstract A novel class-D amplifier comprises a Rectangular Wave Delta Modulator (RWDM), bridged tied load (BTL) output gate-driver and low-pass filter. The rectangular wave delta modulator has a multiple inputs floating-gate hysteresis comparator and a feedback integrator formed by the *L-R* low-pass filter. This integrated amplifier has a flat frequency response with ±0.3 dB up to 20 kHz, deliver up to 0.5 Watts with 97% power efficiency, and a distortion of less than 1% over power and frequency range.

1. Introduction

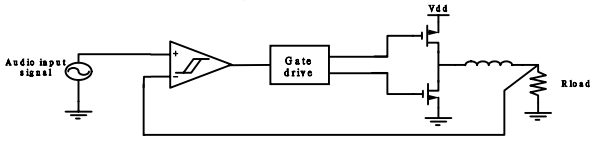
Recent advances in semiconductor technology have renewed interest in class-D integrated audio amplifiers, especially for portable and consumer electronics such as hearing-aids, multimedia players, notebook computers, USB hub-powered/wireless speakers and automotive audio amplifiers, etc. The operation of class-D amplifier was invented in 1959 by Baxandall who suggested using LC-oscillator circuits [1]. As compared to conventional analog class-AB amplifiers, class-D amplifiers operate in a switched mode. This results in a remarkable high power efficiency of 100% while an ideal switching characteristics is presumed. Therefore, the motivating factor driving research in class-D integrated amplifier is efficiency. The increased efficiency of class-D amplifier provides two main advantages over the class-A or AB amplifiers. The first advantage is the reduction of supply current required which translate to longer run-time on batteries, or reduced power supply requirements that translate to lower-cost and smaller power supply design. The second advantage class-D integrated amplifier offers is the reduction of heat generated that translates to more output power in a smaller package, and elimination of heat sinks. These two advantages make class-D integrated amplifier attractive to portable and consumer electronics.

The modulation technique of most class-D amplifiers are based on the Pulse Width Modulation (PWM) technique [2,3] where the PWM signal is issued from the comparison of a high frequency triangular wave and the input wave. Fig. 1(a) shows the typical PWM scheme of class-D amplifiers. The pulse width of the output signal is made proportional to the amplitude of the modulating signals. The signal at the output is recovered from the PWM signal by passing it through a low pass filter, which could be formed by a resistive load and an inductor as a passive R-L filter inherently obtained from earphones or speakers. The average current flowing through the load gives the amplified signal. When there is no signal can get at the output of the comparator with a square wave of 50% duty cycle. So the average output voltage is zero and the quiescent power is ideally zero. The gate-driver output power MOS transistors are designed to drive a low impedance speaker load.

Another common method of generating the output signal in class-D amplifier is to make use of a delta modulation scheme [4]. A modulated rectangular wave is produced whose average value tracks that of the input signal as well. Rectangular wave delta modulation (RWDM) has become an established alternative to PWM audio applications for providing a sinusoidal output voltage with a low harmonic content and ease of control of comparator output voltage [5,6]. In this paper a class-D amplifier based on the RWDM technique is proposed. The proposed RWDM scheme of class-D amplifier, as depicted in Fig. 1(b), comprises only a hysteresis comparator, gate-driving circuits and a feedback integrator formed by the L-R low-pass filter. Basically RWDM is analogous to PWM except the input signal is compared with the feedback signal that is essentially the integrated signal of RWDM by a low-pass filter. Unlike the conventional PWM class-D amplifier, proposed RWDM scheme of class-D amplifier does not require an external triangular-waveform oscillator. This benefits the design to achieve smaller chip area, lower cost and simpler application circuits.



(a) PWM Scheme



(b) RWDM Scheme

Fig. 1. Illustrations of class-D amplifier in (a) PWM scheme and (b) RWDM scheme.

The class-D amplifier based on the RWDM scheme, except for the inductor and the speaker load, could be verified and implemented into a single-chip by UMC 0.5μm CMOS process. The proposed RWDM class-D integrated amplifier is well-suited as a monolithic chip for battery-powered portable consumer electronic applications.

2. Principles of RWDM Technique

The principle of operation of the RWDM technique can be described with the aid of block diagram shown in Fig. 2. The audio input signal denoted as $V_i(t)$ is compared with the feedback signal or a carrier signal $V_c(t)$, obtained by integrating the modulated signal $V_m(t)$, to produce an error signal $E_r(t)$. According to the sign and preset magnitude of $E_r(t)$, the modulated output signal $V_m(t)$ has two possible values $\pm Vs$, whreas the time duration between two successive levels is determined by the slope of audio input signal V_i(t). It can be seen that the feedback signal $V_c(t)$ tracks the audio input signal $V_i(t)$ within the upper and lower boundary levels $\pm\Delta V$. From the modulator-operating principles, it can be observed that the RWDM output signal is decided by the integrator in the feedback path. Assuming that the modulator-switching frequency is high enough so that a small portion of the audio input sine wave is approximated by a straight line, the time duration for one complete cycle at the modulator output is given by [4]

$$T = \frac{4\Delta V S_c}{S_c^2 - S_i^2(t)\,|_{AC}} \qquad (1)$$

Where

$S_i(t)$ = instantaneous slope of the audio input signal
$S_i(t)|_{AC}$ = slope of the audio input signal between points A and C,
$\pm\Delta V$ = value of the hysteresis window, and
$S_c(t)$ = slope of the carrier wave.

The switching frequency of the modulator output is obtained from (1) as

$$f = \frac{1}{T} = \frac{S_c}{4\Delta V}\left[1 - \left(\frac{S_i(t)}{S_c}\right)^2\right] \quad (2)$$

For an input sinusoidal waveform, $V_i \sin\omega t$, the instantaneous slope of the audio input signal is given by

$$S_i(t) = \omega V_i \cos\omega t \quad (3)$$

And the modulator output switching frequency is obtained as

$$f = \frac{S_i}{4\Delta V}\left[1 - \left(\frac{\omega V_i}{Sc}\right)^2 \cos^2 \omega t\right] \quad (4)$$

Equation (4) shows the following:

1) The modulator switching frequency reaches a maximum value of $(S_c/4\Delta V)$ at $\omega t = k(\pi/2)$, where k is an odd number, resulting in an inherent minimum pulse width at the modulator output. Thus, no special effort is needed to provide minimum pulse width duration in the class-D amplifier.
2) The modulator switching frequency has a minimum value of $(S_c/4\Delta V)[1-(\omega V_i/S_c)^2]$, resulting in a maximum pulse at the modulator output.
3) The average switching frequency of the modulator is obtained by averaging the modulator instantaneous switching frequency over several cycles of the audio input signal and is given by

$$F_{avg} = \frac{S_c}{4\Delta V}\left[1 - \frac{\omega^2 V_i^2}{2 \times S_c^2}\right] \quad (5)$$

Since the switching power loss in the class-D amplifier depends on the average switching frequency of the modulator, (5) shows that the efficiency of RWDM class-D amplifier can be optimized by selecting appropriate values of the modulator parameters. From the operating principle of the RWDM, it can be seen that the modulator parameters that affect the frequency spectrum of the modulator output and hence the class-D amplifier output voltage are

1) The hysteresis bandwidth ΔV, is controlled directly by the trip voltage of hysteresis comparator.
2) The integrator gain S_c, is controlled by the time constant of the integrator in the feedback path.
3) The amplitude of the audio input signal V_i.

As a hysteresis behavior in the comparator, $V_c(t)$ can track the amplitude of $V_i(t)$ within the $\pm\Delta V$ boundary as shown in Fig. 2. Also the feedback signal $V_c(t)$ is the integrated signal of RWDM from a low-pass filter at the output, loading conditions from the loads are taken into account to control the RWDM signal and then to control the output power.

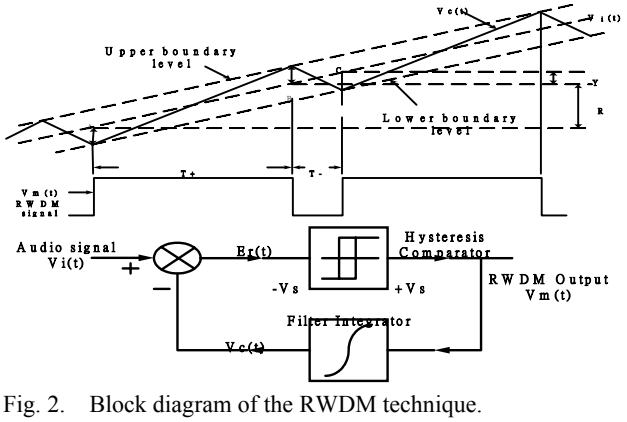


Fig. 2. Block diagram of the RWDM technique.

3. Design Principles

Fig. 3 shows the comprehensive configuration of a Bridge-Tied Load (BTL) class-D amplifier based on the RWDM technique. It is basically a fully differential version of the proposed RWDM scheme shown in Fig. 1(b). By using the BTL configuration, the maximum audio output voltage swing can be double those of the half-bridge configuration in Fig. 1(b). The audio input signal is directly connected to the input of the hysteresis comparator, which is ultimately a high impedance of an input MOSFET hence the loading effect of the signal source will not occur. The switching range of a hysteresis comparator is extended to control the amount of output ripple and switching frequency of the class-D amplifier. With the fitted hysteresis loop, the comparator can produce the output RWDM signal containing only logic high/low that is then integrated by the resistor-inductor L-R network.

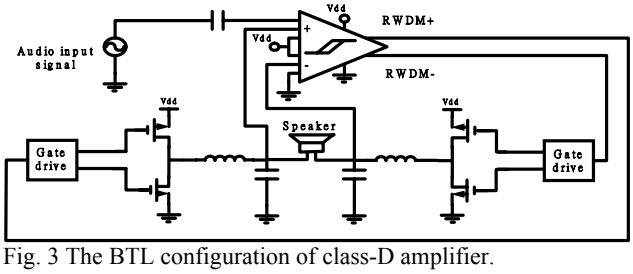


Fig. 3 The BTL configuration of class-D amplifier.

An illustration of a rail-to-rail hysteresis comparator [7] is shown in Fig. 4, where it is seen that the hysteresis is provided from two positive feedback paths produced by M_{10} and M_{11}. The positive feedback occurs only when the current ratio of I_{D10}/I_{D3} or I_{D11}/I_{D4} is greater than unity. If these current ratios increase further, the positive feedback current will increase as well. It expands the positive and negative trip point voltage hence a wider hysteresis is formed and can be controlled. This tunable hysteresis enables the comparator process a wide-range input signal. As represented particular wide-range input the comparator will compare the input signal with the saw-tooth-like feedback signal from the output in the following cycle. This characteristic allows the feedback signal at the gate of M_2 to track the amplitude of the input signal at the gate of M_1 effectively between V_{DD} and ground. Since one of the input gates of both M_1 and M_2 are connected to V_{DD}, so both FGMOSs of M_1 and M_2 are ensured to be turned on at all levels of the input signal. It enables the hysteresis comparator to perform the rail-to-rail feature in a lower supply voltage.

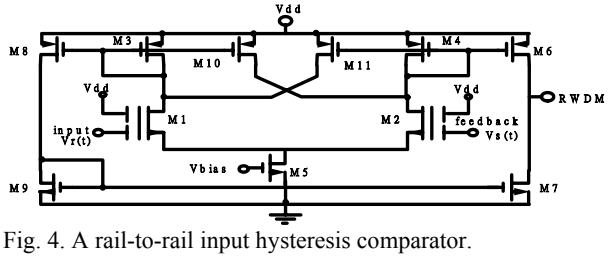


Fig. 4. A rail-to-rail input hysteresis comparator.

Develop a multiple-input hysteresis voltage comparator by means of multiple input floating-gate MOSFETs (MIFGMOS) is to allow low voltage operation for the amplifier. A MIFGMOS is a standard MOS except that common gate is built on poly1 and floated. The number of input control gates built on poly2, which is coupled to the poly1 floating-gate by the capacitors between poly1 and poly2. Therefore FGMOS can be implemented on any double-poly (DP) CMOS processes. The voltage of the floating gate, V_{FG} is determined as a linear sum of all input signals weighted by the capacitor coupling coefficients and can be described as

$$V_{FG} = \sum_{i=0}^{n} k_i V_i + \frac{Q_0}{C_T}$$
$$C_T = \sum_{i=0}^{n} C_i ; k_i = \frac{C_i}{C_T} \qquad (6)$$

Where Q_0 is the total initial charge on the floating gate, C_0 is the capacitor formed between the floating-gate and the substrate, and C_1, C_2, …, C_n are the capacitors between the floating gate and the input control gates. V_0 denotes the substrate voltage, V_i is the voltage of the input control gates i, where i = 1,2…, n. Normally, the initial charge Q_0 can be set by means of charge injection or UV light. However, if Q_0 is set to zero, the drain current of the FGMOS can be written as

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{FG} - V_s - V_{TH}\right)^2 \qquad (7)$$

Equation (7) is written to show a linear sum of the weighted multiple-input voltages. This operation ensures the comparator has the capability to handle large input signal swings while it still operates in the saturation region. Also, FGMOS can have more than one of the control gates, resulting in a MIFGMOS. The audio input signal is directly connected to the input of the comparator, which is normally in the range of 0~V_{DD} so 3-inputs floating-gate MOSFETs as the input differential pairs of the hysteresis comparator are used. In Fig. 5, a wide-range fully differential hysteresis comparator incorporates three-input gates FGMOS devices as the differential input pairs of which the coupling capacitors are designed as $C_1 = k_1 C_T$, $C_2 = k_2 C_T$ and $C_3 = k_3 C_T$ which C_T is the total capacitance of the floating gate and k_i, i= 1~3 are coupling weight coefficients. The first biasing-inputs at both gates of M_1 and M_2 of multiple-input hysteresis voltage comparator having the weight factor of k_1 are connected to V_{DD} to bias the differential pairs. This sets a fixed DC level of $0.5V_{DD}$ at the floating-gate on Ploy1 of the differential pairs. It is seen that first biasing-inputs is used to tune the effective threshold voltage. The first input gates are designed with half of the weight factor of the second gates in order to make the close loop gain of the amplifier equal to 2, which is the requirement to have an output signal swing of $\pm V_{DD}$ while the input signal is only in the range 0~V_{DD}.

4. Preliminary Results

The integrated class-D amplifier as shown in Fig. 3 has been implemented by UMC 0.5μm CMOS DPDM process. Fig. 6 displays frequency response (magnitude and phase) of the amplifier. The simulated transfer reveals a flat line with ±0.3 dB over the audible frequency range of 20 Hz~ 20 kHz. The output voltage signal with saw-tooth waveforms compared with input audio sinusoidal waveforms of 1 V, 20 kHz is shown in Fig. 7(a). The RWDM output signal with rectangular waveforms compared with input audio sinusoidal waveforms of 1 V, 20 kHz is shown in Fig. 7 (b). Fig. 8 shows the efficiency of the amplifier .versus varied audio signal amplitude at 1 kHz. The proposed class-D amplifier can deliver power into the nominal speaker loads of 8 Ω up to 0.5 Watts with 97% power efficiency, and remain a distortion of less than 1% over power and frequency range. The chip size of integrated class-D amplifier IC as demonstrated in the chip-photo of Fig. 9 is 1027μm by 574 μm.

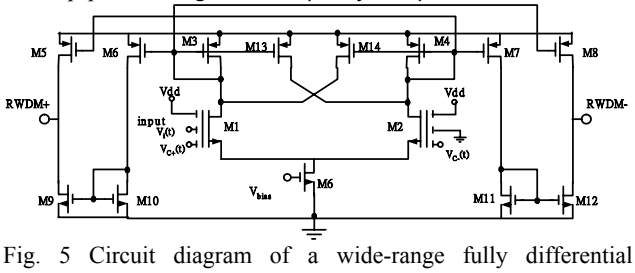


Fig. 5 Circuit diagram of a wide-range fully differential comparator.

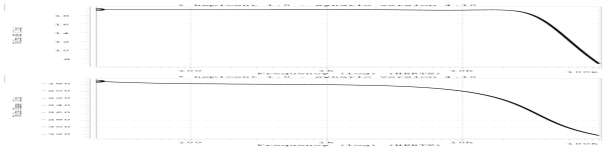
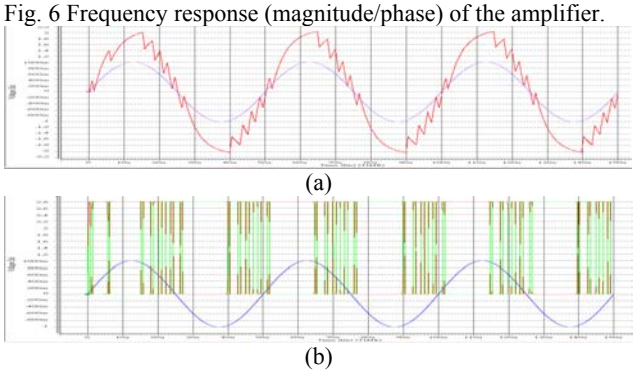


Fig. 6 Frequency response (magnitude/phase) of the amplifier.



(a) (b)

Fig. 7 (a) The output voltage signal and (b) RWDM output signal are compared with input audio waveforms of 1 V, 20 kHz.

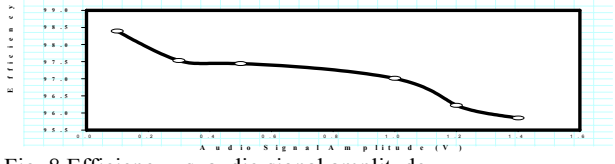


Fig. 8 Efficiency vs. audio signal amplitude.

Fig. 9 A micrograph of 0.5W RWDM class-D amplifier IC.

5. Conclusions

A new proposed class-D amplifier based on the RWDM technique is presented. The amplifier has a very simple architecture that makes it easier for it to be integrated with other circuit blocks on a system level. The power efficiency of this amplifier is 97 % at 0.5 Watt s with a 2.8-V power supply. By virtue of the high efficiency of class-D architecture coupled with the low voltage operation provided by the use of floating-gate MOSFET hysteresis comparator, this amplifier is suitable for portable devices with battery operations.

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