Effects of Noise and Nonlinearity on the Calibration of a Non-Binary Capacitor Array in a Successive Approximation Analog-to-Digital Converter

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Abstract—— A successive approximation analog-to-digital converter using a non-binary capacitor array is presented. A perceptron learning rule is used as the capacitor calibration algorithm. The nonlinearity is analyzed using the Volterra series. The effects of noise and nonlinearity are modeled to verify the calibration robustness. With the presence of noise and nonlinearity, the capacitor weights are adaptively calibrated to match the physical capacitors with better than 22-bit accuracy. The accuracy is no longer limited by capacitor matching.

I. Introduction

Many modern fabrication technologies are driven by digital circuitry. It is challenging to build high performance analog circuitry using the fabrication technology in deeper sub-micron and nanometer era. New architecture must be explored to design high performance analog and mixed signal circuitry in deeper sub-micron technology. In delta-sigma converters, the signal is sampled at many times the Nyquist rate and digital filtering is used to remove the noise outside the signal bandwidth [1]. The requirement on analog anti-aliasing filters is relaxed. Delta-sigma converters are often used in high accuracy and low speed applications. High-speed analog-to-digital converters (ADCs) often use flash, pipeline or interleaved architectures. They can run at very high speed but usually at low accuracy [2,3,4,5]. Successive approximation register (SAR) converters offer the combination of resolution and speed unmatched by delta-sigma, pipeline or flash type ADCs. SAR's have no latency, and can be multiplexed. Furthermore, the power consumption is relatively low. These features make SAR converters ideal for data acquisition and fiber-optic applications.

The advantage of the binary-weighted DAC in conventional SAR ADC is that the back-end digital complexity is low. An accuracy of 10 bits can be easily achieved with straightforward design techniques using capacitor based charge redistribution converters because capacitor matching better than 0.1% is common [6]. However, building a binary weighted DAC with greater than 16-bit accuracy and greater than 1 MSPS speed is not trivial. In order to get better than 10 bits accuracy in charge-redistribution DAC, production laser trimming or other trimming methods are used to guarantee tighter capacitor matching. The production laser trimming is expensive. The accuracy of other trimming methods is usually limited to the size of the smallest capacitor that can be fabricated in a well-controlled way. The capacitor matching in the capacitor array is the limiting factor for getting higher accuracy. We present a new calibration method to greatly relax the matching requirement of the capacitor array so that capacitor matching no longer limits the accuracy.

Instead of matching the physical capacitors themselves, we build a capacitor array with no strict matching requirement and adaptively adjust the digital representation of the capacitors: capacitor weights to match the fabricated capacitors in the capacitor array. In our SAR ADC based on non-binary capacitor array, we take advantage of the redundancy in the non-binary capacitor array and the adaptive calibration algorithm to greatly relax the capacitor matching requirement. The capacitor calibration algorithm is based on a perceptron learning rule that was originally developed for Artificial Intelligence applications [7]. This algorithm calibrates the capacitor weights so that the matching requirement on the physical capacitor array is no longer a limiting factor. The effects of noise and nonlinearity on the calibration are also modeled. Volterra series approach is used to analyze the nonlinearity.

II. Capacitor Array Calibration Algorithm

If the capacitor weights reflect the physical capacitor values, then we can use this set of capacitor weights to get accurate digital result in the successive approximation conversion process by adding the corresponding capacitor weight when the comparator output is 1. We use the perceptron learning rule [7] to calibrate the capacitor weights. In order to create learning cases, we have to create redundancy in the system. A capacitor array with radix less than 2 in the charge-redistribution SAR converter creates redundancy.

In non-binary system, there are multiple combinations of capacitors in the successive approximation conversion process that will lead to the same final digital result. The errors made in the early steps of the successive approximation conversion process can be corrected in later steps because of the many-to-one correspondence between the combinations of capacitors and the final digital result. Smaller radix will give us more redundancy and will tolerate more initial incorrect decisions but it will require more capacitors in the array and longer time for conversion. There is not enough redundancy if the radix is very close to 2. Radix 1.8 is a good trade-off. The actual ratio between adjacent capacitors can deviate from this radix and will be calibrated out.

A non-binary capacitor array is shown in Fig. 1. The ratio between adjacent capacitors is approximately 1.8 which means that $R = 1.8$. In order to get 16-bit resolution, the

largest capacitor in the array should be great than $C \times 2^{16}$. We need 20 capacitors in the capacitor array. The top plates of all the capacitors are connected to the input of the comparator. The bottom plate of each capacitor can be switched to the analog input Vin, the reference voltage Vref or the signal ground Sgnd. The comparator output SARout is the decision of each successive approximation step during conversion.

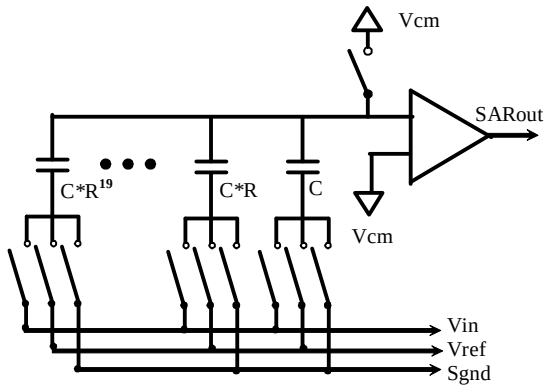

Fig. 1. A non-binary capacitor array and a comparator

The capacitor weight corresponding to capacitor *j* is denoted as *W(j)* (*j* = 19 to 0). *Woff* is the weight for the system offset. The capacitor weights are set to initially guessed values. The calibration is not sensitive to these initial weights. The calibration algorithm works as follows:

1. Sample the reference voltage using a random vector {*A(j)*}. The bottom plate of capacitor *j* is switched to the reference voltage Vref if *A(j)* = 1. The bottom plate of capacitor *j* is switched to the signal ground Sgnd if *A(j)* = 0. We can use a linear feedback register (LFSR) to generate this random vector. This will create a charge on the top plate of the array. Add the corresponding capacitor weights and offset W_{off} to get a digital result D_a.

$$D_a = W_{off} + \sum_j A(j) \times W(j)$$

2. Perform successive approximation starting from the largest capacitor. After 20 cycles, we can get a result in the SAR register {*B(j)*}. *A(j)* and *B(j)* may not be the same due to the redundancy and the noise in the system. Add the corresponding capacitor weights to get D_b. D_a and D_b may be different because of the redundancy and the noise in the system.

$$D_b = \sum_j B(j) \times W(j)$$

3. After the SAR conversion process, we get the sign of the residual analog voltage on the top plate of the array: S_a by checking the comparator output at the end of SAR process. We may check the comparator output multiple times and take the average to reduce the effect of noise. We can also get the sign of D_a minus D_b which is the digital sign: S_d.

$$S_d = D_a - D_b$$

4. We have a learning case if the analog sign and digital sign do not equal. The analog sign S_a reflects the real result. The digital sign may be wrong because the capacitor weights may not accurately reflect the corresponding capacitance before we finish the calibration. We need change the capacitor weights to the right direction. We can correct the capacitor weights according to the perceptron learning rule [7]:

$$W(j) \leftarrow W(j) + \alpha \times [A(j) - B(j)] \times (S_a - S_d)$$

$$W_{off} \leftarrow W_{off} + \alpha \times (S_a - S_d)$$

where α is called the learning rate. *A(j)* and *B(j)* may not be the same due to the redundancy and the noise in the system. This is essential to the algorithm. Otherwise, nothing can be learned from the process.

5. Loop through step 1 to 4 for predetermined number of times or until there is no significant improvement, then change α to a smaller value.

6. Loop through step 1 to 5 until α is smaller than the accuracy level we want.

It has been proven that the weight space has no local minimum[7]. Provided the learning rate is not so large to cause overshooting and the learning cases represent linearly separable function, the capacitor weights will converge to the correct values. If we calibrate long enough, we can potentially calibrate the capacitor weights to an accuracy level better than the noise level in the system because of the intrinsic averaging effect in the calibration process.

III. System Architecture and Design

A. System Architecture

We propose to use a mixed-signal micro-controller architecture to provide centralized control for the analog and digital circuitry in our SAR ADC as shown in Fig. 2. The system uses a unified control structure. The address unit generates the program address to program ROM. The address unit implements increment, load immediate address for program jumps, and load interrupt vector modes. The ROM contains the program to be executed. The instructions from ROM are fed to the instruction decode block. There are separate decoding blocks for the analog and digital datapaths to generate the control signals for the respective blocks. This allows a unified programming model for implementing the capacitor array calibration algorithm, writing the program for the normal SAR conversion process in micro-code, and interfacing to external peripherals. This architecture simplifies the sequencing of each step, allows algorithm development and changes, allows design-for-test (DFT) code to be implemented, and provides an intellectual property (IP) block portable to other mixed-signal designs.

The analog blocks in the SAR converter include a 20-bit linear feedback shift register (LFSR), a non-binary capacitor array (i.e. cap array), a comparator and SAR return path logic. The random vector generated by the

LFSR is used to control the bottom plate connection of the capacitor array during the sampling phase. The capacitor is connected to the reference voltage Vref if the corresponding bit in LFSR is 1. The capacitor is connected to the signal ground Sgnd if the corresponding bit in LFSR is 0.

The digital blocks include a 64-word by 32-bit register file, a 32-bit arithmetic and logic unit (ALU) and accumulator, and serial or parallel interface. The main block in the ALU is a 32-bit adder. We use 32-bit datapath to accommodate a wide range of capacitor weights for high accuracy. Other peripheral or arithmetic blocks can be added as needed.

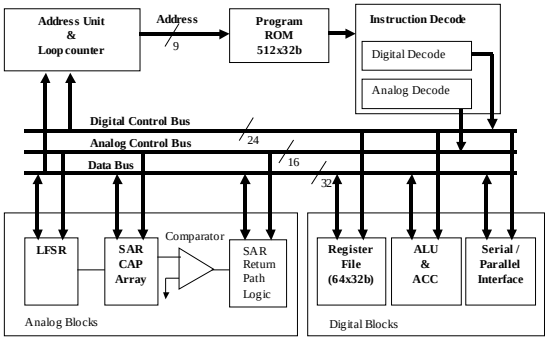

Fig. 2. The block diagram of the ADC using a mixed-signal microcontroller architecture

The instruction set contains two parts: a digital instruction word and an analog instruction word. A digital instruction consists of a 6-bit opcode, and three 6-bit operands: source 1, source 2 and destination. The analog instruction consists of a 3-bit opcode and a 5-bit operand. The instruction set allows simultaneous control of both the analog and digital blocks.

This system provides the infrastructure to implement the calibration algorithm as the instructions running on the mixed-signal microcontroller. The system can also handle normal successive approximation conversion process when we sample the analog input voltage. We only need call a different program, which gives us the flexibility. We have a complete successive approximation A/D converter.

B. System Clock

We design a 16-bit, 1.5 MSPS successive approximation A/D converter using the non-binary capacitor array. We allocate 12 clock cycles for sampling. The successive approximation conversion takes 20 cycles because there are 20 capacitors in the array. The total number of clock cycles for one complete conversion is 32. The system clock frequency is 48 MHz.

IV. Analysis of Noise and Nonlinearity

A. Noise

The analog power supply voltage is 3.3 V for the 0.25 um process. The reference voltage is 2.5 V. The target signal-to-noise ratio (SNR) is 92 dB. The peak to peak input voltage $V_{in(p-p)}$ is 2.5 V. The total root-mean-square (RMS) noise voltage V_n can be calculated as

$$V_n = \frac{V_{in(p-p)}}{2\sqrt{2}\times 10^{92/20}} = 22.2\ \mu\text{V}$$

Two main noise sources: the kT/C noise V_{n_cap} and the comparator noise V_{n_comp}. We allocate the noise budget so that the kT/C noise voltage is twice the comparator noise. Then the kT/C noise voltage is

$$V_{n\_cap} = 19.86\ \mu\text{V}$$

The comparator noise is

$$V_{n\_comp} = 9.93\ \mu\text{V}$$

We know that the kT/C noise is approximately 64 μV for a capacitor of 1 pF at room temperature. So the total effective capacitance of the capacitor array should be

$$C_{total} = \left(\frac{64}{V_{n\_cap}}\right)^2 = 10.4\ \text{pF}$$

The smallest capacitance is

$$C_{LSB} = \frac{C_{total}}{\sum_{k=0}^{19} 1.8^k} = 0.065\ \text{fF}$$

The largest capacitance is

$$C_{MSB} = C_{LSB}\times 1.8^{19} = 4.6\ \text{pF}$$

The smallest capacitor is too small to fabricate in a well-controlled way directly, so we divide the array into 3 sections and use two bridge capacitors between adjacent sections to implement this capacitor array. The total effective capacitance at the input node of comparator is about 10.4 pF. The actual capacitance ratio between two adjacent capacitors can deviate from 1.8. The calibration algorithm will make the capacitor weights match the fabricated capacitors.

In order to design a high speed comparator [8], we use preamplifiers to amplify the input voltage to a sufficiently large value V_x and then apply it the latch. A comparator consists of 5 preamplifiers and a latch is shown in Fig. 3. It has two modes of operation: tracking and latching. Preamplifiers are enabled to amplify the input difference while the latch is disabled in the tracking mode. In the latching mode, preamplifiers are isolated from the latch and the latch is enabled so that the voltage at the latch input is re-generatively amplified. A logic level will be generated at the latch output.

Assume that the root mean square (RMS) error of the capacitor weights equals σ after calibration. The worst case RMS error in the conversion result due to capacitor weight errors is $\sqrt{20}\sigma$ for 20 capacitors. We choose a 6-sigma

error to be smaller than least significant bit (LSB) of a 16-bit ADC.

$$6\sqrt{20}\sigma \le 2^{-16} \Rightarrow \sigma < 2^{-21}$$

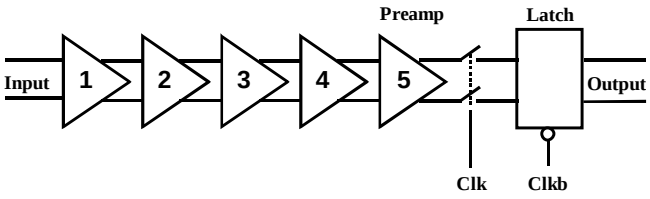

Fig. 3. A comparator with preamplifiers and latch

The calibration needs to calibrate the capacitor weights to better than 21-bit accuracy in order to get 16-bit accuracy for the ADC. The voltage to be resolved by the comparator is smaller than $\sigma \times V_{in(p-p)}$. The total gain of the preamplifiers should be:

$$G_{preamp} \ge \frac{V_x}{\sigma \times V_{in(p-p)}}$$

The first 4 stages are low gain and high bandwidth preamplifiers. The fifth stage is a high gain and relatively low bandwidth preamplifier.

The comparator offset is part of the system offset. There is an offset register corresponding to the system offset. The system offset is calibrated automatically during the capacitor array calibration.

The noise and interference sources at a typical switch node are shown in Fig. 4. The typical noise sources are thermal noise V_{nth}, interference V_{int} and flicker noise (1/f noise) V_{nflick}. They all affect the system performance. The major noise sources in the system include the kT/C noise in the capacitor array, the charge injection noise [9] from the tracking switch, the noise from the reference voltage and the noise in the comparator. They will affect the dynamic range in the ADC. They may also affect the calibration, but the noise effect is averaged in the calibration process. The calibration accuracy does not improve indefinitely simply by averaging longer because the contribution of low frequency noise component in flicker noise becomes more significant. Flicker noise imposes a limit on the calibration accuracy.

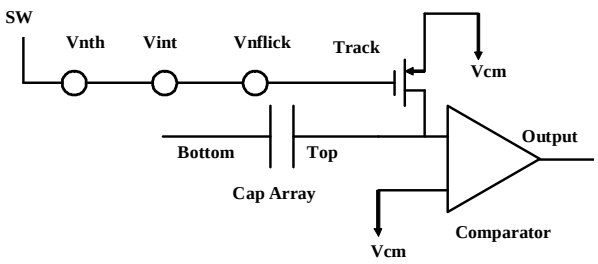

Fig. 4. The noise and interference sources

B. Nonlinearity

Under the assumption of weak nonlinearity in the circuitry, we use Volterra series [10] to analyze the nonlinearity. The Volterra series representation provides an explicit nonlinear representation of the system response and the insight into the system operation. We know what to modify in order to meet the nonlinearity specification. This is the advantage of Volterra series approach over the simulation methods.

The preamplifiers stage 1 to stage 4 use the architecture as shown in Fig. 5. They are low gain and high bandwidth stages. PMOS transistors M1 and M2 are the input differential pair. Diode connected transistors M3 and M4 are the loads. A quasi-autozero technique can remove signal hysteresis by shorting the output momentarily before comparison. The gate of M5 is controlled by quasi-autozero signal QAZ.

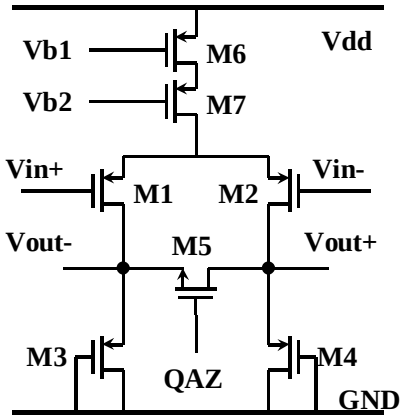

Fig. 5. Preamplifiers stage 1 to 4 in the comparator

We use Volterra series to analyze the nonlinearity for the differential amplifier in Fig. 5. The second order harmonic distortion [10] due to mismatches is approximately:

$$HD_2 \approx \frac{V_{in}K'_{2g_m}}{8}\left(\frac{3\Delta g_m}{g_m} - \frac{\Delta K_{2g_m}}{K_{2g_m}} + \frac{15}{2}\frac{\Delta g_m}{g_m}\frac{\Delta G_L}{G_L}\right)$$

g_m, K_{2g_m} and G_L are the nominal transconductance of M1 and M2, the nominal 2nd order nonlinear coefficient for g_m, and the nominal conductance of the load transistors M3 and M4, repectively. Δg_m, ΔK_{2g_m} and ΔG_L are the mismatches of g_m, K_{2g_m} and G_L, respectively. K'_{2g_m} is the normalized 2nd nonlinear coefficient for g_m.

The third order harmonic distortion is

$$HD_3 = \frac{V_{in}^2}{8g_m}\left(\frac{K_{3g_m}}{2} - \frac{K_{2g_m}^2}{g_m + g_{mb}} + \frac{K_{2g_m\&g_{mb}}K_{2g_m}}{2(g_m + g_{mb})}\right)$$

g_{mb} is the bulk transconductance of M1 and M2. K_{3g_m} is the 3rd order nonlinear coefficient for g_m. $K_{2g_m\&g_{mb}}$ is the 2nd order nonlinear coefficient describing the nonlinear

dependence of the drain current on gate-source voltage V_{GS} and source-bulk voltage V_{SB}.

We can derive higher order distortions using the same method. Other nonlinearity sources include input-dependent sampling switch resistance and parasitic capacitance, charge injection from the tracking switch, charge sharing between the anti-aliasing filter capacitor and the non-linear parasitic capacitor of the sampling switch. We can derive the harmonic distortions using symbolic analysis program if we consider all these nonlinearities. The expression may become very complex. We use the approximate expression consisting of major terms to gain the insight about the contribution of individual nonlinearity.

We include these nonlinearities in the modeling and simulation to evaluate the effect of the nonlinearity to the capacitor array calibration. We estimate the system distortion from the nonlinear coefficients using the above analytical equations and make sure they still meet the system requirement. We know what parameters to change in order to meet the distortion requirements. This is the advantage of the Volterra series approach.

V. Simulation Results

A. Simulation Method

We build a model for a 16-bit successive approximation A/D converter using the non-binary capacitor array. The ADC is expected to run at 1.5 MSPS. The power consumption is expected to be 25 mW. We simulate the analog circuitry such as the sampling network and comparator using SPICE. The simulation shows that they meet the speed requirement and noise specification. Our focus here is the calibration algorithm. We just use the noise design target in the simulation for the calibration. The thermal noise voltage is 19.86 μV. The comparator noise voltage is 9.93 μV. We implement the capacitor array calibration algorithm based on the perceptron learning rule. The simulation is done using Verilog. The analog quantities are represented using floating point numbers. The reference voltage is 2.5 V. The offset is assumed to be 10 mV. The calibration algorithm is implemented as the microcode running on the mixed signal microcontroller.

B. The Convergence of Capacitor Weights

The 20 capacitor weights and one offset are scrambled to a large extent in the early stage of calibration. The calibration corrects the capacitor weights based on the learning cases. This adaptive correction mechanism makes the capacitor weights converge nicely to the correct values. The accuracy of the capacitor weights is calculated from the statistics of the end results of calibrations. We represent the calibration accuracy in terms of the equivalent accuracy level in bits. It is calculated as in the following equation:

$$accuracy(j) = \log_2 \frac{W_{total}}{\sigma(j)}$$

where $\sigma(j)$ is the standard deviation of capacitor weight j, W_{total} is the sum of total capacitor weights. The offset corresponds to j = 20.

C. The Effect of Averaging

There is intrinsic averaging effect in the calibration process. Additional averaging can improve the convergence speed and the calibration accuracy. There are two basic averaging methods. Comparator averaging refers to the averaging of the sign check at the comparator output in the end of the conversion cycle during calibration. Thermal noise averaging or kT/C averaging is done by using the same random vector *A(j)* to sample and forcing the conversion result *B(j)* to be the same from prior cycle, then checking the sign of the new comparator output. The sign is averaged with other sign checks corresponding to the same pair of *A(j)* and *B(j)*. The calibration accuracy with different averaging schemes is shown in Fig. 6. It shows 4 cases: (1) no averaging, (2)16 comparator averages, (3)16 comparator averages and 4 kT/C averages, and (4)16 comparator averages and 16 kT/C averages. Comparing to the case of no averaging, we see about 1-bit accuracy improvement for the cases with averaging. The intrinsic averaging is already very good in this case.

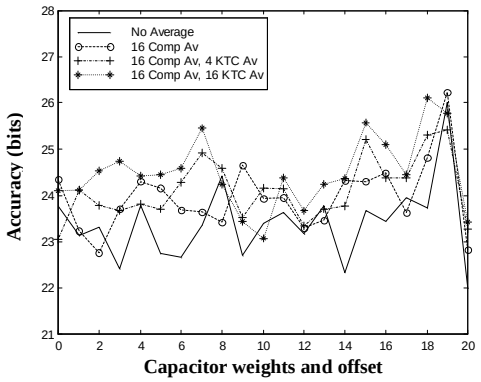

Fig. 6. Calibration accuracy with different averages

D. The Effects of Nonlinearity

We need make sure that the calibration is robust under different conditions. So we consider the effects of the non-idealities in the system such as noise, interference and nonlinearity. We analyze them and model them. We also simulate them to evaluate their effects. We introduce nonlinearity in the model. Fig. 7 shows the calibration result when the nonlinearity of -88dB is included to the system model. The accuracy of capacitor weights is still better than 22-bit. The capacitor weights are calibrated with better than 22-bit accuracy consistently after the capacitor array calibration process. The matching requirement for the non-binary capacitor array can be greatly relaxed.

The simulated ADC output spectrum after the calibration for a full scale input sine wave of 150kHz is shown in Fig. 8. The second harmonics and higher order harmonics can be seen in the spectrum. This demonstrates that the calibration works well even with nonlinearity in the system. This shows the effectiveness and the robustness of the calibration algorithm. The total calibration time is about 50ms. Since capacitor ratios do not vary with temperature and time, the calibration only needs to be done once at power up.

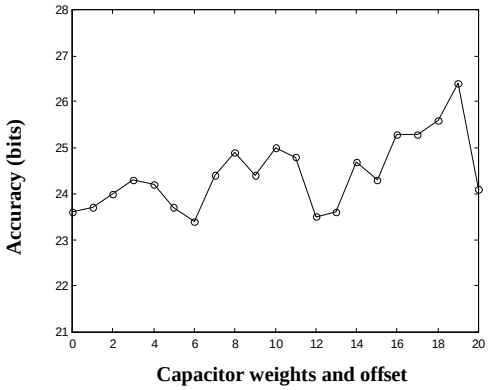

Fig. 7. Calibration accuracy with -88 dB nonlinearity in the system

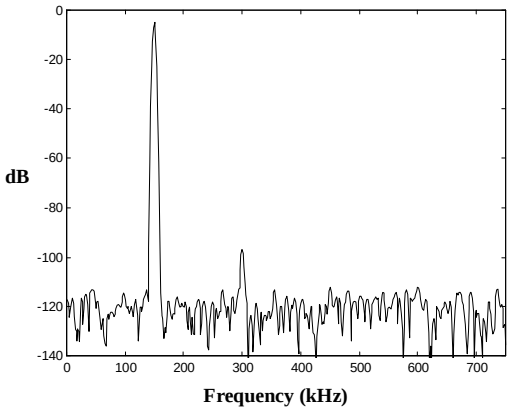

Fig. 8. ADC output spectrum for full scale input sine wave

VI. Conclusion

The new architecture and calibration technique of a high performance successive approximation ADC using non-binary capacitor array are presented. A mixed-signal microcontroller architecture is used to implement the relatively complex capacitor array calibration algorithm for the SAR ADC. The Volterra series is used to analyze the nonlinearity. The capacitor weights are calibrated with better than 22-bit accuracy with the presence of noise and nonlinearity. It demonstrates the robustness of the calibration algorithm. It is essential to the design of high speed and high resolution A/D converters. It has even more advantages for mixed signal VLSI in system-on-chip applications in deeper submicron technology since it relaxes the matching requirement on analog circuitry.

With 22-bit accuracy for the calibrated capacitor weights, we can potentially get even higher resolution with the same architecture. The limiting factor is the noise in the circuit. Capacitor matching is no longer a limiting factor. There is a trade-off between speed and noise level. We can use larger capacitance in the array if we want to lower the noise level. However, larger capacitance will slow down the conversion speed. This algorithm may also be used to calibrate other analog circuits such as pipeline ADC and relax the matching requirement.

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