Analysis of MOS Cross-Coupled LC-Tank Oscillators using Short-Channel Device Equations

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Abstract— New analytical techniques for estimating the large-signal periodic steady-state solution of MOS LC-tank oscillators using short-channel device equations are presented. These techniques allow us to make quantitative estimates of the oscillator steady-state performance without the need for time-consuming transient simulations using simulators such as SPICE. Further, our engineering techniques provide insight and quantitative understanding on the design of current-day, deep-submicron MOS LC-tank oscillators and serve as a starting point in a design strategy that includes complete phase noise/timing jitter analysis and optimization. Our analytical results for a cross-coupled LC-tank oscillator that was previously fabricated and tested are in good agreement with simulations using HSPICE.

I. Introduction

An accurate periodic steady-state solution for oscillators is an essential step for any CAD as well as analytic approach aimed at obtaining accurate estimates for oscillator phase-noise performance. Advanced RF circuit simulator packages such as SpectreRF and SuperSpiceRF[1] obtain the large-signal periodic steady-state solution of an oscillator by running transient analysis long enough for the oscillator to reach its periodic steady-state (PSS) solution [1, 2]. For example, an oscillator operating at 10 GHz frequency requires transient analysis to be run for as long as 20 ns with a time-step ranging from 1 ps to 5 ps. Efficient numerical techniques, both in the time-domain and frequency-domain, have been implemented in such CAD tools which are based on harmonic balance and shooting methods. Not until an accurate PSS solution is reached can phase noise analysis on these oscillators be performed.

From the analytic point of view of obtaining the oscillator steady-state solution, few significant attempts have been made [6–8]. More substantive work is available for the large-signal analysis of differential amplifier pair, e.g., [9–11]. Most of these attempts, however, use long-channel device equations for modeling the MOS transistor I-V characteristics. These *square-law* type of equations do not take into account short-channel effects, such as velocity saturation and mobility degradation and hence, are inaccurate for current-day oscillator designs. Therefore, there is a need for new accurate analytical methods which use the more accurate short-channel device equations [12] to obtain the oscillator periodic steady-state solution.

In this paper, we develop analytically using short-channel device equations the periodic steady-state expressions for the most common MOS oscillator topology: *the cross-coupled LC-tank oscillator*. These equations serve as starting point for an oscillator design methodology that allows us to derive analytically closed-form expressions for the oscillator perturbation projection vector (PPV) [5]. This, in turn, leads to the calculation of a single scalar c, which completely characterizes the phase noise performance of an oscillator. Hence, such design methodology based on analytical expressions allows us to accurately estimate the oscillator phase noise/timing jitter from its constituent circuit parameters using hand analysis. This can further lead to a systematic and quantitative approach for analytically optimizing oscillators with respect to phase noise. Theoretical predictions of the oscillator's steady-state performance are compared with results of circuit simulations using HSPICE for a previously fabricated oscillator [13] for which simulations sufficiently represent measured results.

II. Short-Channel Equations

The square-law (long-channel) characteristic equations provide moderate accuracies for devices with minimum channel lengths greater than 4 μm. However, in the deep submicron regime, below 0.5 μm, these equations are inapplicable due to higher-order short-channel effects which necessitate using more complex models, such as the *short-channel MOS device equations* [12]. This is a sufficiently accurate, yet compact model for short-channel devices (in the saturation region, i.e., $V_{DS} \geq V_{DS,sat}$) and is given by

$$I_D = WC_{ox}v_{sat}\frac{(V_{GS}-V_t)^2}{V_{GS}-V_t+E_{sat}L}, \tag{1}$$

$$V_{DS,sat} = \frac{(V_{GS}-V_t)E_{sat}L}{V_{GS}-V_t+E_{sat}L}, \tag{2}$$

[1] SuperSpiceRF is a next generation RF circuit simulator from Berkeley Design Automation, Inc. and incorporates ideas of [3–5] for oscillator phase noise analysis.

where

$$E_{sat} = \frac{2v_{sat}}{\mu_{eff}}, \quad \mu_{eff} = \frac{\mu_0}{1 + \Theta(V_{GS} - V_t)},$$

Θ is a parameter that is inversely proportional to the oxide thickness usually in the range from $0.1\,\mathrm{V}^{-1}$ to $0.4\,\mathrm{V}^{-1}$, C_{ox} is the gate oxide capacitance per unit area, μ_0 is the *low-field* mobility of the carrier, W is the device width, L is the device length, V_{GS} is the device gate-source voltage, V_t is the threshold voltage, and v_{sat} is the velocity saturation index.

III. Cross-Coupled Oscillator

The most common and convenient LC oscillator configuration for realization in MOS technology is the cross-coupled LC-tank oscillator shown in Fig. 1. In monolithic form, transistors M1 and M2 are biased with a tail current source I_{SS}, connected to the sources of M1 and M2. The inductors are usually on-chip spiral inductors with relatively low Q (less than 10) and the resistors R_L represent the inductor parasitics. The load capacitors C_L represent chip parasitics plus any added load capacitances. These capacitors are essential for the operation of the oscillator and in the simplest form, when maximum frequency precision is not needed, they are composed purely of chip parasitics. Tuning of the oscillator frequency can also be achieved by replacing these capacitors with MOS or diode varactors.

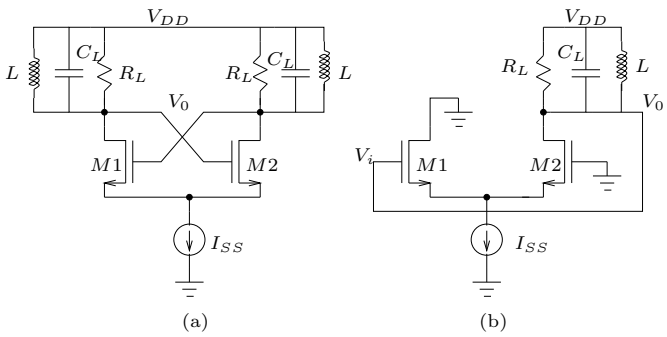


Fig. 1. (a) Cross-coupled oscillator schematic and (b) single-ended version.

A. Large-Signal Analysis

The following analysis applies equally to a corresponding p-channel cross-coupled pair with appropriate sign changes. The large-signal analysis begins by assuming that M1 and M2 are perfectly matched. We will do the analysis for the single-ended version of the oscillator (shown in Fig. 1(b)), knowing that we will have the same frequency and distortion characteristics as the fully differential form. The only difference is the magnitude of the output waveforms which is half of that of the fully differential form.

For this large-signal analysis, we assume that the output resistance of the tail current source $R_{SS} \to \infty$ and that the output resistance of each transistor $r_0 \to \infty$ since these assumptions do not strongly affect the large-signal behavior of the circuit. We also assume that the drain resistors are small enough that neither transistor operates in the triode region if $V_i \le V_{DD}$. Applying short-channel equations to transistor M1,

$$I_1 = WC_{ox}v_{sat}\frac{(V_{GS_1} - V_t)^2}{V_{GS_1} - V_t + E_{sat}L}. \tag{3}$$

and defining the parameters V_a and b as

$$V_a = \frac{I_{SS}}{WC_{ox}v_{sat}}, \quad b = \frac{E_{sat}L}{V_a},$$

we can normalize the voltages and currents in Eq. (3) as

$$\frac{I_1}{I_{SS}} = \frac{WC_{ox}v_{sat}}{I_{SS}}\frac{(V_{GS_1} - V_t)^2}{V_{GS_1} - V_t + E_{sat}L} = \frac{1}{V_a}\frac{(V_{GS_1} - V_t)^2}{V_{GS_1} - V_t + E_{sat}L}.$$

A similar derivation can be performed for transistor M2. Thus, the normalized drain current equations for both transistors are

$$i_1 = \frac{v_1^2}{v_1 + b}, \tag{4}$$

$$i_2 = \frac{v_2^2}{v_2 + b}, \tag{5}$$

where, by definition

$$i_1 = \tfrac{I_1}{I_{SS}}, \qquad v_1 = \tfrac{V_{GS_1} - V_t}{V_a},$$
$$i_2 = \tfrac{I_2}{I_{SS}}, \qquad v_2 = \tfrac{V_{GS_2} - V_t}{V_a}.$$

From KCL at the sources of M1 and M2 we have

$$i_1 + i_2 = 1. \tag{6}$$

Using Eqs. (4), (5), and (6) to eliminate i_2 gives

$$v_1 = \frac{1}{2}\left(i_1 + \sqrt{i_1^2 + 4i_1 b}\right), \tag{7}$$

$$v_2 = \frac{1}{2}\left(1 - i_1 + \sqrt{1 + i_1^2 - 2i_1 + 4b - 4i_1 b}\right). \tag{8}$$

From KVL around the input loop, the input voltage can be written as

$$V_i = V_{GS_1} - V_{GS_2},$$

which is conveniently normalized as

$$v_i = \frac{V_i}{V_a} = \frac{(V_{GS_1} - V_t) - (V_{GS_2} - V_t)}{V_a} = v_1 - v_2,$$

to finally get

$$v_i = \frac{1}{2}\left(2i_1 - 1 + \sqrt{i_1^2 + 4i_1 b} - \sqrt{1 + i_1^2 - 2i_1 + 4b - 4i_1 b}\right). \tag{9}$$

With the aid of a computer solution, it is a straightforward matter to solve Eq. (9) for i_1 as a function of v_i and with b as a parameter.

Remark 1. Note that Eq. (9) is only valid for $i_1 \in [0,1]$. This implies the solution is valid when

$$v_i \in \left[-\frac{1}{2}\left(1+\sqrt{1+4b}\right), \frac{1}{2}\left(1+\sqrt{1+4b}\right)\right], \qquad (10)$$

and when $v_i > \frac{1}{2}\left(1+\sqrt{1+4b}\right)$, $i_1 = 1$. On the other hand, $i_1 = 0$ when $v_i < -\frac{1}{2}\left(1+\sqrt{1+4b}\right)$. Furthermore, Eq. (9) was derived assuming that the transistors are in saturation region. Note that if the transistor goes into linear region when the current has completely switched to one of the branches, the above derivation still holds. The above derivation becomes invalid only if $V_{DS} < V_{DS,sat}$ for some transistor with v_i in the range given in Eq. (10). □

Remark 2. Consider the case when

$$v_i = \frac{1}{2}\left(1+\sqrt{1+4b}\right)$$

and $i_1 = 1$. We need to determine the conditions when M1 is in saturation for this case. Since $i_2 = 0$, $V_{GS_2} = V_t$ and therefore $V_S = -V_t$. Hence, $V_{DS_1} = V_t$ and

$$V_{GS_1} = V_t + V_a v_i,$$

and from Eq. (2) we have

$$V_{DS,sat_1} = \frac{(V_{GS_1} - V_t)E_{sat}L}{V_{GS_1} - V_t + E_{sat}L}, \qquad (11)$$

$$= V_a \frac{\frac{1}{2}\left(1+\sqrt{1+4b}\right)b}{\frac{1}{2}\left(1+\sqrt{1+4b}\right)+b}. \qquad (12)$$

Therefore $V_{DS} \geq V_{DS,sat}$ translates to

$$\frac{V_t}{V_a} \geq \frac{\frac{1}{2}\left(1+\sqrt{1+4b}\right)b}{\frac{1}{2}\left(1+\sqrt{1+4b}\right)+b}.$$

Usually this is not a very stringent condition and can be easily achieved in designs. Note that V_t is larger than V_{t_0} due to the body effect. □

A computer solution of Eq. (9) results in three possible solutions for i_1. Only one of these solutions behaves properly, i.e., for $i_1 = 1$ we have $v_i > \frac{1}{2}(1+\sqrt{1+4b})$ and for $i_1 = 0$ we have $v_i < \frac{1}{2}(1+\sqrt{1+4b})$. This behavior is shown in the plots of i_1 versus v_i for $b = 0, 1, \ldots, 5$ in Fig. 2. Notice that v_i is in the range given in Eq. (10).

B. Oscillator Universal Curves

The normalized current $i_1(t)$ do not appear to be expressible in a simple analytic solution; however, it is quite apparent that a Fourier series expansion of i can be used to express this waveform in terms of its average value and its harmonic components. Since the current waveform possesses odd symmetry and the driving signal is periodic, we then have

$$i_1(t) = i_{1,1}\cos\omega t + i_{1,3}\cos 3\omega t + i_{1,5}\cos 5\omega t + \ldots, \quad (13)$$

where

$$i_{1,k} = \frac{2}{\pi}\int_0^{\pi} i_1(t)\cos k\omega t \; \mathrm{d}\omega t.$$

A numerical solution can be used to derive the Fourier coefficients $i_{1,k}$ for the fundamental and the first several harmonics. Note that in order to calculate the harmonic components of the current, it is assumed that the voltage waveforms are almost sinusoidal. This, in general, is a valid assumption if the Q of the circuit is moderate, which we will assume. Table I presents $i_{1,k}(v_i)$ for $k = 1, 3, 5, 7$. The results of a computer numerical solution for the normalized drain current Fourier coefficients are shown in Figs. 3(a)-3(d). In these plots the odd harmonic currents are plotted as a function of v_i for various values of b. (Note that even harmonic currents are absent). The curves show a monotonic rise and represent the case where the device is always saturated. For the other curves in Figs. 3(c) and 3(d), the point where i_1 begins to fall at low v_i coincides with partial operation in the triode region. The waveforms in Figs. 3(a)-3(d) can be used to produce universal curves for oscillator design. Given v_i and b, these curves can be used to determine the Fourier coefficients in the Fourier series expansion of i_1 given in Eq. (13).

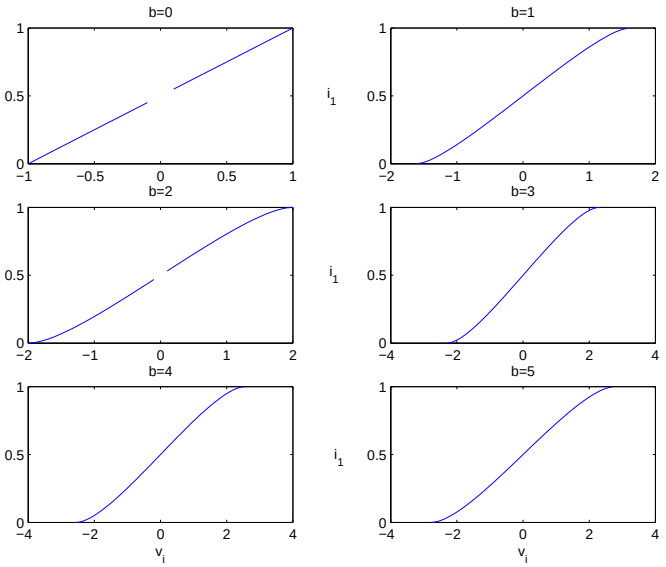
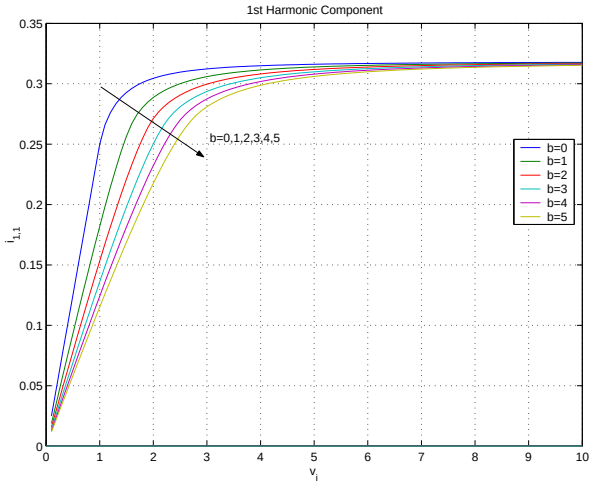


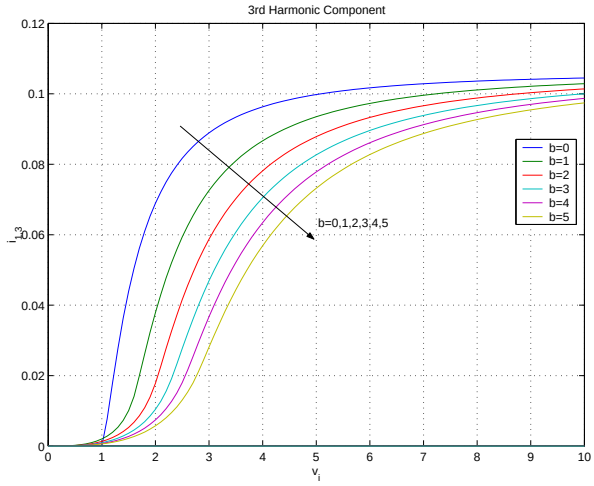
Fig. 2. Normalized drain current i_1 versus normalized signal voltage v_i for different values of b.

TABLE I
TABULATION OF $i_{1,k}$ VS. v_i FOR $b = 1$.

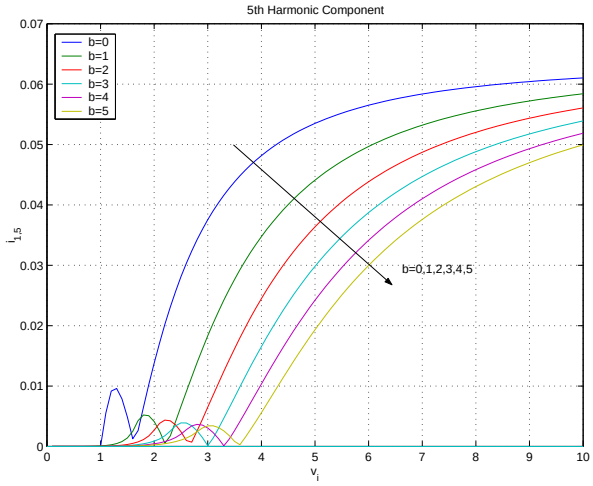
v_i	$i_{1,1}$	$i_{1,3}$	$i_{1,5}$	$i_{1,7}$
0.0	0.0000	0.0000	0.0000	0.0000
0.5	0.0931	—	—	—
1.0	0.1819	−0.0020	—	—
1.5	0.2567	−0.0101	−0.0014	—
2.0	0.2886	−0.0379	−0.0041	0.0026
2.5	0.3001	−0.0594	0.0066	0.0053
3.0	0.3059	−0.0726	0.0183	0.0011
4.0	0.3114	−0.0867	0.0347	−0.0113
5.0	0.3140	−0.0935	0.0441	−0.0209
7.0	0.3161	−0.0996	0.0532	−0.0316
10.0	0.3172	−0.1029	0.0584	−0.0383
∞	0.3183	−0.1061	0.0637	−0.0455



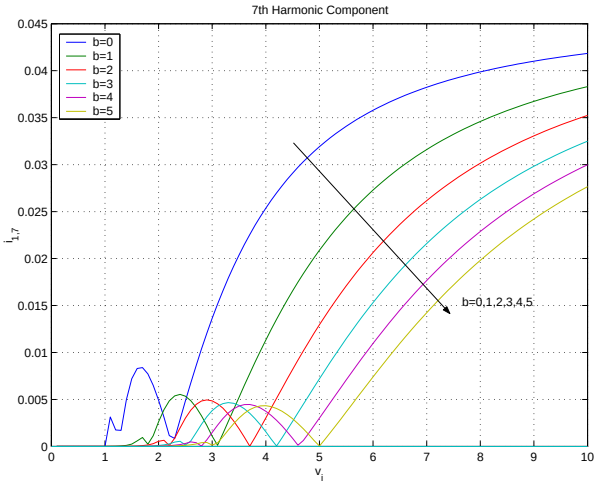
(a) 1st harmonic component



(b) 3rd harmonic component



(c) 5th harmonic component



(d) 7th harmonic component

Fig. 3. Normalized harmonic currents versus normalized signal voltage and parameter b.

A sketch of i_1 vs. wt, shown in Fig. 4, indicates how the waveform varies with v_i for $b = 2$.

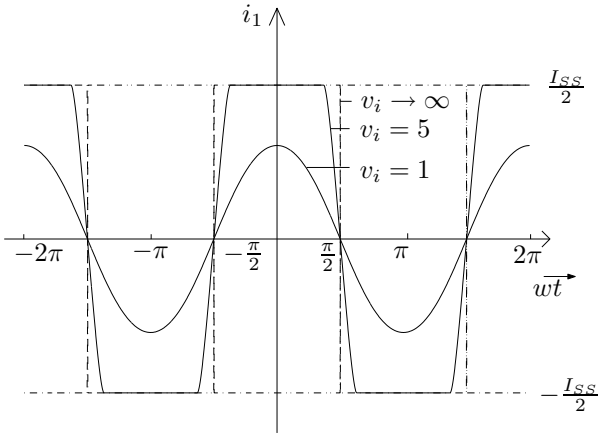


Fig. 4. Sketch of i vs. wt for different values of v_o.

C. Comparison of Analysis and Simulations

To confirm the validity of the proposed characterization technique we compare results of simulations and measurements of a 4.7 GHz oscillator with on-chip inductor [13] shown in Fig. 5. This oscillator is fabricated using 0.35 μm CMOS process and uses transistor parasitics for tank capacitors in the oscillator.

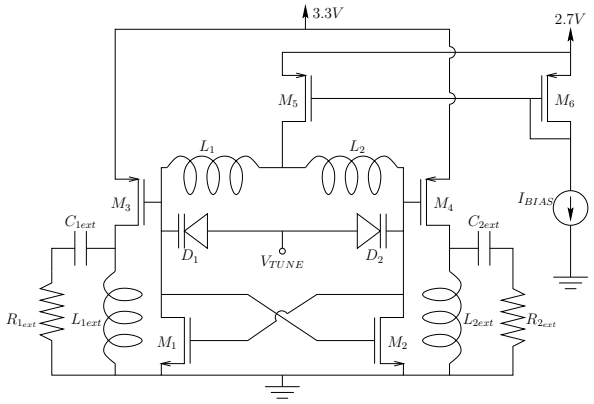


Fig. 5. 4.7 GHz oscillator with on-chip inductor.

Short-channel device model parameters were extracted for the specific technology by running test circuits to give: $v_{sat} = 86301.58$ m/s, $E_{sat} = 9.234\,\mathrm{V}/\mu$, and $V_t = 0.43$ V. All loading effects are conveniently reflected to the output and derived as an effective resistance R_L, seen at the drain

of M1. The output voltage amplitude was calculated using the first harmonic component of I_1 as $V_m = I_{1,1}R_L = 0.2\,\mathrm{V}$. The drain current I_1 can then be derived using the oscillator universal curves and plotted as seen in Fig. 6.

Waveform distortion in the oscillator voltage may be of importance in some applications and can be calculated as follows. Drain current in transistor M1 of Fig. 5 produces third, fifth, and seventh harmonics as given in Figs. 3(a)-3(d). Once these are known, the harmonic voltage in V_1 is readily calculated assuming that C_L is the dominant loading at the drain of M1 (the inductors are assumed an open circuit at all harmonics of the oscillation frequency). Table II lists the resulting normalized harmonic components. The nth harmonic distortion in V_1 is given by

$$\mathrm{HD}_n = \frac{I_{1,n}}{n\omega_0 C_L V_m}, \quad n = 3, 5, 7. \tag{14}$$

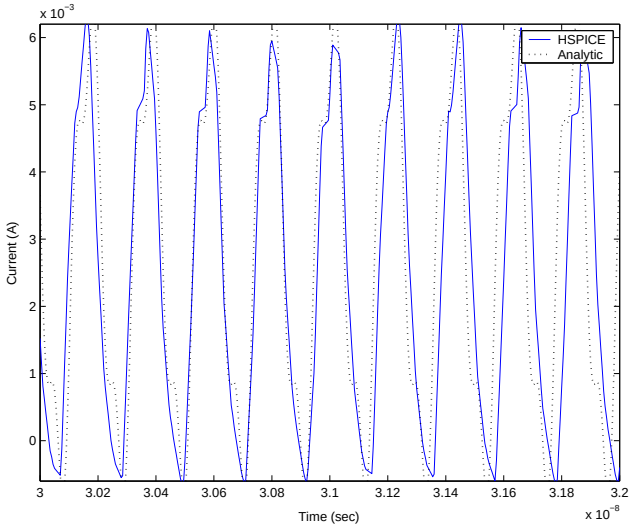


Fig. 6. Comparison between analytical results and HSPICE simulations for the estimated drain current I_1.

TABLE II
NORMALIZED HARMONIC COMPONENTS.

Frequency [GHz]	HSPICE† [$\times 10^{-3}$]	Analysis [$\times 10^{-3}$]
4.7847	1.00	1.00
9.5694	4.97	0.00
14.3541	29.82	26.92
19.1388	2.51	0.00
23.9235	5.91	4.97
28.7081	0.62	0.00
33.4928	1.77	1.50

† Even harmonics are present due to nonlinear capacitive parasitics that were not accounted for in the analysis.

IV. Conclusion

Quantitative analytical expressions for the cross-coupled LC-tank oscillator periodic steady-state solution have been derived. The derivation was based on MOS short-channel device equations assuming the transistors operate in the saturation region. The techniques presented for the cross-coupled oscillator are intuitive and allow for similar derivations for other oscillator topologies. The validity of the proposed analysis has been tested by comparing our analytical results with simulations of an actual fabricated and measured oscillator, where we find that our analysis is in good agreement with simulations as well as measured results.

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References

[1] M. Mansour, A. Mehrotra, W. Walker, and A. Narayan,"Analysis Techniques for Obtaining the Steady-State Solution of MOS LC Oscillators," *invited paper to be presented at IEEE ISCAS*, May 2004.

[2] A. Mehrotra, *ECE 452 Course Notes*, University of Illinois at Urbana-Champaign, 2001.

[3] A. Demir, A. Mehrotra, and J. Roychowdhury, "Phase noise in oscillators: A unifying theory and numerical methods for characterization," in *Proceedings of IEEE TCAS*, vol. 47, no. 5, pp. 655-674, May 2000.

[4] A. Demir, A. Mehrotra, and J. Roychowdhury, "Phase noise and timing jitter in oscillators," in *Proceedings of IEEE CICC*, pp. 45-48, 1998.

[5] A. Demir, D. Long, and J. Roychowdhury, "Computing phase noise eigenfunctions directly from steady-state Jacobian matrices," in *Proceedings of IEEE/ACM ICCAD*, pp. 283-289, 2000.

[6] R. Meyer, *EECS 242 Course Notes*, University of California at Berkeley, 1999.

[7] A. Mehrotra, *ECE 383 Course Notes*, University of Illinois at Urbana-Champaign, 2001.

[8] B. Razavi, *Design of Integrated Circuits for Optical Communications*. McGraw Hill, 2002.

[9] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw Hill, 2000.

[10] P. Gray, P. Hurst, et. al, *Analysis and Design of Analog Integrated Circuits*, fourth edition. John Wiley and Sons, 2001.

[11] P. Allen and D. Holberg, *CMOS Analog Circuit Design*, second edition. Oxford University Press, 2002.

[12] P. Ko, "Approaches to Scaling," *Chapter 1 in VLSI Electronics*, vol. 18, Academic Press, 1989.

[13] P. Kinget, "A fully integrated 2.7 V 0.35 μm CMOS VCO for 5 GHz wireless applications," in *Digest of Technical Papers of IEEE ISSCC*, pp. 226-227, 1998.