NSGA-Based Parasitic-aware Optimization of a 5GHz Low-noise VCO[1]

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Abstract—A parasitic-aware RF synthesis tool based on a non-dominated sorting genetic algorithm (NSGA) is introduced. The NSGA-based optimizer casts the design problem as a multi-objective optimization problem and offers multiple solutions along the Pareto optimal front. Monte-Carlo simulations are then performed to efficiently assess sensitivity at solution points with respect to process, voltage, and temperature (PVT) variations. An example design of a 10mW 5GHz voltage-controlled oscillator (VCO) in 250nm SiGe BiCMOS achieves a 12% tuning range with a phase noise of -133dBc/Hz at 3MHz offset. The Figure-of-Merit (FOM) is 188dBc/Hz and power-frequency-tuning normalized FOM (PFTN-FOM) is -4dB.

I. Introduction

The parasitic-aware synthesis paradigm was conceived to combat performance degradations owing to device and package parasitics to achieve optimum performance [1]-[4]. The parasitic-aware optimization methodology depicted in Fig. 1 comprises three major modules linked via a netlist: an optimization core, a parasitic-aware compact model generator, and a standard circuit simulator. The optimization core first modifies the design variables in the netlist according to a chosen optimization algorithm. The netlist is simultaneously updated with information from the compact model generator. A user-specified circuit simulator such as *HSPICE* or *SPECTRE* then simulates the parasitic-laden netlist. After simulation, the outputs are passed back to the optimization core for evaluation and generation of the new netlist variables. Without doubt, the most critical component in parasitic-aware synthesis is the optimization core. Previously, simulated annealing (SA) and particle swarm optimization (PSO) algorithms have been used to implement the core optimizer [1],[4]. Although both techniques have hill-climbing capabilities and can avoid being trapped in local minima, each has shortcomings. Both techniques scale a set of design objectives into a single optimization objective (fitness or cost function) by multiplying each design objective by a user-defined weight [5]. Even though this weighted-sum approach is intuitive and easy to implement, potential high sensitivity solutions to weight variations makes the task of setting the weight factors problematic [6]. This often results in sub-optimum solutions. In addition, the computational efficiency of SA is relatively low because it works with a single-point solution rather than a population of solutions [1], [4]-[7].

In this paper, a parasitic-aware optimization technique based on a non-dominated sorting genetic algorithm (NSGA) is introduced. Like PSO, NSGA works with multiple points in the solution space to achieve high computational efficiency. But unlike the two previously described methods where the weighted-sum cost function leads to a single solution, a non-dominated sorting loop is introduced to distribute the population of solutions along the Pareto optimal front. Monte-Carlo simulations are then efficiently run to assess sensitivity of each solution point with respect to process, voltage, and temperature (PVT) variations [4]. The new techniques are validated in the design and optimization of a 5GHz voltage-controlled oscillator in a 250nm SiGe BiCMOS technology. Section II briefly outlines the topology and design of the VCO. A description of NSGA is presented in Section III. Section IV shows results including Monte-Carlo simulations with PVT variations for maximizing circuit robustness, and Section V concludes the contribution.

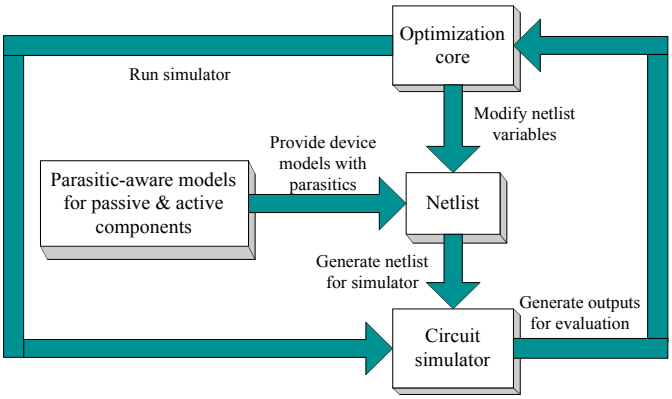

Fig. 1: The parasitic-aware synthesis paradigm for the design and optimization of radio frequency integrated circuits.

II. Voltage-Controlled Oscillator Design

One of the key RF circuit blocks in realizing integrated communication systems is the voltage-controlled oscillator. In the past few years, VCO performance has improved dramatically due to continuous research efforts aimed at circuit innovations and process improvements. But as carrier frequencies continue to move to higher regions of the available frequency spectrum, VCO design is becoming increasingly more challenging since parasitics associated with both on-chip passive and active components and the package have greater impact on circuit performance [1].

Figure 2 shows a schematic of a complementary cross-coupled VCO in CMOS technology. The cross-coupled NFET and PFET pairs form two small-signal negative resistance generators that compensate resistive losses in the LC tank circuit. Advantages of the complementary topology over its NMOS- and PMOS-only counterparts include larger output swing for the same power dissipation and better rise and fall time symmetries [8]. Accumulation mode MOS varactors and switched-capacitor circuits are used to achieve a relatively linear tuning behavior and reduce VCO gain, respectively [9]. Note that only a single switched-capacitor is implemented in this design to reduce the number of probes required during testing; of course, additional switched-capacitor branches are easily added for greater control of the VCO center frequency and gain. The product of the tank inductance and its quality factor (Q) is maximized to maximize output swing and minimize phase noise [10]. To

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reduce flicker noise up-conversion, tail resistor R_T is used for biasing the VCO instead of an NMOS current mirror [12]. Inductor L_T is inserted in series with the tail resistor R_T to provide high impedance at the second harmonic frequency. The oscillation frequency is determined by the tank inductance (L) and the variable plus parasitic capacitances ($C_{var\text{-}nominal}$ and $C_{parasitic}$, respectively):

$$f_{osc} = \frac{1}{2\pi\sqrt{L\cdot\left(C_{var\_nominal} + C_{parasitic}\right)}} \quad (1)$$

The tuning range, which is usually expressed as a percentage of the center frequency, is defined as:

$$\text{Tuning range} = \frac{f_{max} - f_{min}}{f_{osc}} \times 100\% \quad (2)$$

where f_{max} and f_{min} are maximum and minimum oscillation frequencies, respectively. The phase noise of the VCO can be computed using a linear time-variant equation from [8]:

$$\mathcal{L}\{\Delta\omega\} = 10\cdot\log_{10}\left[\frac{\Gamma_{rms}^2}{q_{max}^2}\cdot\frac{\bar{i}_n^2/\Delta f}{2\Delta\omega^2}\right] \quad (3)$$

where $\Delta\omega$ is the offset frequency from the carrier, $\bar{i}_n^2/\Delta f$ is the power spectral density of the current noise source, q_{max} is the maximum charge swing, and Γ_{rms} is the root-mean-square value of the effective impulse sensitivity function.

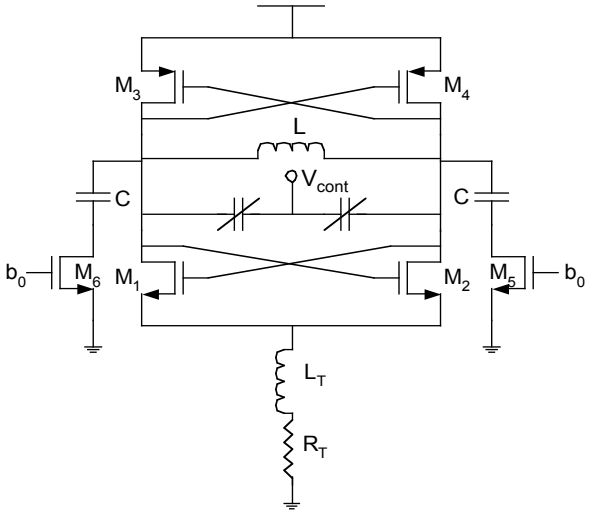

Fig. 2: A complementary cross-coupled CMOS LC tank voltage-controlled oscillator with fine (varactor) and coarse (switched-capacitor) center frequency controls.

The objective here is to use the new NSGA-based optimization tool and its associated design centering methodology to synthesize a 5GHz VCO that meets or exceeds the following design specifications: output phase noise < -130dBc/Hz at 3MHz offset, tuning range > 10%, minimum VCO gain, and a maximum power dissipation of 10mW. Because the design constraints are set at a fairly demanding level of performance, conventional manual design methods are sufficiently inaccurate and cumbersome that an optimum design is highly unlikely without CAD synthesis. In particular, this challenge necessitates the use of a design and optimization tool that includes device and package parasitics as part of the design process from the beginning of the design.

III. NSGA-Based Parasitic-Aware Optimization

Inspired from Darwin's theory of evolution, the genetic algorithm (GA) has been used extensively in various forms in optimization tools over the last two decades. As illustrated in Fig. 3, the GA begins by generating a population of random solutions with each solution (individual) represented by a bit string called chromosomes. A user-defined fitness function is then evaluated for each individual in the population to determine its probability of reproduction. Three operators are applied to the current population to determine the next population: reproduction, crossover, and mutation. The reproduction operator places individuals from the current population into the next based on their fitness values. A number of methods exist for implementing the reproduction operator. The most common ones are the roulette wheel, the ranking method, the binary tournament method, and the Pareto domination tournament that is chosen for this work [5], [6], [11]. If two randomly chosen individuals are compared, and one is superior to the other in every objective, it is called the dominant solution; the other is referred to as the dominated solution. On the other hand, if each is better than the other in some objective, then the two individuals are said to be non-dominated. Individuals with high fitness values have a higher probability of reproducing than individuals with low fitness values, thus guaranteeing that bad solutions are eliminated through the evolutionary process. The crossover operator takes two randomly chosen individuals and swaps their chromosomes at a random position within the bit string. The mutation operator then randomly flips a bit in the chromosomes of one or more randomly selected individuals based on a user-defined mutation coefficient. The purpose of the crossover and mutation operators is to introduce new solutions to the population. The process continues until the desired solution is found or the specified number of iterations is reached.

Two major drawbacks exist for conventional optimization techniques (original GA, PSO, etc.) that combine multiple objectives into a single cost function: sensitivity to weight variations as mentioned in Section I, and objective conflict. In real-world multi-objective optimization problems, optimal solutions for each individual objective are different. A solution that optimizes all objectives does not usually exist. Mathematically, the most favorable solution is the one with the least objective conflict but there is no guarantee that such a solution will satisfy the problem requirement.

NSGA was introduced in [11] to obtain good solutions as well as to maintain a stable sub-population by using both a ranking method and a niche mechanism. Figure 4 shows an NSGA flow chart. The main difference between the original GA and NSGA is in how the reproduction operator is handled. The crossover and mutation operators remain unchanged. For the Pareto domination tournament method, two candidates are randomly picked from the population. Instead of comparing them based on their scaled fitness values, a set of individuals randomly chosen from the population is used for comparison. Each candidate is then compared against every individual in the comparison set. If one candidate is dominated by the comparison set while the other one is not, the latter is chosen for reproduction while the dominated solution is aborted. On the other hand, if both members of the pair are non-dominated, a niche count is found for each by counting the number of points in the population within a certain distance σ from that individual. The normalized Euclidean distance d_{ij} between two solutions i and j is calculated as

$$d_{ij} = \sqrt{\sum_{k=1}^{n} \left(\frac{x_{k,i} - x_{k,j}}{x_{k,\max} - x_{k,\min}} \right)^2} \quad (4)$$

where $x_{k\text{-}min}$ and $x_{k\text{-}max}$ are the minimum and maximum constraints for the *kth* variable in each solution, and *n* is the total number of variables for a solution. The candidate with the smallest niche value is passed onto the next generation. The niche mechanism prevents quick convergence toward a single solution, and thus guarantees diversity in the population. Based on the literature and extensive simulation results, a value of σ = 0.5 is chosen [5], [11].

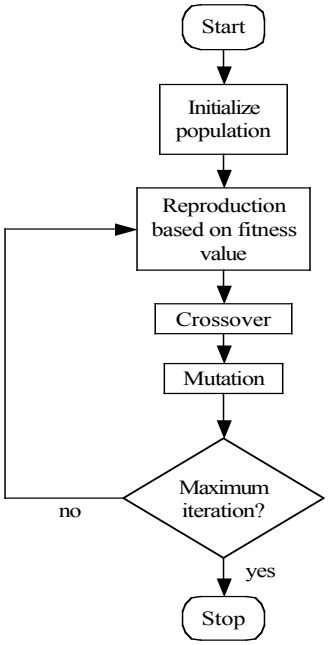

Fig. 3: Basic genetic algorithm flowchart.

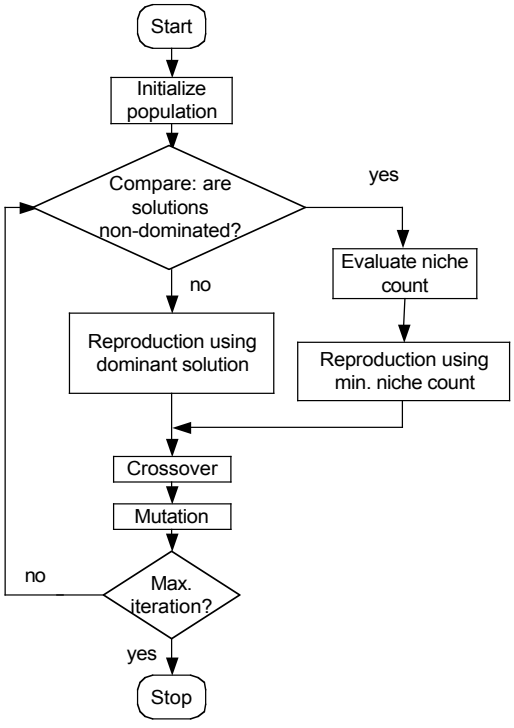

Fig. 4: NSGA flow chart.

IV. Optimization Results

The design of the VCO is carried out using 250nm SiGe BiCMOS process parameters. The optimizer interfaces with the *Cadence Design Systems SPECTRE-RF* simulator so phase noise is readily computed. The widths and lengths of the PMOS and NMOS devices, the number of fingers in the layout of the MOS varactors, and the size of the switched-capacitors constitute the set of design variables. The coarse-tuning NMOS switches are sized so their on-resistances do not significantly load the LC tank. Initially, the inductor value is fixed in a simulation run due to the unavailability of compact models for the parasitic components versus continuous inductance values. Multiple simulations were run with different discrete inductance values to yield an oscillation frequency of 5GHz. The power dissipation is set to the maximum specified value of 10mW throughout the optimization process. The number of individuals in the population is 32, and the maximum number of iterations is 50. The number of bits in the bit string representing the design variables is determined by the minimum and maximum constraints placed on the variables. In our simulations, each design variable is represented by a nine-bit word. Convergence for NSGA is achieved when the optimizer stops introducing new solutions along the Pareto optimal front. The simulation times for the GA, PSO, and NSGA are compared in Table 1. Due to the insertion of the non-dominated selection loop, NSGA consumes about 20% more simulation time compared to GA and PSO. All simulations are carried out on Sun Fire V480 servers with 900MHz UltraSparc-III processors. Figure 5 compares the solutions in the final objective space between ordinary GA, PSO, and NSGA. Both conventional GA and PSO yield only a single-point solution along the Pareto optimal front for a single optimization run while NSGA provides 12 solutions in this example among the continuum of design variable trade-offs.

Table 1. Efficiency comparison of GA, PSO and NSGA.

	GA	PSO	NSGA
Simulation time	40 hours	38 hours	46 hours

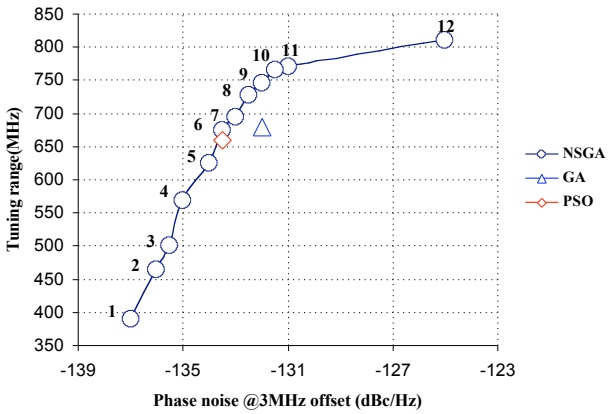

Fig. 5: Objective space comparison between GA and NSGA.

In order to assess the sensitivity of the solutions to PVT variations, post optimization PVT analysis using Monte-Carlo simulations was performed at each solution point assuming Gaussian distributions with σ = 20% standard deviations in all passive device values and the power supply voltage, σ = 1% deviations in all active device geometries,

and □ = 10% deviations in the threshold voltages. The operating temperature is randomly varied from 0 to 75°C. Figure 6 shows the average tuning range versus the average phase noise for 250 Monte-Carlo simulations at each solution point. As expected, it is in close agreement with Fig. 5. Figure 7 shows the standard deviation of the tuning range versus that of the phase noise for each solution point. Based on the resulting statistics, design points 8 and 12 represent the most robust and manufacturable designs because they exhibit the lowest sensitivity characteristics. A yield analysis using the obtained statistical information is performed for each solution point based on the 10% tuning range requirement and the -130dBc/Hz@3MHz offset phase noise specification. The yield distribution is assumed to be Gaussian and the results are shown in Table 2. Clearly, design point 8, which is chosen to be the final design, meets the design specifications and offers excellent yield performance.

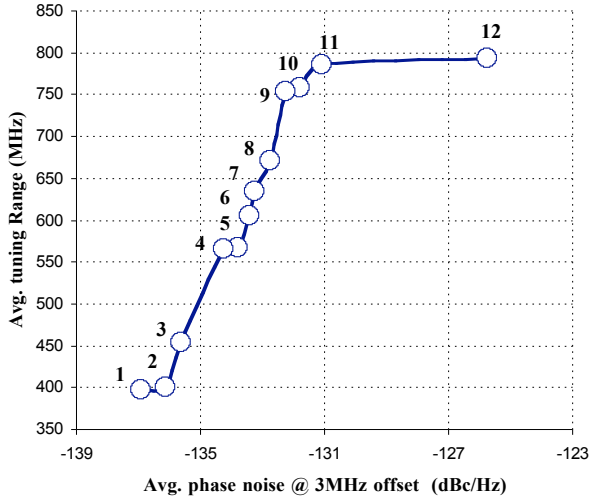

Fig. 6: Post optimization PVT analysis results: average of tuning range versus average of phase noise for 250 Monte-Carlo simulations per point.

Figures 8 and 9 show the nominal phase noise and tuning plots of design point 8, respectively. The post optimization PVT simulation plot is shown in Fig. 10. The design specification and the achieved results are summarized in Table 3. The VCO Figure-of-Merit (FOM) and Power-Frequency-Tuning-Normalized Figure of Merit (PFTN-FOM), two frequently-used parameters to compare performances of VCOs at different frequencies, are defined in (5) and (6), respectively:

$$FOM = 10 \cdot \log\left[\left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1}{10^3 \cdot P \cdot L\{\Delta\omega\}}\right] \quad (5)$$

$$\text{PFTN}\_\text{FOM} = 10 \log\left[\frac{kT}{P}\left(\frac{\omega_{tune}}{\Delta\omega}\right)^2 \frac{1}{L\{\Delta\omega\}}\right] \quad (6)$$

where ω_0 is the center frequency, P is the power dissipation in Watts, k is the Boltzmann's constant, T is the absolute temperature in degrees Kelvin, ω_{tune} is the tuning frequency, and $\Delta\omega$ and $L\{\Delta\omega\}$ are the offset frequency with respect to the carrier and its associated phase noise [8]. Simulation of the final design achieves a FOM of 188dBc/Hz and a PFTN-FOM of -4dB.

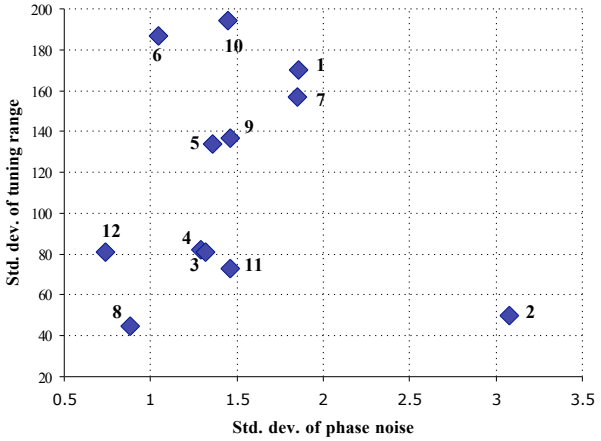

Fig. 7: Post optimization PVT analysis results: standard deviation of tuning range versus standard deviation of phase noise for 250 Monte-Carlo simulations per point.

Table 2. Yield analysis based on Gaussian distribution.

Design point	Yield based on 10% tuning spec (%)	Yield base on -130dBc/Hz @3MHz phase noise spec
1	19.00	99.99
2	0.07	97.64
3	10.00	99.99
4	53.00	99.95
5	52.00	99.75
6	60.00	99.95
7	69.00	95.63
8	99.32	99.9
9	93.00	93.92
10	86.00	89.17
11	99.90	77.06
12	99.81	0

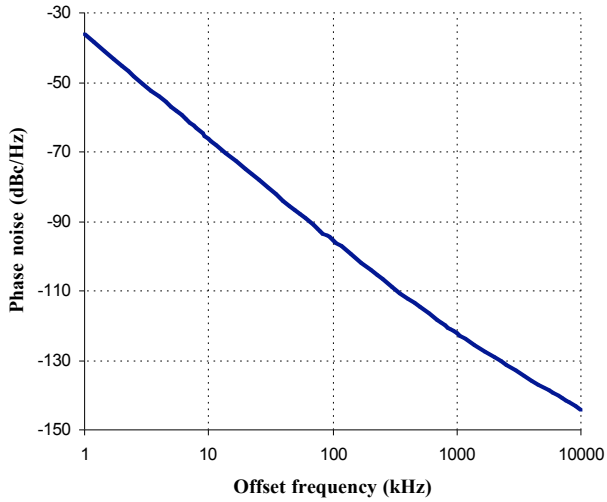

Fig. 8: VCO phase noise plot.

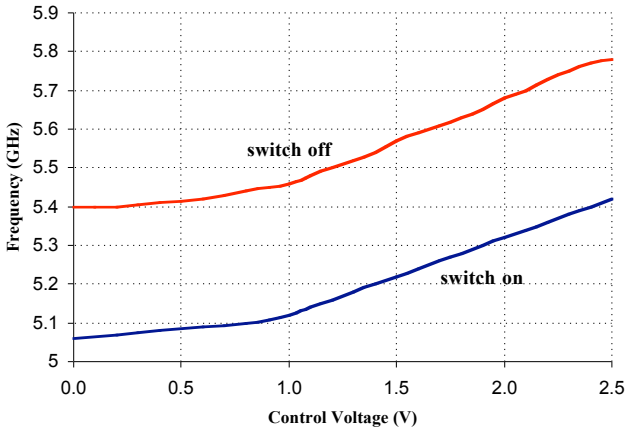

Fig. 9: VCO tuning plot.

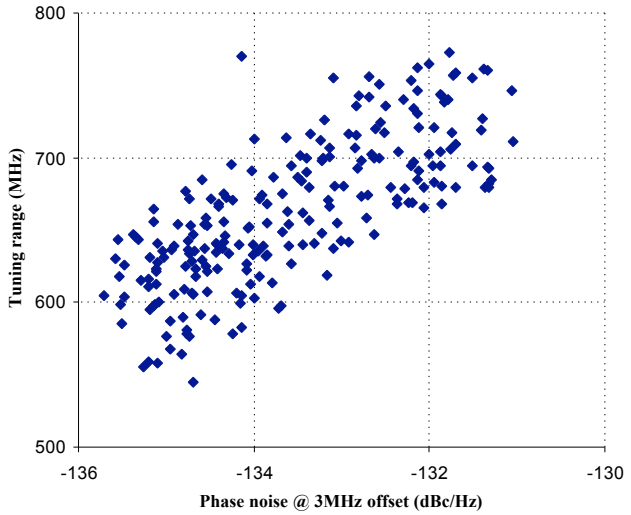

Fig. 10: Post PVT optimization of the final design.

Table 3. VCO Performance summary.

	Desired spec.	Achieved spec.
ω_0	5GHz	5.6GHz
Tuning	10%	12%
VCO Gain	Minimize	130MHz/V
Phase noise	Minimize	-133dBc/Hz@3MHz
Power	10mW	10mW
FOM	/	188dBc/Hz
PFTN-FOM	/	-4dB

V. Conclusions

In this paper, a parasitic-aware optimization tool based on a non-dominated sorting genetic algorithm (NSGA) is presented. The tool is applied to the design and optimization of a 5GHz VCO in a 250nm SiGe BiCMOS process. The optimized results include a 5.6GHz center frequency, -133dBc/Hz phase noise at 3MHz offset, and a 12% tuning range with 10mW of power dissipation. The FOM and the PFTN-FOM achieved are 188dBc/Hz and -4dB, respectively. The NSGA-based parasitic-aware optimization methodology shows promising potential for future mixed-signal and RF applications due to its capability to generate multiple solutions along the Pareto optimal front as well as its efficiency in parallel execution.

VI. References

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