# On Mismatch in the Deep Sub-Micron Era - from Physics to Circuits*

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**Abstract— Rapid decrease in feature sizes has increasingly accentuated the importance of matching between transistors. Deep sub-micron designs will further emphasize the need to focus on the effects of mismatch. Furthermore, increased efforts on high level analog device modeling will necessitate accompanying mismatch simulation and measurement methods. The deep sub-micron era forces circuit designers to learn more about the physics and the technology of transistors. This study introduces a method and assists circuit designers in including this method in their traditional design flow of circuits. By proposing a solution to the problem of building a modeling bridge between transistor mismatch and circuit response to it, we hope to enable designers to incorporate low level mismatch information in their higher level design.**

## I. Introduction

In the real world, it is hard to match two objects exactly. This is a well known fact for people working in the manufacturing industry. Most of the time, objects are manufactured within certain accuracy tolerances. The same situation can be attributed to the manufacture of transistors. But for transistors, matching becomes highly crucial, as opposed to, say the matching between the sizes of two circuit packages. Due to its special condition, matching in transistors deserves a deeper understanding. Even if we had modelled mismatch between two transistors, without having a relationship defining how the circuit works under mismatch between these two transistors, the resultant model would essentially prove useless. Incorporating the effects of mismatch on the properties of a circuit and building a modeling bridge between the mismatch in two transistors to influents causing this mismatch are crucial problems that need to be addressed.

Appropriate handling of mismatch necessitates a precise definition. Mismatch is intricately tied to the issue of process variations. Process variation is the deviation of process parameters from their nominal values. Mismatch is caused by the combined effects of global, local and random variations, minus the amount that affects both transistors in question equally. Process variations can affect all the transistors equally without any mismatch in transistor pairs by setting the complete set of nominal values to new ones in a circuit. However, it is highly unlikely that all the transistors will be affected equally, even if they had been designed to be precisely equal in terms of dimensions and operating points. This can largely be attributed to the increased effect of random variations in deep sub-micron circuits. In a circuit, variations will follow a distribution, typically quite close to a Gaussian distribution.

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Previous modeling approaches for mismatch are insufficient in addressing the needs of the deep sub-micron era. A typical source of error in current mismatch models stems from distributing mismatch between two transistors equally, whereby the parameter of one transistor is increased above its nominal value and the same parameter of the other transistor is decreased equally in absolute terms from its nominal value [5]. This may provide incorrect results, as the values of the parameters of both transistors may be below their nominal values as opposed to one parameter being below and the other one being above the nominal value.

Iterative modifications to hand-design, which necessitate intuition and textbook based formulas, bring forth the necessity for more simulations. With a suboptimal hand-design, one ends up sitting in front of a computer trying to optimize the circuit for considerable periods of time. A method apparently is needed which can be applied during a hand-design stage to reduce the number of cycles between the simulator and manual design.

Effects of mismatch have been observed in the transistor level only. Yet intuitively, a comprehension of the effects of mismatch to circuit sub-blocks and circuits is highly desirable. To avoid errors, various parameter values and corresponding distributions between p-type and n-type transistors should be paid attention to, as we strive to do in this study.

Having even approximate formulas for circuit design is quite valuable. Most of the time, these formulas are used instead of simulators, especially for analog design. Research is needed to establish a way to transfer the analogous convenience and design speedup to mismatch analysis. We designate such an approach as a *hand-calculation method* for mismatch and suggest that it avoids the expenditure of unnecessary hours trying to optimize the circuit using simulation outputs only, as the proposed method provides a significant design speedup right upfront.

We hypothesize that in the next few years, there will ensue a shift towards the use of statistical transistor models in simulators. Increased computer speeds will help complete these statistical simulations rapidly. The gap between netlist and circuit schematics should be dealt with by indicating the pair of transistors that can be involved in mismatch. Monte Carlo Analysis (MCA) based simulation techniques presented in this paper will be of paramount importance in helping to achieve the transition from current simulators to next generation ones. With the approaches presented, analog behavioral modeling of circuit blocks for mismatch can be performed; the consequent models can be used in an HDL like Verilog-A. Helping speed up simulations, the proposed method can also help the testing of mismatch for a particular circuit block. The use of probability distribution functions (pdf) will help fast and efficient analog behavioral

modeling for mismatch with current CAD tools. Improvements to the circuit block can be translated to its behavioral mismatch model and resimulated, thus helping engender mismatch modelled circuit libraries.

## II. Previous Work on Mismatch

Circuit designers have been trying to deal with mismatch for decades. The first approaches were in the form of circuit optimization. These kinds of studies are circuit specific and are not easily generalizable [6]. Such approaches by themselves are no longer adequate in preventing mismatch, since most of the time, process variation effects are compensated in these optimizations instead of mismatch. An alternative approach for dealing with mismatch consists of layout optimizations. Being able to compensate for local variations, this technique is of limited relevance to the problem of random variations. This technique has its limits, too, as layout optimizations may consume significant time; furthermore, targeting the challenging problem of balancing the interconnect between the two transistors for which mismatch compensation is targeted, remains still outstanding. Additionally, layout optimizations suffer from the restriction to linear optimizations as transistors have rectangular shapes, whereas parameter distributions have non-linear distributions.

In addition to designing circuits to accommodate mismatch, *modeling* mismatch has also attracted attention. Mismatch has initially been attributed to electrical or empirical parameters [1],[5],[7],[8]. This approach though has introduced significant levels of error as Taylor series have been used with only first order, i.e. linear, terms to define the relationships between circuit parameters.

A second generation of work in the literature has approached the problem in terms of BSIM parameters [2],[3]. The Principal Component Analysis (PCA) technique has been used to attribute a weight to all parameters [9]. These weights represent essentially a model of the degree of influence to mismatch on each parameter. Unfortunately, PCA does not incorporate a consideration of the possible dependence between SPICE parameters. BSIM has quite a number of empirical parameters, most of which are determined by parameter extraction. The meaning of assigning a weight to a parameter that itself is found by using a parameter extraction method is arguable. Also, correlations between each parameter need to be measured in PCA. However, the correlation coefficient is, by definition, a linear relationship with no non-linear content in it, hence causing inaccuracies. Non-linear PCA has also been researched and applied in signal processing research [10]. This approach has not been applied to mismatch yet. But even this possible augmentation of the PCA approach will still exhibit important challenges, primarily due to the inaccuracy caused by the application of this method to extracted parameters.

The establishment of the defining relationships between mismatch and its influents remains largely an open problem. An initial step in this direction has been undertaken in [4] with mismatch attributed to physical parameters. The work mentioned in this paper targets the same research space.

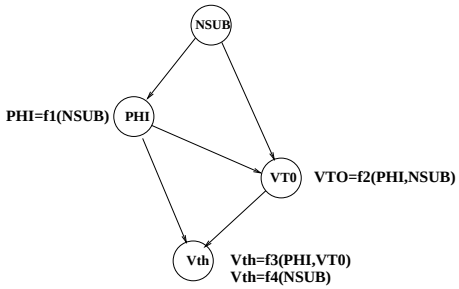


Fig. 1. Target Parameter *Vth* with source parameter *NSUB*

## III. Simulation and Measurement Methodologies

### A. Terminology and Methods

Correctly simulating mismatch is of high importance in circuits. Wrong simulation methods will result in unnecessary optimizations to the circuit, increasing design time, and even possibly causing a failing circuit. Designers have been using MCA in order to observe the effects of mismatch. More runs will give better histograms, as the distributions to parameters are scanned more evenly. The smoother the histogram, the closer an approximation to the probability distribution function (pdf) for the target parameter is attained.

Selecting which parameters to assign distributions to is crucial in MCA. The relation of parameters to each other is very important in making these assignments. Obviously, we need to assign the distributions to parameters which are independent. Interestingly, many designers fall victim to the fallacy of assigning distributions to parameters that are not independent but correlated. Yet in the deep sub-micron era, this kind of an approach can be tolerated no longer, as circuits are designed with very strict operating regions. Independence between two or more parameters implies that these parameters are not all a function of some common parameter. If, instead, dependent parameters are assigned distributions in MCA, we will end up with results that are incorrect. An independent assignment to correlated parameters produces an estimate that is more pessimistic than a "worst-case analysis", as points in the result space of a worst-case analysis should by definition be at least attainable.

In order to select which parameters are going to be assigned the distributions, a solid understanding of the relationships between these parameters is necessary. *Connectivity graphs* are introduced to capture these relationships. Fig. 1 shows one example of such a graph. The relationships of a number of SPICE parameters are indicated in the figure. The parameter at the tip of an arrow is a, possibly non-linear, function of the parameter at the tail. In this graph, *VT0* and *PHI* are both functions of *NSUB*. *Vth*, on the other hand, is a function of *VT0* and *PHI*. This implies that in determining *Vth* or any other parameter which is a function of *VT0* and *PHI*, *VT0* and *PHI* can no longer be treated as independent. The parameters in the example are chosen as SPICE parameters. More generally, these could be circuit level parameters such as $g_m$, $Gain$, $I_D$, etc. We denote parameters like *Vth* in the above example as the *target parameters*. The target parameter is the one that is the output of an MCA. It can be

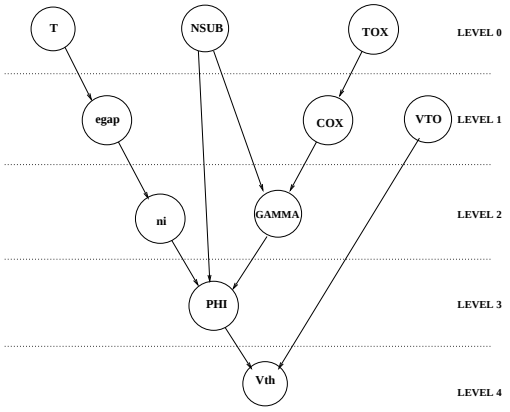


Fig. 2. Target parameter *Vth* with source parameters *T, NSUB, TOX, VT0*

inferred from Fig. 1 that even if there is no direct arrow between *Vth* and *NSUB*, due to the remaining dependencies, *Vth* can be expressed as a function of *NSUB*. Obtaining this new function is just a matter of substituting the formulas of *NSUB* and *VT0* into the function of *Vth*. The new function is denoted f4 in the figure, with different numbers indicating distinct functions.

Looked at from another perspective, the main idea of applying MCA is to obtain a pdf for a high level target parameter. The obvious reason is that we do not have direct accurate formulas to calculate a target parameter using its constituents, necessitating an approximation of the pdf using MCA. High level in this context implies that the parameter in question is a circuit parameter rather than a SPICE parameter. Circuit parameters can be considered to start with $I_D$ at the lowest level. The gain of an amplifier, Common Mode Reject Ratio (CMRR) or Power Supply Reject Ratio of an OpAmp can be considered to be high level circuit parameters. Almost all the formulas used to find high level circuit parameters in circuit design are essentially good approximations. They are often sufficient in providing us insight but fail consistently to deliver simulation accurate results. Simulation accuracy, however, hinges on the fact that simulations are performed using transistor level formulas, and these formulas are propagated through high level parameters using basic circuit rules. So in a way, a target parameter is being written as a function of low level parameters.

SPICE parameters have various dependencies between them. This stems from the fact that SPICE models exploit parameter fitting and extraction. A manufacturer provides SPICE parameter extraction and test results to the circuit designer in the form of *modelcards* for a particular technology. There exists a choice in selecting which parameters to extract, and which parameters to derive in terms of these while creating SPICE modelcards. This stems from the fact that SPICE parameters may either have a physical meaning or may just be a fitting parameter in a function. Basically, some parameters are not given in modelcards, but are calculated from the given ones[1]. In our case, this choice determines the shape of our connectivity graph and defines which parameters to use as *sources* in these graphs. For example, *NSUB* can be considered a source parameter in Fig. 1. The reason that the designer has to make such a choice in assigning source parameters and building the connectivity graph stems from the fact that one has to use the supplied SPICE parameters in order to make an inference about mismatch, as these parameters are extracted over the lifespan of the corresponding technology.

[1] This could result in a small deviation between the two transistor models.

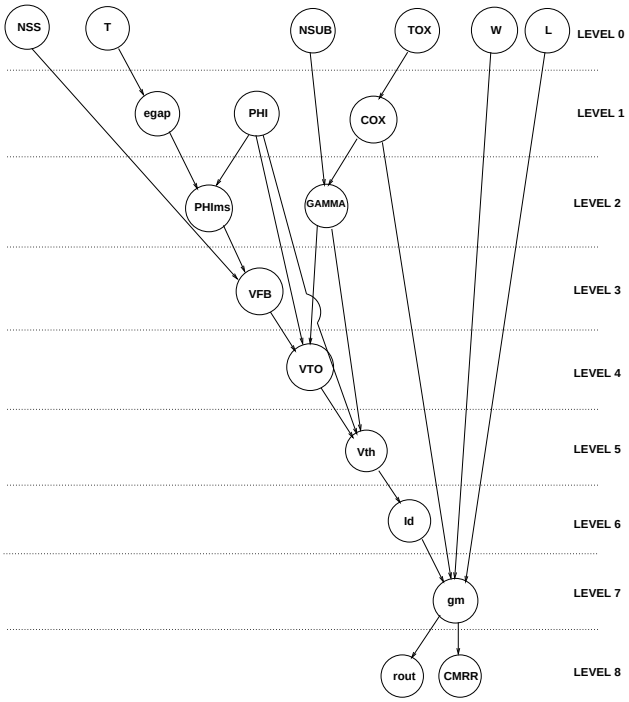


Fig. 3. Target parameter *Vth* with source parameters *NSS, T, PHI, NSUB, TOX*

Fig. 2 shows another connectivity scenario. This time, *VT0* is not calculated, but is given in the modelcard directly. This means that *VT0* is a *fitted* parameter found by the extraction process, implying that it may be a fitting constant in some formula or that it may have been measured on a graph. In this figure, the *level* terminology is introduced denoting the hierarchy between parameters. Level 0 parameters should be given special attention, as they are purely physical parameters, i.e., source parameters according to our definition. Basically, parameters at a higher level will be functions of the ones at lower levels. *VT0* does not have a direct physical meaning, so it is not included in Level 0 parameters, although it is a source parameter according to our definition. Not all source parameters are at Level 0 though, since they may represent fitted SPICE parameters.

Fig. 3 shows a connectivity scenario for an OpAmp. In this scenario, *PHI* has a physical meaning, but it is not included in Level 0 parameters. It is desirable to know the distributions of Level 0 parameters as it is best to assign these parameters independent distributions so as to determine the effects of mismatch at higher level parameters. Assigning a distribution to a source parameter that is not at Level 0 (such as *PHI* in the figure) will introduce errors to the proposed analysis. This is because parameters that are not at Level 0 are either fitted parameters or they are parameters that are calculated from other parameters in the graph. As a result, *PHI* is not assigned a distribution in Fig. 3.

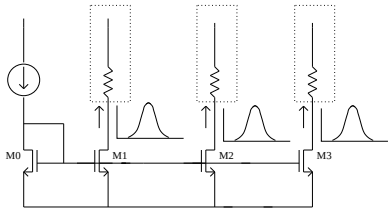


Fig. 4. Current mirror

As can be noted, *Vth* is a common parameter in both connectivity graphs, while both have different source parameters and different dependencies. *W* and *L* in the formula of $g_m$ are considered to be Level 0 parameters as it is safe to assign distributions to them. CMRR and $R_{out}$ are the target parameters.

The flexibility of connectivity graphs derives from the fact that we can consider them piecewise, like taking the *boundary cells* connected to the target parameter with a single edge and the target parameter apart. Assigning a precalculated distribution to the boundary cells directly will not cause correlation errors because calculation of the distributions of boundary cells will be performed using the full connectivity graph.

### *B. Application of the Simulation Method*

Fig. 4 shows the basic circuit that has been utilized in the literature for mismatch modeling. M0 is the *reference* transistor, and M1, M2 and M3 are used to mirror the current flowing through M0. We will call each of M1, M2 and M3 a *dependent* transistor. Furthermore, we will *group* a reference transistor and a dependent transistor during our mismatch analysis. In this circuit, the effects of mismatch in the $I_D$, i.e. the drain current, constitute the main target; we therefore want to find the pdf of $I_D$. Assuming an ideal reference, each drain current will have a probability distribution. If the transistors are identical, this distribution will be the same. It is interesting to find the same property, the pdf, between these branches when mismatch is actually causing a different current to flow through them. Prior to this study, mismatch was assumed to be occurring equally separated between the parameters of two transistors [5]. This assumption has tempted the model developers to distribute mismatch generating parameter variances equally between each transistor, i.e., the dependent and the reference ones here. However, it is overlooked that the corresponding parameters in this transistor pair could both rise above their nominal values, yet be equal. This situation can happen due to process variations. Distribution of mismatch independently to each transistor introduced in this study avoids such a fallacy.

The idea of representing target parameters as pdf's allows us to treat the pdf as a signal, hence giving us the ability to carry this mismatch information between circuit sub-blocks as if it were an ordinary signal, such as current. This idea is proposed to constitute a bridge between mismatch modeling and high level analog CAD design approaches. Mismatch and high level design ideas should be combined to speed the analog design process so that it can cope with digital design speed and technology.

In Fig. 4, mismatch information is supplied as input to the dotted squares. These dotted squares, here containing a resistor, can be any circuit block. The target parameter, current, in the current mirror sublock, becomes a source to another block. By this approach, the mismatch information is communicated between blocks, reaching the circuit output at the end.

TABLE I
MEASURED SENSITIVITIES

| $S_{id_2}^{L_1}$ | $S_{id_2}^{W_1}$ | $S_{id_2}^{TOX_1}$ | $S_{id_2}^{UO_1}$ | $S_{id_2}^{XJ_1}$ | $S_{id_2}^{NCH_1}$ | $S_{id_2}^{id_1}$ |
|---|---|---|---|---|---|---|
| 0.744 | -0.63 | 0.333 | -0.178 | -0.04 | 0.10133 | 0.86 |
| $S_{id_2}^{L_2}$ | $S_{id_2}^{W_2}$ | $S_{id_2}^{TOX_2}$ | $S_{id_2}^{UO_2}$ | $S_{id_2}^{XJ_2}$ | $S_{id_2}^{NCH_2}$ | |
| -0.786 | 0.648 | -0.3466 | 0.178 | 0.0433 | -0.010133 | |

We have stated that simulations are accurate since they are performed using lowest level parameters. A similar approach can be exploited to simulate or model mismatch. In Table I, we have found sensitivities of our target parameter for the circuit in Fig. 4 to each source parameter in its connectivity graph. Sensitivity of a parameter $\alpha$ to a parameter $\beta$ is defined as $S_\beta^\alpha = \frac{d\alpha}{d\beta} \cdot \frac{\beta}{\alpha}$. The meaning of sensitivity is defined as the amount of change in parameter $\alpha$, divided by the amount of change in parameter $\beta$. Observation of the table reveals that the sensitivities of id2, the drain current of the dependent transistor, may have different sensitivities for the same parameter pertaining to each transistor. In previous studies, same sensitivity was assumed to occur for the transistors on which we analyse the mismatch. This has been causing errors as mentioned previously [4].

This table, as well as all other simulation results in this paper are obtained by running HSPICE simulations for a $0.18\mu$ technology. The BSIM3 model is used for transistors. To determine the table entries, relevant parameters are swept, and the target parameter is plotted in terms of the sweep parameter. Other parameters are held at their nominal values. The sensitivity can be measured directly from the output. It is observed that these graphs are highly linear in the region of interest, enabling a small signal approximation. As the swept parameters are independent of each other since they are source parameters in our connectivity graphs, superposition principles apply in calculating the target parameter. This is a very advantageous property of the sensitivity function, which we will further refer to.

Sensitivities of the target parameter to parameters in the dependent and the reference transistor display opposite signs. This implies that, if a process variation causes an increase in the same parameter in both transistors, this will have a compensating effect at the target parameter. Whenever the same parameter in both transistors changes in different directions, the mismatch effect will be at its maximum. These signs can be reasoned from Equation (1) which identifies the condition for matching in a current mirror[2]. As these measurements are performed using BSIM3 parameters by relating a high level parameter to low level independent parameters directly, the results promise to be highly accurate.

The accuracy can be observed in Fig. 5. This figure is a comparison of MCA and the method proposed above. Instead of using a histogram for the MCA results, bin averages are plotted to obtain a smoother graph than a histogram. This is attained by using a normalization over 1. To obtain the result in the fig-

[2]We remind the reader that *PHI* in SPICE corresponds to $2\phi$ in Equation (1).

$$\frac{I_{dep}}{I_{ref}} = \frac{L_{ref} \cdot W_{dep}}{L_{dep} \cdot W_{ref}} \cdot \frac{V_{GSdep} - VT0_{dep} - \gamma_{dep} \cdot (\sqrt{2\phi_{dep} - V_{SBdep}} - \sqrt{2\phi_{dep}})}{V_{GSref} - VT0_{ref} - \gamma_{ref} \cdot (\sqrt{2\phi_{ref} - V_{SBref}} - \sqrt{2\phi_{ref}})} \quad (1)$$

ure, a 300$\mu$A reference current is applied to the circuit through the drain of M0. Transistor lengths are chosen to be the minimum allowed by the technology. The widths are chosen to be 0.54$\mu$m. Sensitivities given in Table I are multiplied with the associated percentage changes in the source parameters separately and added to end up with the percentage change for the target parameter. To determine the source percentage changes, standard deviations assigned to them in the MCA are divided by their means. The result is multiplied by the mean of the target parameter to change the percentage into standard deviation. While plotting the Gaussian curve, the nominal current is used for the mean and the standard deviation is computed using the sum found above. The mean is guaranteed by converting the means of source parameters to percentage changes. The error is analyzed by summing each bin error and found to be on the order of 0.1%. This is obtained by using the results of a 10000 point MCA. If a more accurate MCA is run, this error may even decrease further as MCA will give smoother histograms with more cycles.

## IV. Simulation Results

### A. Application of the Hand-Calculation Method

Having thus obtained an accurate way of finding the pdf of the target parameter, we also need a hand-calculation method for estimating the effects of mismatch on the target parameter. For this estimate, we rely on the connectivity graphs. If we want to write the target parameter in terms of source parameters, then the formula we end up with would be too inordinate to work on. We could not even take its derivative easily. To overcome this problem, we use the sensitivity function. Considering Fig. 3 again, in determining $S_{NSUB}^{VT}$, we can instead use the sensitivities $S_{VT0}^{VT}$ and $S_{PHI}^{VT}$ directly. Here, *VT* and *Vth* are used interchangeably. In order to incorporate the sensitivity information of these intermediate parameters in the connectivity graph to source parameters, we have used the sensitivities $S_{PHI}^{VT0}$, $S_{NSUB}^{PHI}$ and $S_{NSUB}^{VT0}$. $S_{PHI}^{VT0}$ is involved because *VT0* is a function of *PHI*. It may not be apparent from this simple example, but only sensitivities of nodes that have a direct arrow to each node are needed. As a result, $S_{NSUB}^{VT}$ is given by Equation (2). In fact, this result constitutes a very good approximation. It is a better approximation than using correlation coefficients because of the versatility of the sensitivity function. As we can form a connectivity graph for any level SPICE parameter, we can use connectivity graphs and the accompanying methods for any technology.

We have confirmed the applicability of propagating the percentage change in our source parameters using the sensitivity relationships between directly connected nodes in our connectivity graphs towards the target parameter by an example. Assuming the scenario in Fig. 6 for our modelcard, the equations between nodes are given by formulas in Equations (3), (4), and (5). Here, *VT0* is a fitted parameter and we therefore avoid the assignment of a distribution to it. In order to relate *Vth* to *NSUB*, we could substitute Equations (3) and (4) into the equation for *Vth* and end up having a function that does not include these two parameters. As explained above, we can write the relation of sensitivities as in Equation (6) this time. Using these functions, sensitivities are evaluated mathematically. The function that directly gives *Vth* in terms of *NSUB* is also directly used to calculate $S_{NSUB}^{VT}$. The formula pair resulting from using Equation (6) and the direct calculation is identified. Plugging in the variables in these formulas with parameters given or calculated from the BSIM3 modelcard provides results of 0.0504554 and 0.0478611 for evaluation using the connectivity graph and direct evaluation, respectively. The consequent 5.14% error is low in comparison to the error caused by the inaccuracy of the textbook circuit design formulas. We have made it possible to convey the sensitivity of source parameters to high level circuit parameters without having to write the target parameter in terms of source parameters only. We can find formulas for the four sensitivities involved in Equation (6), evaluate them, and use these four values in Equation (6) directly.

$$S_{nsub}^{vt} = S_{phif}^{vt} * S_{nsub}^{phif} + S_{vt0}^{vt} * (S_{phif}^{vt0} * S_{nsub}^{phif} + S_{nsub}^{vt0}) \quad (2)$$

$$phif = \frac{2\,k\,t\,\log(\frac{nsub}{ni})}{q} \quad (3)$$

$$gamma = \frac{\sqrt{2}\,\sqrt{epsi \cdot nsub \cdot q}}{cox} \quad (4)$$

$$vt = gamma\left(-\sqrt{phif} + \sqrt{phif + vsb}\right) + vt0 \quad (5)$$

$$S_{nsub}^{vt} = S_{gamma}^{vt} * S_{nsub}^{gamma} + S_{phi}^{vt} * S_{nsub}^{phi} \quad (6)$$

### B. Application of pdf Propagation Using Simulation Method

In Fig. 7, a differential gain stage is shown when it is used in the first stage of an OpAmp. As seen in the figure, this differential amplifier is biased with a current mirror. It can be easily inferred that the dotted box in Fig. 4 is replaced now with the differential amplifier sub-block. We see that mismatch in the current is given as a pdf input to the dotted area. Identifying the transistor pairs that may have mismatch as *g1* for M1 and M2, *g2* for M3 and M4 and *g3* for M5 and M6, we have run simulations individually activating each mismatch group, then combining them and running simulations again. In doing this, each transistor independently is assigned its version of the SPICE parameters and is assigned independent distributions for its source parameters. Doing this ensures that random effects of mismatch are correctly simulated. An MCA with 10000 cycles is run. To reduce visualization complexity, AC analysis results between 1Mhz and 1GHz are plotted in Fig. 8 for a 100 point MCA with the same conditions preserved. The lines closely spaced in the figure indicate that the distribution has a peak in this region.

In our simulations for the 3.3V differential amplifier, all transistors are chosen to have *L* as 0.18$\mu$m. M1 and M2 have widths of 3.6$\mu$m while the remaining transistors have half of this. *TOX*, *XJ*, *NCH*, *UO*, *W* and *L* are chosen as source parameters. A

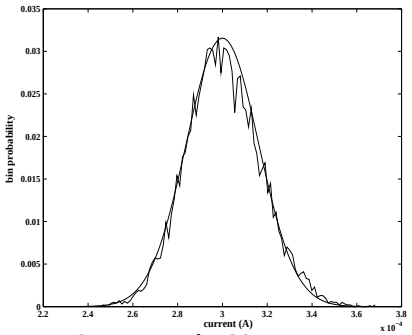


Fig. 5. Comparison of MCA to our estimation method

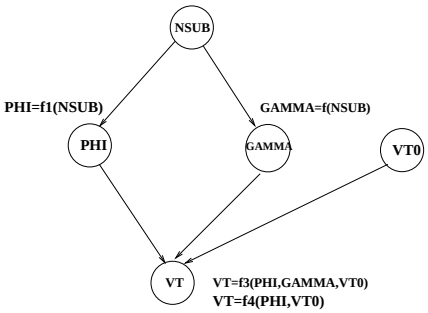


Fig. 6. Target *Vth*, source *NSUB* & *VTO* parameters

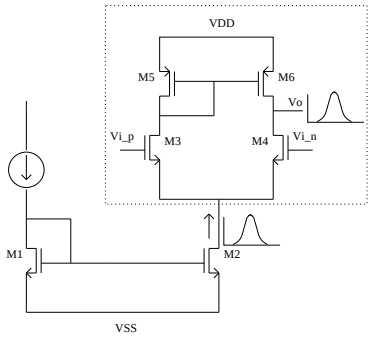


Fig. 7. First Stage of an OpAmp

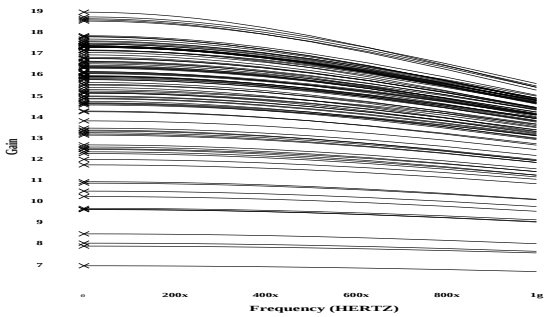


Fig. 8. MCA for AC gain of the differential amplifier, groups *g1*, *g2* and *g3* are all activated - Gain vs. Frequency

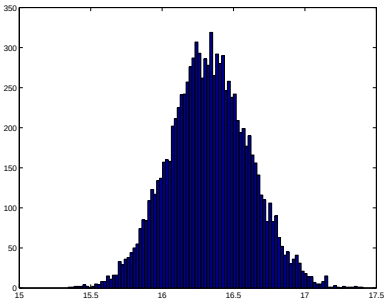

Fig. 9. Histogram for AC gain at 125 Mhz with mismatch in *g1*

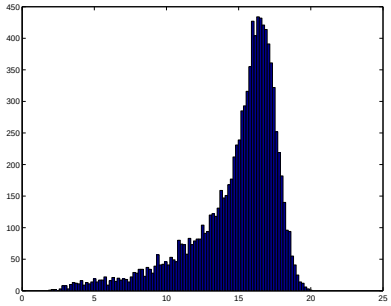

Fig. 10. Histogram for AC gain at 125 Mhz with mismatch in all groups

program that takes MCA outputs and samples them at a single frequency is written. AC response is sampled at 125Mhz. The results are plotted as a histogram which has 100 bins for the 10000 cycle MCA. First, only group *g1* is activated, implying that the differential amplifier module is assumed to have no mismatch in its transistors. The results are shown in Fig. 9. Then, groups *g2* and *g3* are assumed to have mismatch and the corresponding MC AC simulations are performed. A histogram of essentially similar shape as Fig. 10 is attained. Comparing these two simulations, groups *g2* and *g3* are observed to cause a wider spread in the gain; furthermore, the bell-shaped output is no longer present. These distributions, while occasionally making the target parameter safer within its design margins, most of the time have a deteriorating effect. As circuits and circuit subblocks are assigned certain circuit level parameter limits, such as 'gain should exceed 10', or 'bandwidth should exceed 120MHz,' random effects and process variations most of the time make the circuit block drop below these limits. Predicting the distribution of these circuit parameters even before simulation, using hand calculations through connectivity graphs, will decrease analog design time and increase efficiency. In Fig. 10, all groups are assumed to have mismatch. In this case, apparently, *g2* and *g3* together have dominated the shape of the distribution for the gain as opposed to g1, as it is mentioned above that *g2* and *g3* have a similar shaped distribution.

## V. Summary and Conclusion

This paper discusses the random effects involved in mismatch and presents test and simulation techniques. Connectivity graphs and their efficiency for accurate calculations are introduced. A methodology to convey mismatch information at transistor level to high level circuit design parameters is presented. Two approaches, one a hand-calculation method and the other a simulation based method for mismatch prediction of high level circuit parameters, are presented whereby the conventional circuit design approaches are strictly adhered to. A new viewpoint for mismatch is given by treating transistors separately in a group. The idea of conveying mismatch information between circuit blocks as a pdf signal is introduced. Test and measurement techniques are outlined for accurately measuring or simulating the effects of mismatch.

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