Electrostatic Discharge Implantation to Improve Machine-Model ESD Robustness of Stacked NMOS in Mixed-Voltage I/O Interface Circuits

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Abstract

A novel electrostatic discharge (ESD) implantation method is proposed to significantly improve machine-model (MM) ESD robustness of NMOS device in stacked configuration (stacked NMOS). By using this ESD implantation method, the ESD current is discharged far away from the surface channel of NMOS, therefore the stacked NMOS in the mixed-voltage I/O interface can sustain a much higher ESD level, especially under the MM ESD stress. The MM ESD robustness of the stacked NMOS with a device dimension of W/L=300µm/0.5µm for each NMOS has been successfully improved from the original 358V to become 491V in a 0.25-µm CMOS process. This ESD implantation method with the n-type impurity is fully process-compatible to general sub-quarter-micron CMOS processes.

1. Introduction

Component-level ESD stresses on IC products had been classified as three models [1]: the human-body model (HBM) [2]-[4], the machine model (MM) [5]-[6], and the charged device model (CDM) [7]-[8]. The ESD voltage ratio between the HBM and MM ESD robustness of CMOS IC products were around ~10 in the submicron (1.0 ~ 0.5µm) CMOS processes [9]-[10]. Typically, a CMOS IC product, which has a HBM ESD robustness of 2kV, can sustain a MM ESD stress of 200V. However, this ratio has approached to about 15 ~ 20 in the sub-quarter-micron CMOS processes. The CMOS IC fabricated by the sub-quarter-micron CMOS processes can be still designed to have a high HBM robustness, but it becomes more challenging to have a high enough MM ESD level.

In the past, most of ESD design efforts were focused to improve HBM ESD robustness of IC products. With a high HBM ESD robustness, the IC products also had a high enough MM ESD level. However, the MM ESD robustness of IC products has been found to degrade much worse than its HBM ESD robustness in the sub-quarter-micron CMOS processes. How to effectively improve MM ESD robustness of IC products has become a challenge in the sub-quarter-micron CMOS processes. But, from the past literature, it is seldom to see the design or method for improving MM ESD robustness.

In order to enhance ESD robustness, some ESD implantations had been reported for including into process flow to modify the device structures for ESD protection [11]-[13]. The N-type ESD implantation was used to cover the LDD (lightly-doped drain) peak structure and to make a deeper junction in NMOS device for ESD protection [11]. The P-type ESD implantation with a higher concentration located under the drain junction of NMOS was used to reduce the junction breakdown voltage and to earlier turn on the parasitic lateral BJT of the NMOS [12]. Moreover, both of the N-type and P-type ESD implantations were used in NMOS device to wish a higher ESD robustness [13]. The experimental results to compare the effectiveness among those ESD implantation methods had been investigated in a 0.18-µm CMOS process [14].

In the mixed-voltage circuit application, the stacked NMOS structure had been widely used in the mixed-voltage I/O buffer [15], to solve the gate-oxide reliability issue without using the additional thick gate-oxide process (or called as dual gate oxide in some CMOS processes) [16], or even used in the power-rail ESD clamp circuit [17]. Unfortunately, in such mixed-voltage I/O circuits the stacked NMOS often have much lower ESD level, as compared to the buffer with single NMOS [18]-[19]. To improve ESD robustness of the stacked NMOS in the mixed-voltage I/O interface, ESD implantation method is the method without occupied extra silicon area to enhance ESD robustness.

In this paper, a novel ESD implantation method to especially improve machine-model (MM) ESD robustness of stacked NMOS is proposed and verified in a 0.25-µm CMOS processes.

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2. HBM and MM ESD Current Waveforms

The real ESD current discharging waveforms of HBM and MM ESD stresses through the gate-grounded NMOS (ggNMOS) are measured and compared to find the difference. The experimental setup to measure the current waveforms during ESD test is illustrated in Fig. 1, where the digital oscilloscope with current probe is used to measure the ESD transient currents in time domain. The actual ESD current waveforms flowing through the ggNMOS with a device dimension of W/L=300μm/0.5μm under 4-kV HBM and 400-V MM ESD stresses are measured and shown in Fig. 2 and Fig. 3, respectively.

The current peak of 4-kV HBM ESD stress in Fig. 2 is 3.54A, whereas that of 400-V MM ESD stress in Fig. 3 is as high as 4.94A. As comparing these two ESD current waveforms, the MM ESD stress has a much higher ESD current peak within a shorter current pulse width. This implies that the MM ESD events generate more heat in a shorter time period to burn out the device, and therefore cause a much lower ESD robustness. MM ESD protection has become more difficult than HBM in sub-quarter-micron CMOS processes.

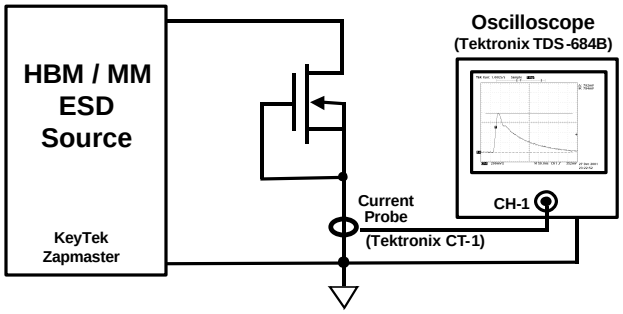

Figure 1. The experimental setup to measure the ESD transient current waveforms during ESD test.

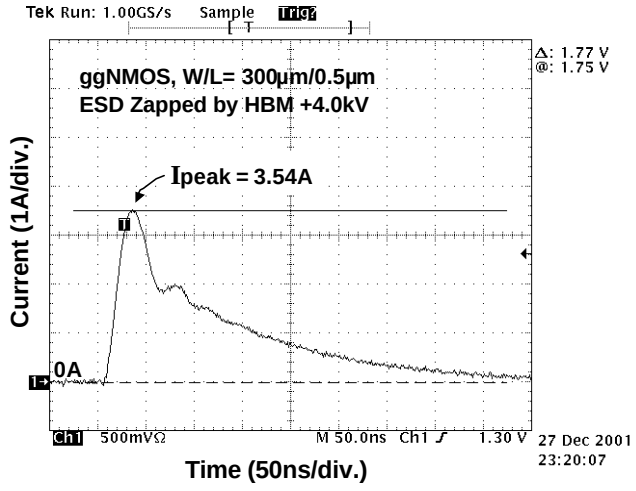

Figure 2. The measured ESD current discharging waveform through the ggNMOS, which is zapped by 4-kV HBM ESD voltage.

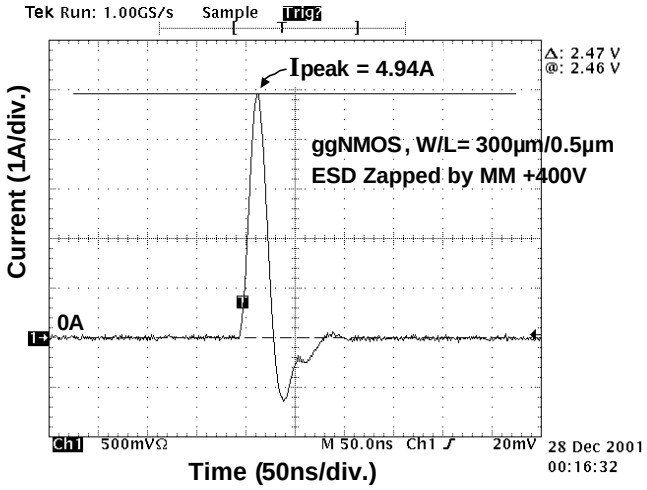

Figure 3. The measured ESD current discharging waveform through the ggNMOS, which is zapped by 400-V MM ESD voltage.

3. ESD Implantation Methods

In submicron CMOS technology, the stacked NMOS in the mixed-voltage I/O interface fabricated with LDD structure to overcome the hot-carrier issue, as shown in Fig. 4, often leads to a lower ESD robustness. To improve ESD robustness, some CMOS processes provide one extra ESD-implantation mask to modify the stacked NMOS in the mixed-voltage I/O interface without the LDD peak structure [14]. One of the traditional ESD implantation methods, with n-type impurity for improving ESD robustness of stacked NMOS, is shown in Fig. 5. The N_ESD impurity in sub-quarter-micron CMOS process often has a lower concentration than that of N+ drain/source diffusion to overcome the hot-carrier issue. A comparison on the effectiveness of improving ESD robustness among the traditional ESD implantation methods had been experimentally investigated in [14].

To significantly improve MM ESD robustness of the stacked NMOS in I/O interface, the novel ESD implantation method is proposed in Fig. 6, where the spacing "S" is the important layout parameter to be investigated. In Fig. 6, the ESD implantation region covers the whole drain region of NMOS device, but except the region around the drain contact. The corresponding layout top view of the stacked NMOS with the proposed ESD implantation method is drawn in Fig. 7, where the layout parameter "S" is also indicated. This ESD implantation region has a doping concentration (N_ESD) lighter than that of the original (N+) drain diffusion. Therefore, the junction covered by the proposed ESD implantation method has an increased junction breakdown voltage. But, the region without covering by this ESD implantation has the original junction breakdown voltage.

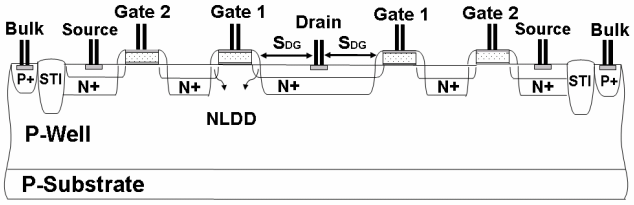

Figure 4. The normal stacked NMOS with lightly-doped-drain (LDD) structure to overcome the hot-carrier issue.

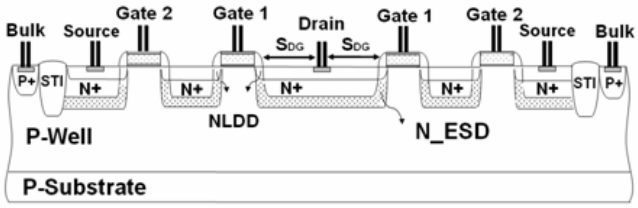

Figure 5. The traditional ESD implantation method with n-type impurity for improving ESD robustness of the stacked NMOS.

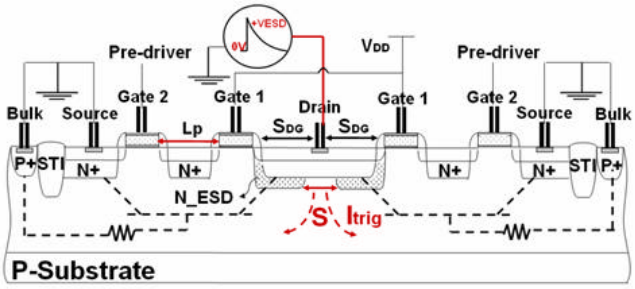

Figure 6. The new proposed ESD implantation method to significantly improve machine-model ESD robustness of the stacked NMOS. The spacing "S" is the important layout parameter to be investigated.

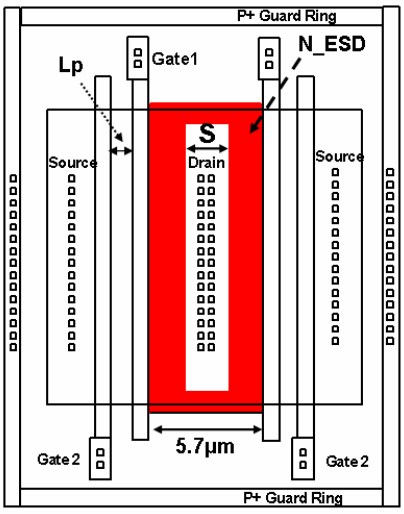

Figure 7. The corresponding layout top view of the stacked NMOS with the new proposed ESD implantation method. The layout parameter "S" is also indicated in this figure.

When a positive ESD voltage is zapped to the pad with the VSS relatively grounded, the drain of stacked NMOS is stressed by the ESD voltage and therefore breaks down to clamp the overstress voltage on the pad. The region, which is not covered by the N_ESD implantation, has a lower junction breakdown voltage. So, the ESD current is first discharged through this region to generate the substrate current (*Itrig*, indicated in Fig. 6) to quickly trigger on the parasitic lateral n-p-n BJT in the stacked NMOS structure. ESD current is mainly discharged through this lateral n-p-n BJT in the stacked NMOS, where such ESD current path is far away from the weakest surface channel of the stacked NMOS. With the self-generated substrate triggering current, the lateral n-p-n BJT in the stacked NMOS structure can be fully turned on more quickly [20]. So, the faster transient current of MM ESD events can be quickly discharged through the lateral n-p-n BJT in the stacked NMOS structure. This causes a significant improvement on ESD robustness of the stacked NMOS in the mixed-voltage I/O interface, especially during the MM ESD zapping.

4. Experimental Results

To investigate the effectiveness of the new proposed ESD implantation method, some test chips drawn with different layout spacing "S" had been fabricated in a 0.25-μm CMOS process with shallow trend isolation (STI). The new proposed N_ESD implantation (shown in Fig. 6) on the test devices is directly realized by using the traditional ESD implantation method with light n-type impurity, which had been an optional process step in general CMOS technologies provided by the most foundries. But, the region to be implanted with the light n-type impurity is drawn in the layout of test devices with different spacing "S". To simplify investigate the dependence of the ESD-implanted region (adjusted by the spacing "S" in layout) on ESD robustness of stacked NMOS structure, the layout spacing of the drain diffusion is fixed at 5.7 μm for all devices in the experimental test chips. The spacing (SDG) from drain contact to poly gate edge is 2.4μm, and the spacing (Lp) between poly gate1 and poly gate2 is 0.4μm. The fabricated devices with different spacing "S" are measured by the curve tracer to investigate DC I-V charactertics, by the transmission line pulsing (TLP) system [21]-[23] to investigate secondary breakdown current (It2), and by the *ZapMaster* ESD simulator to investigate HBM and MM ESD robustness. The experimental results are shown in the following subsections.

4.1. DC I-V Characteristics

The measured DC I-V curves of the stacked NMOS devices with different layout spacing "S" are compared in

Fig. 8. The breakdown voltage (Vt1) of the stacked-NMOS devices with S=0, 2.3, and 3.9μm are almost 9.92V. The holding voltage (Vh) of the stacked-NMOS devices with S=0, 2.3, and 3.9μm is about 5.76V. Therefore, the new proposed N_ESD implantation method does not modify the channel region of the stacked-NMOS devices. When such stacked-NMOS devices are used in the output buffer as the pull-down devices, their I-V curves are similar to that of the normal stacked-NMOS device without ESD implantation in the same CMOS process. This result provides the same device I-V behavior on the N_ESD implanted stacked NMOS as that of normal stacked-NMOS, for working as the functional output devices in CMOS ICs.

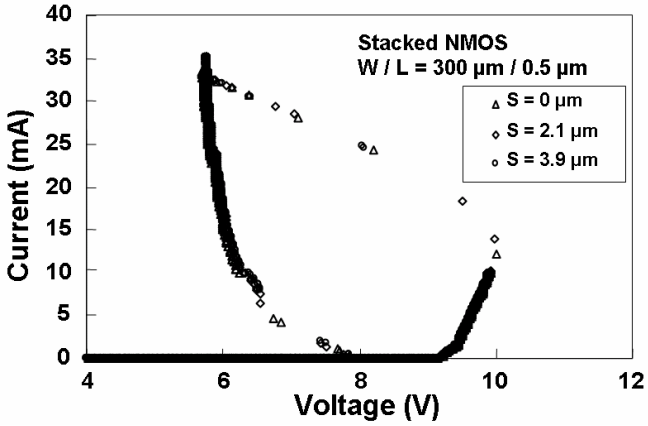

Figure 8. The measured DC I-V curves of stacked NMOS with the new proposed ESD implantation under different layout spacing "S".

4.2. TLP I-V Characteristics

The TLP-measured I-V curves of stacked NMOS with W/L= 300μm/0.5μm, fabricated in a 0.25-μm CMOS process with the new proposed ESD implantation method, are shown in Fig. 9 under the different layout spacing "S". The TLP system used in this measurement has been set up with a pulse width of 100ns and a rise time of 10ns [23]. The dependence of the second breakdown current (It2) on the layout spacing "S" of the stacked NMOS fabricated with the new proposed ESD implantation method is shown in Fig. 10. The It2 of the stacked NMOS with S=0μm is only 3.25A, when it has a device dimension of W/L=300μm/0.5μm. But, its It2 can be significantly improved up to 4.03A, when the spacing S is increased to 3.9μm. Under the same layout area of the stacked NMOS with W/L=300μm/0.5μm, the It2 can be improved 24% by using the new proposed ESD implantation method.

The TLP-measured I-V curves of ESD-implanted stacked NMOS under different channel width but a fixed S=1.5μm are shown in Fig. 11. The It2 of such ESD-implanted stacked NMOS is linearly increased with its channel width from 1.17A (W=100μm) to 6.6A (W=600μm).This implies that the ESD-implanted stacked NMOS with multiple fingers in layout will have good turn-on uniformity during ESD stress.

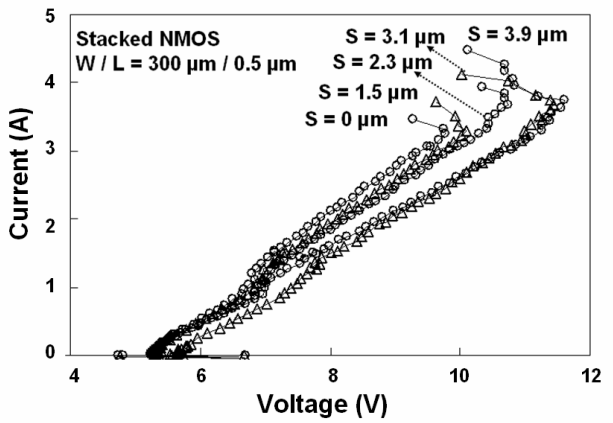

Figure 9. The TLP-measured I-V curves of stacked NMOS with the new proposed ESD implantation under different layout spacing "S".

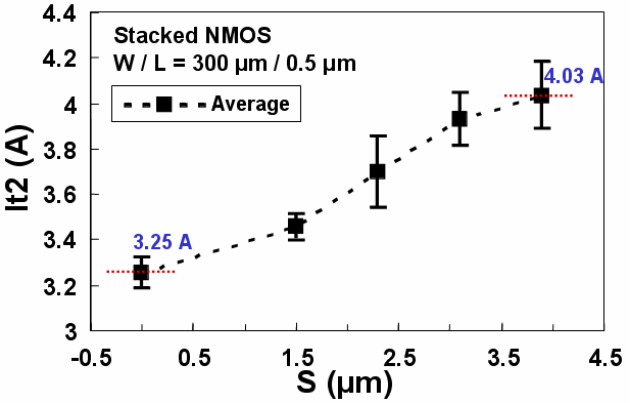

Figure 10. The dependence of the second breakdown current (It2) on the layout spacing "S" of the stacked NMOS fabricated with the new proposed ESD implantation method.

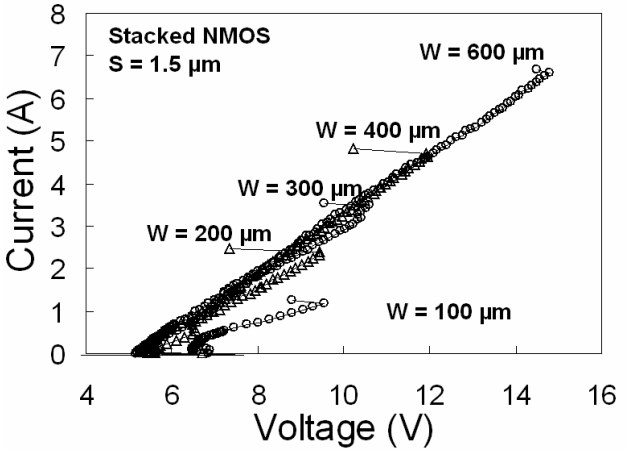

Figure 11. The TLP-measured I-V curves of stacked NMOS with the new proposed ESD implantation under different channel width but a fixed S=1.5μm.

4.3. ESD Test Results

The ESD-implanted stacked NMOS devices are also verified by the ZapMaster ESD simulator under both HBM and MM ESD stresses. The ESD failure threshold (ESD level) is defined at the minimum voltage level of ESD stress that causes the stacked NMOS having a leakage current greater than 1μA under the voltage bias of 3.3V. The dependences of HBM and MM ESD levels on the channel width of stacked NMOS with S= 0 or 1.5 μm are shown in Fig. 12. The HBM and MM ESD levels are linearly increased, when the channel width of stacked NMOS is increased. However, as comparing the lines between the HBM and MM ESD levels under different layout spacing S, the MM ESD level has an obvious improvement if the stacked NMOS is drawn with a wider S.

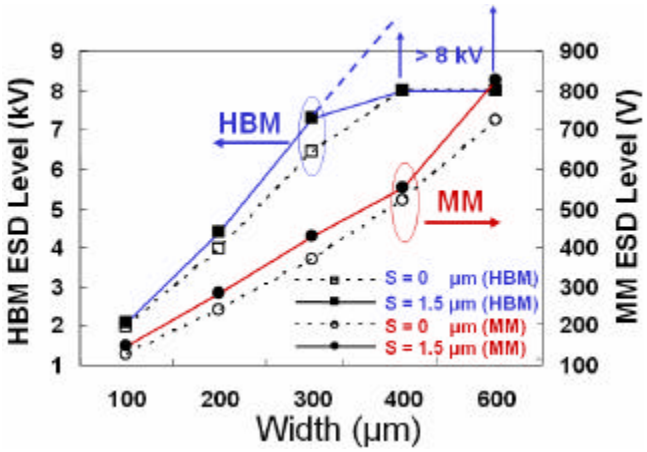

Figure 12. The dependence of HBM and MM ESD robustness on the channel width of ESD-implanted stacked NMOS with S= 0 or 1.5μm.

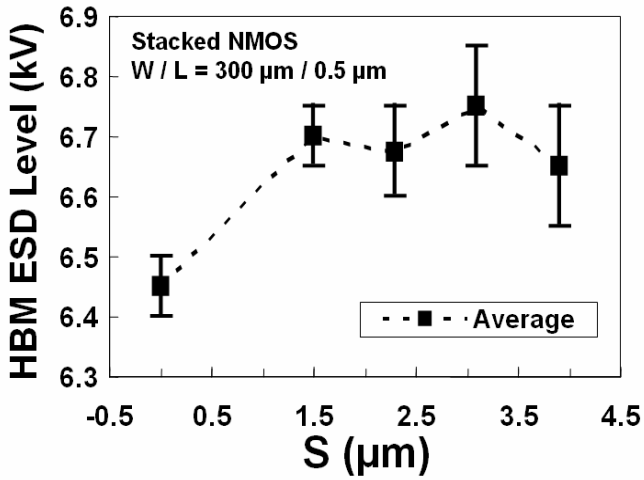

Figure 13. The dependence of the HBM ESD robustness on the layout spacing "S" of the stacked NMOS fabricated with the new proposed ESD implantation method.

The dependences of the HBM and MM ESD robustness on the layout spacing "S" of ESD-implanted stacked NMOS, under a fixed device dimension of W/L=300μm/0.5μm, are shown in Fig. 13 and Fig. 14, respectively. With the same layout area and device dimension in the ESD-implanted stacked NMOS, the wider spacing "S" can lead to higher HBM and MM ESD levels. The HBM ESD level of this ESD-implanted stacked NMOS with a fixed device dimension of W/L=300μm/0.5μm is slightly improved from the original 6.45kV (with S=0) to become 6.65kV (with S=3.9μm). However, the MM ESD level of this ESD-implanted stacked NMOS, with W/L=300μm/0.5μm, is significantly improved from the original 358V (with S=0μm) to become 491V (with S=3.9μm), as that shown in Fig. 14. The MM ESD level can be greatly improved 37% by using the new proposed N_ESD implantation method.

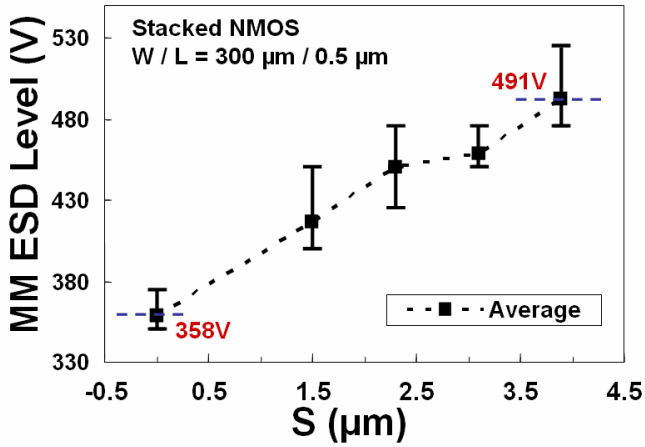

Figure 14. The dependence of the MM ESD robustness on the layout spacing "S" of the stacked NMOS fabricated with the new proposed ESD implantation method.

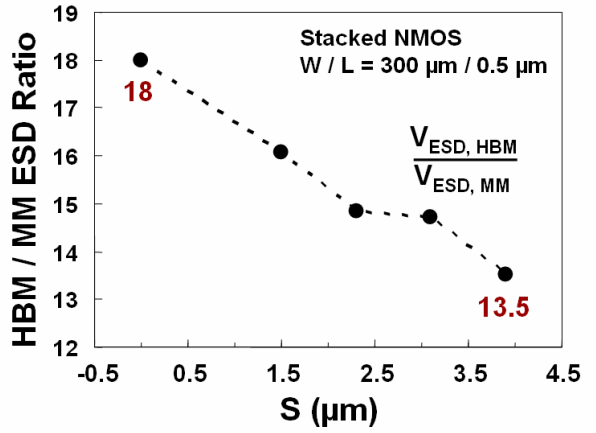

Figure 15. The dependence of the HBM/MM ratio on the layout spacing "S" of the stacked NMOS fabricated with the new proposed ESD implantation method.

The ratio between the HBM and MM ESD levels on the layout spacing "S" of the ESD-implanted stacked NMOS with W/L=300μm/0.5μm are further compared in Fig. 15.

The HBM/MM ESD level ratio of the ESD-implanted stacked NMOS with W/L=300μm/0.5μm has a value of 18 when the spacing S=0μm. As seen in Fig. 15, this HBM/MM ESD level ratio can be decreased to 13.5, when the spacing "S" is enlarged to 3.9μm in the ESD-implanted stacked NMOS. From the experimental results, the new proposed N_ESD implantation method can significantly increase the MM ESD level of stacked NMOS devices in sub-quarter-micron CMOS processes. The HBM/MM ESD level ratio of can be successfully decreased 25% by using the new proposed N_ESD implantation method.

5. Conclusion

A novel ESD implantation method proposed to significantly improve machine-model ESD robustness of stacked NMOS in the mixed-voltage I/O interface has been practically verified in a 0.25-μm CMOS process. From the experimental results, this new ESD implantation method can successfully increase the MM ESD level of stacked NMOS, with a fixed device dimension of W/L=300μm/0.5μm and the same silicon area, from the original 358V to become 491V when the layout spacing S is increased from 0 to 3.9 μm. The HBM/MM ESD level ratio can be successfully reduced 25% by this ESD implantation method. The proposed ESD implantation method, which is process compatible to general CMOS processes with an additional non-critical mask layer of light-doping ESD implantation, is very suitable for using in the IC products to improve their machine-model ESD robustness without adding any extra silicon area.

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