MONOLITHIC DC-DC CONVERTER ANALYSIS AND MOSFET GATE VOLTAGE OPTIMIZATION

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***Abstract* — The design of an efficient monolithic buck converter is presented in this paper. A low swing MOSFET gate drive technique is proposed that improves the efficiency characteristics of a DC-DC converter. A model of the parasitic impedances of a buck converter is developed. With this model, a design space is described which characterizes the integration of both active and passive devices of a buck converter onto the same die based on a 0.18 μm CMOS technology. The optimum gate voltage swing of a power MOSFET that maximizes efficiency is shown to be lower than a standard full voltage swing. An efficiency of 88% at a switching frequency of 102 MHz is achieved for a voltage conversion from 1.8 volts to 0.9 volts with a low swing DC-DC converter. The power dissipation of a low swing DC-DC converter is reduced by 24.5%, improving the efficiency by 3.9% as compared to a full swing DC-DC converter.**

1. INTRODUCTION

Buck converters are popular due to the high efficiency and high quality output voltage regulation characteristics of these circuits. In current microprocessor systems, the primary power supply is typically an external (non-integrated) buck converter which converts a DC voltage supplied by the main power supply to a lower DC voltage (see Fig. 1).

With technology scaling, supply voltages are lowered in order to maintain both the power dissipation and the device electric fields within acceptable limits. Microprocessors, with increased power dissipation and reduced supply voltages, demand greater amounts of current from external power supplies, creating an increasingly significant power generation and distribution problem (both on-chip and off-chip) with each new technology generation [1].

In a typical non-integrated switching DC-DC converter, significant energy is dissipated in the parasitic impedances of the circuit board interconnect and among the discrete components of the regulator [1], [2]. As microprocessor current demands increase, the energy losses of the off-chip power generation and distribution increase, further degrading the efficiency of DC-DC converters. Integrating both the active and passive devices of a buck converter onto the same die as a dual-V_{DD} microprocessor has been proposed in [2] in order to improve efficiency, reduce fabrication costs, and decrease the number of I/O pads dedicated for power delivery on the microprocessor die. A model has been developed and an analysis is presented that describes a design space for full integration of active and passive devices onto the same die as a dual-V_{DD} microprocessor [2].

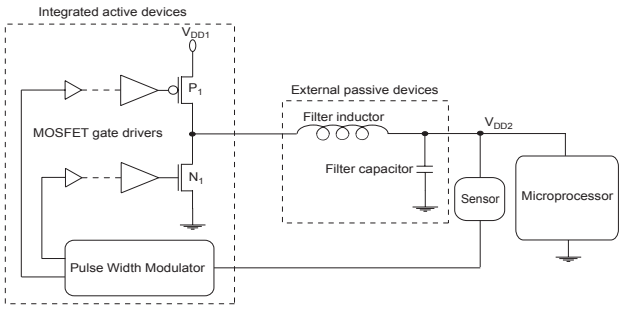

Fig. 1. Buck converter circuit.

The independent variables of the buck converter power expressions proposed in [2] are the switching frequency f_s and the inductor current ripple Δi. The buck converter model proposed in [2] assumes that the PMOS to NMOS width ratio within each MOSFET gate driver is two. Similarly, the tapering factor [3] of the MOSFET gate drivers is assumed to be two, assuming a worst case energy efficiency analysis. The signal swing at all of the internal nodes of the buck converter is assumed to be full rail between ground and V_{DD1}. The model proposed in [2] provides an accurate representation of the parasitic losses of a full voltage swing buck converter (with an error of less than 2.4% as compared to simulation). The model proposed in [2], however, does not provide the flexibility to further optimize the buck converter efficiency by varying the driver tapering factors and gate voltages of the

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power MOSFETs. A more comprehensive parasitic model of a buck converter is, therefore, desirable.

A more general model of a monolithic buck converter is presented in this paper. Closed form expressions that characterize the power consumption of a buck converter are proposed. The gate voltages and tapering factors of the MOSFETs are included as independent parameters in the proposed model. With the proposed buck converter energy model, a design space is presented which characterizes the integration of both active and passive devices onto the same die assuming a 0.18 μm CMOS technology. An efficiency of 84.1% is demonstrated for a voltage conversion from 1.8 volts to 0.9 volts at the target design point for a full swing DC-DC converter. Proposed expressions for estimating the efficiency of a full swing buck converter are within 0.3% of circuit simulation.

A high switching frequency is the key design parameter that enables the full integration of a high efficiency buck converter [2]. At these high switching frequencies, the energy dissipated in the power MOSFETs and gate drivers dominates the total losses of a DC-DC converter. The efficiency can, therefore, be improved by applying MOSFET power reduction techniques. A low swing MOSFET gate drive technique is proposed in this paper that improves the efficiency of a DC-DC converter. It is shown that the power dissipation of a low swing DC-DC converter is reduced by 24.5%, improving the efficiency by 3.9% as compared to a full swing DC-DC converter. Lowering the input and output voltage swing of power MOSFET gate drivers is shown to be effective for enhancing the efficiency characteristics of a DC-DC converter.

The paper is organized as follows. The proposed DC-DC converter circuit model and closed form expressions characterizing the average power dissipation of a buck converter are presented in Section 2. With the proposed model, the efficiency characteristics of a buck converter are analyzed in Section 3. Finally, some conclusions are offered in Section 4.

2. CIRCUIT MODEL OF A BUCK CONVERTER

A circuit model has been developed to analyze the efficiency characteristics of a buck converter. The proposed circuit model for the parasitic impedances of a buck converter is shown in Fig. 2.

The operation of a buck converter circuit behaves in the following manner. The power MOSFETs, labeled as P_1 and N_1 in Fig. 2, produce an AC signal at $Node_1$ by a non-overlapping switching action controlled by a pulse width modulator. The AC signal at $Node_1$ is applied to a second order low pass filter composed of an inductor and a capacitor. Assuming the filter corner frequency is much smaller than the switching frequency f_s of the power MOSFETs, the low pass filter passes to the output the DC component of the AC signal at $Node_1$ and a small amount of high frequency harmonics generated by the switching action of the power MOSFETs.

The buck converter output voltage $V_{DD2}(t)$ is [2]

$$V_{DD2}(t) = V_{DD2} + V_{ripple}(t), \tag{1}$$

where V_{DD2} is the DC component of the output voltage and $V_{ripple}(t)$ is the voltage ripple waveform caused by the non-ideal characteristics of the output filter. The DC component of the output voltage is [2]

$$V_{DD2} = \frac{1}{T_S}\int_0^{T_s} V_S(t)dt = DV_{DD1}, \tag{2}$$

where $V_s(t)$ is the AC signal generated at $Node_1$ and T_s, D, and V_{DD1} are the period, duty cycle, and amplitude, respectively, of $V_s(t)$.

The power transistors are typically large in physical size with a high parasitic capacitance. To control the operation of the power transistors, a series of MOSFET gate drivers are required as shown in Figs. 1 and 2. The driver buffers are tapered as shown in Fig. 2. The gate driver buffers are controlled by a pulse width modulator (PWM). Using a fast feedback circuit, the PWM generates the necessary control signals for the power MOSFETs such that a square wave with an appropriate duty cycle is produced at $Node_1$. During the operation of a buck converter, the duty cycle and/or switching frequency are modified in order to maintain the output voltage at the desired value (output regulation) whenever variations in the load current and voltage demand are detected. Due to the strong dependence of the output voltage on the switching duty cycle [see (2)], precise output voltage regulation can be maintained by a buck converter with a fast feedback circuit [2].

The power consumed by a buck converter is due to a combination of conduction losses caused by the parasitic resistive impedances and switching losses due to the parasitic capacitive impedances of the circuit components. The power consumed by the pulse width modulation feedback circuit and the integrated filter capacitor is typically small as compared to the power consumed by the power train (the power MOSFETs, MOSFET gate drivers, and the filter inductor) [2]. Therefore, only the power dissipation of the power train components is considered in the efficiency analysis.

The MOSFET related power losses are analyzed in Section 2.1. The MOSFET model used during the analysis is discussed in Section 2.2. An analysis of the filter inductor related losses is presented in Section 2.3.

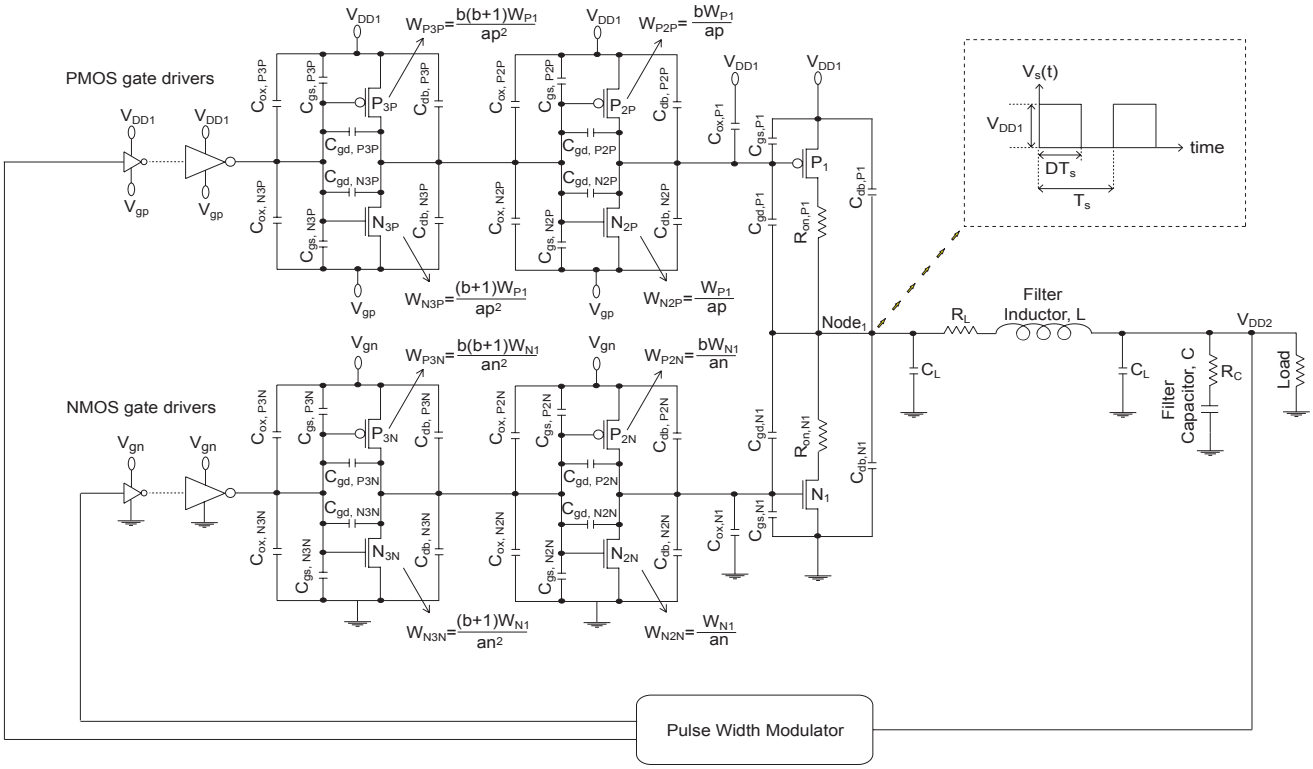

Fig. 2. Parasitic impedances and transistor geometric sizes of a buck converter.

2.1. MOSFET Power Dissipation

The total power loss of a MOSFET is a combination of conduction losses and dynamic switching losses. The conduction power is dissipated in the series resistance of the transistors operating in the active region. The dynamic power is dissipated each switching cycle while charging/discharging the gate oxide, gate-to-source/drain overlap, and drain-to-body junction capacitances of the MOSFETs.

As shown in Fig. 2, the buffers driving P_1 have a ground voltage of V_{gp} where $0 \le V_{gp} < (V_{DD1}+V_{tp})$. The unit energy (per 1 µm wide power MOSFET) dissipated in the drivers of P_1, assuming $ap > (b + 1)$, is

$$E_{PMOSdrivers} \cong \frac{1}{ap-b-1}(bC_{0PMOS}+C_{0NMOS})(V_{DD1}-V_{gp})^2, \quad (3)$$

$$C_{0NMOS} = C_{ox0NMOS} + 2C_{gd0NMOS} + C_{gs0NMOS} + C_{db0NMOS}, \quad (4)$$

$$C_{0PMOS} = C_{ox0PMOS} + 2C_{gd0PMOS} + C_{gs0PMOS} + C_{db0PMOS}, \quad (5)$$

where C_{ox0}, C_{gs0}, C_{gd0}, and C_{db0} are the gate oxide, gate-to-source overlap, gate-to-drain overlap, and the drain-to-body junction capacitances, respectively, of a 1 µm wide transistor, ap is the tapering factor of the buffers driving P_1, and b is the PMOS to NMOS transistor width ratio within each inverter (see Fig. 2).

The voltage swing at the gate of P_1 is between V_{gp} and V_{DD1}. The dynamic energy dissipated during a full switching cycle to charge/discharge the parasitic capacitances of a 1 µm wide P-type power transistor is

$$E_{P1} = [(C_{ox0PMOS}+C_{gs0PMOS})(V_{DD1}-V_{gp})^2 + 2C_{gd0PMOS}(-V_{DD1}V_{gp}+V_{DD1}^2+\frac{V_{gp}^2}{2})+C_{db0PMOS}V_{DD1}^2]. \quad (6)$$

Combining (3), (6), and the conduction power dissipated by the effective series resistance of P_1, the total power dissipation related to P_1 is

$$P_{P1TOTAL} = \frac{R_{0PMOS}}{W_{P1}} i_{rmsPMOS}^2 + W_{P1}E_{P1TOTALswitching}f_s, \quad (7)$$

$$E_{P1TOTALswitching} = E_{P1} + E_{PMOSdrivers}, \quad (8)$$

$$i_{rmsPMOS} = \sqrt{D(I^2+\frac{\Delta i^2}{3})}, \quad (9)$$

where R_{0PMOS} is the effective series resistance of a 1 µm wide PMOS transistor, W_{P1} is the width of P_1, f_s is the switching frequency of the buck converter, D is the duty cycle of the signal generated at $Node_1$ (see Fig. 2), I is the

DC current supplied to the microprocessor, and Δi is the current ripple of the filter inductor.

As shown in Fig. 2, the buffers driving N_1 have a supply voltage of V_{gn} ($V_{tn} < V_{gn} \leq V_{DD1}$). The unit energy (per 1 µm wide power MOSFET) dissipated in these buffers, assuming $an > (b + 1)$, is

$$E_{NMOSdrivers} \cong \frac{1}{an-b-1}(bC_{0PMOS} + C_{0NMOS})V_{gn}^2, \quad (10)$$

where an is the tapering factor of the N_1 gate drivers.

The voltage swing at the gate of N_1 is between ground (0 volts) and V_{gn}. The dynamic energy dissipated during a full switching cycle to charge/discharge the parasitic capacitances of a 1 µm wide N-type power transistor is

$$E_{N1} = [(C_{ox0NMOS} + C_{gs0NMOS} + C_{gd0NMOS})V_{gn}^2 + (C_{gd0NMOS} + C_{db0NMOS})V_{DD1}^2]. \quad (11)$$

Combining (10), (11), and the conduction power dissipated in the effective series resistance of N_1, the total power dissipation related to N_1 is

$$P_{N1TOTAL} = \frac{R_{0NMOS}}{W_{N1}} i_{rmsNMOS}^2 + W_{N1} E_{N1TOTALswitching} f_s, \quad (12)$$

$$E_{N1TOTALswitching} = E_{N1} + E_{NMOSdrivers}, \quad (13)$$

$$i_{rmsNMOS} = \sqrt{(1-D)(I^2 + \frac{\Delta i^2}{3})}, \quad (14)$$

where R_{0NMOS} is the effective series resistance of a 1 µm wide NMOS transistor and W_{N1} is the width of N_1.

As given by (7) and (12), increasing the MOSFET transistor width reduces the conduction losses while increasing the switching losses. An optimum MOSFET width, therefore, exists that minimizes the total MOSFET related power. The optimum transistor widths for N_1 and P_1, respectively, are

$$W_{N1opt} = \sqrt{\frac{R_{0NMOS} i_{rmsNMOS}^2}{f_s E_{N1TOTALswitching}}}, \quad (15)$$

$$W_{P1opt} = \sqrt{\frac{R_{0PMOS} i_{rmsPMOS}^2}{f_s E_{P1TOTALswitching}}}. \quad (16)$$

2.2. MOSFET Model

A low swing MOSFET gate drive technique is investigated in this paper to improve the efficiency of a DC-DC converter. At a reduced gate voltage, the effective series resistance of a MOSFET increases. As has been discussed in Section 2.1., conduction power dissipated in the series resistance of a power MOSFET constitutes a significant portion of the total MOSFET related power consumption in a buck converter (half of the total power dissipation of a power MOSFET with an optimized transistor width). An accurate MOSFET model is, therefore, required to evaluate the effective series resistance of the MOSFETs at each gate voltage within the range of analysis. The MOSFETs are modeled using the n^{th} power law MOSFET model [4]. As shown in Fig. 3, the n^{th} power law MOSFET model captures the dependence of the effective series resistance of the MOSFETs on the gate voltages. The worst case error of the model as compared to the simulation data is less than 10%.

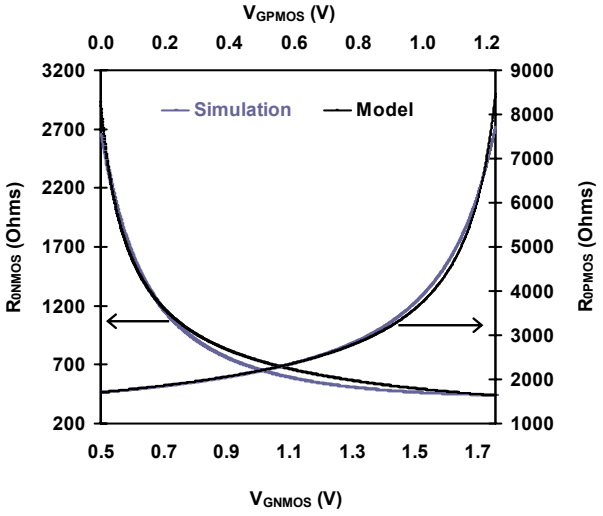

Fig. 3. Variation of the effective series resistance of 1 µm wide NMOS and PMOS transistors with gate voltage, V_G ($|V_{DS}| = 0.1$ volts).

2.3. Filter Inductor Power Dissipation

Some portion of the total energy consumption of a buck converter occurs due to the series resistance and stray capacitance of the filter inductor. As has been shown in [2], the power dissipation in the integrated inductor dominates the total power losses of a buck converter at low switching frequencies.

The integrated filter inductor is a metal slab completely encapsulated by a magnetic material. The magnetic film surrounding the metal is an amorphous CoZrTa alloy that exhibits a good high frequency response, small hysteresis losses, and can be integrated in a standard high temperature CMOS silicon process [5], [6].

In the following analysis it is assumed that the parasitic impedances of an integrated inductor scale linearly with the inductance (within the range of analysis) [6]. The total power dissipated in the filter inductor is

$$P_{inductor} = LR_{L0} i_{rms}^2 + \frac{C_{L0}}{L} V_{DD1}^2 f_s, \quad (17)$$

$$L = \frac{(V_{DD1} - V_{DD2})D}{2\Delta i f_s}, \quad (18)$$

where C_{L0} and R_{L0} are, respectively, the parasitic stray capacitance and parasitic series resistance per nH inductance and L is the filter inductance.

3. BUCK CONVERTER ANALYSIS

The DC-DC converter provides 1.8 volts to 0.9 volts conversion while supplying 250 mA per phase DC current to the load in a 0.18 µm CMOS technology. The tapering factors of the P_1 and N_1 drivers are treated as independent variables and *ap* and *an* are assumed to be equal ($a = an = ap$). PMOS to NMOS width ratio b within each MOSFET gate driver is assumed to be two.

Using the model proposed in Section 2, the maximum efficiency attainable for each tapering factor ($8 \le a \le 24$) is evaluated. The efficiency of a buck converter is

$$\eta = 100 \times \frac{P_{load}}{P_{load} + P_{buck}}, \quad (19)$$

where P_{load} is the average power delivered to the load and P_{buck} is the average total internal power consumption of a buck converter.

The switching frequency is the primary design variable used in the analysis. The efficiency of a buck converter is analyzed over the frequency range, 10 MHz $\le f_s \le$ 1 GHz. At each tapering factor, the maximum attainable efficiency is evaluated over the switching frequency range, varying the circuit configuration. Maximum efficiency circuit configurations determined by the model are simulated verifying the circuit operation and performance characteristics. The maximum efficiency and the total transistor width of the power MOSFETs and gate drivers for each tapering factor are shown in Fig. 4. The tapering factor, switching frequency, and filter inductance of the full swing and low swing circuit configurations with the maximum efficiency characteristics are listed in Table 1.

In the first part of the analysis, V_{gp} and V_{gn} (see Fig. 2) are fixed at 0 volts and 1.8 volts (full swing configuration), respectively. As listed in Table 1, the maximum efficiency attainable with a full swing DC-DC converter is 84.1% based on a tapering factor of 10. The switching frequency of the maximum efficiency configuration is 102 MHz. The analytic estimate of the efficiency for the full swing configuration is within 0.3% of the simulations.

In the full swing maximum efficiency circuit configuration, 62% of the total buck converter power is dissipated in the power MOSFETs (P_1 and N_1) and the MOSFET gate driver buffers while 38% of the total power dissipation occurs in the parasitic impedances of the filter inductor. As most of the buck converter energy is dissipated in the MOSFETs, MOSFET related power reduction techniques can be effective in enhancing the efficiency characteristics of a DC-DC converter.

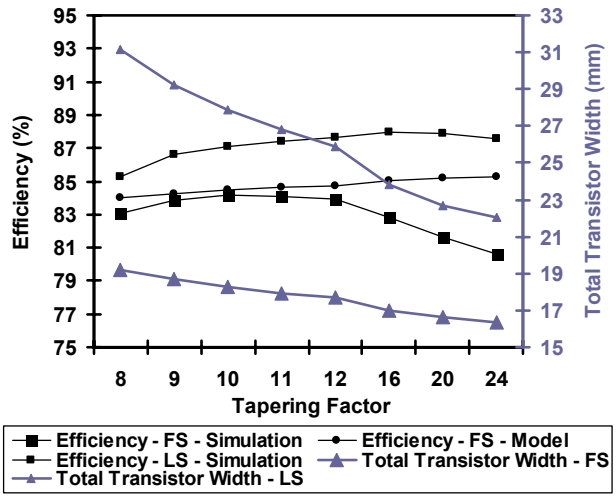

Fig. 4. Total transistor width and simulated maximum efficiency of the full swing (FS) and low swing (LS) circuits for different tapering factors.

TABLE I
EFFICIENCY (η) CHARACTERISTICS OF THE FULL SWING (FS) AND LOW SWING (LS) DC-DC CONVERTER CIRCUITS OBTAINED FROM THE POWER MODEL AND SIMULATION (V_{DD1} = 1.8 VOLTS AND C = 3 NF)

	FS Model	FS Simulation	LS Simulation
V_{gp} (V)	0	0	0.64
V_{gn} (V)	1.8	1.8	1.13
f_s (MHz)	102	102	102
L (nH)	8.8	8.8	8.8
a	10	10	16
Maximum η (%)	84.4	84.1	88.0
Power reduction	N/A	N/A	24.5%
η difference	+0.3%	0	+3.9%

In the second part of the analysis, V_{gp} and V_{gn} are included in the optimization process as independent variables. The effect of reducing the voltage swing of the MOSFET gate driver buffers has been explored. For $0 \le V_{gp} < 1.2$ volts and 0.5 volts $\le V_{gn} \le 1.8$ volts, an optimal choice of gate voltage is performed at each tapering factor a ($8 \le a \le 24$). V_{gp}, V_{gn}, the switching frequency f_s, filter inductance L, and the optimum MOSFET size of the maximum efficiency configurations are determined for each driver tapering factor a. Optimum V_{gp}, V_{gn}, and transistor widths (of P_1 and N_1) that maximize efficiency for each a are shown in Fig. 5. The optimum circuit configurations obtained from the model are simulated to verify operation. As listed in Table 1, the total power dissipation of the low swing buck converter is reduced by 24.5% as

compared to the full swing maximum efficiency configuration by increasing V_{gp} from 0 to 0.64 volts and lowering V_{gn} from 1.8 to 1.13 volts. The maximum efficiency for a low swing DC-DC converter is 88%, 3.9% higher than achieved with a full swing DC-DC converter.

The optimal circuit configurations with the highest efficiency characteristics change as the gate voltages are reduced from the full swing voltage. The effective series resistance of a MOSFET is increased while the total dynamic switching energy is decreased with reduced gate voltage. The optimum MOSFET width that minimizes the power dissipation, therefore, increases with a reduced gate voltage swing [as given by (15) and (16) and as shown in Fig. 5]. As shown in Fig. 4, the total transistor width of the power MOSFETs and gate drivers for the low swing circuit configuration with the highest efficiency is 30% larger as compared to the full swing circuit.

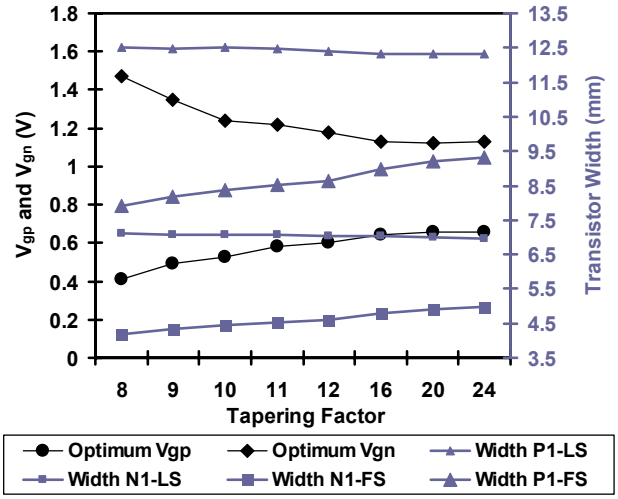

Fig. 5. Optimum V_{gp}, V_{gn}, and width of the power transistors (P_1 and N_1) for the maximum efficiency low swing (LS) configuration for different tapering factors. Optimum power transistor width of the maximum efficiency full swing (FS) DC-DC converter configurations are also shown for comparison.

The proposed model does not include short-circuit currents in the MOSFET drivers. The model, therefore, produces an efficiency that increases monotonically with increasing a, as shown in Fig. 4. With increasing tapering factor, the dynamic switching power is reduced while the short-circuit currents increase [3]. At a certain range of a, the dynamic switching energy losses dominate the total losses. As shown in Fig. 4, the efficiency of a buck converter increases with higher a in the range dominated by switching losses. After the peak efficiency is reached, the increasing short-circuit losses in the power MOSFET gate drivers begin to dominate the total power dissipation of the buck converter. Hence, the efficiency degrades with further increases in a. The optimum tapering factors are 10 and 16 for the full swing and low swing circuits, respectively.

4. CONCLUSIONS

An analysis of the power characteristics of a standard switching DC-DC converter topology, a buck converter, is provided in this paper. Closed form expressions for the total power dissipation of a buck converter are proposed. A range of design parameters is evaluated, permitting the development of a design space for full integration of active and passive devices onto the same die for a target CMOS technology. An efficiency of 84.1% is demonstrated for a voltage conversion from 1.8 volts to 0.9 volts with a full swing monolithic buck converter operating at 102 MHz assuming a 0.18 μm CMOS technology.

The effect of reducing the MOSFET gate voltage swings is explored with the proposed circuit model. The optimum gate voltage swing of a power MOSFET that maximizes efficiency is lower than the standard full swing voltage. It is shown that the power dissipation of a buck converter is reduced by 24.5% as compared to the full swing maximum efficiency configuration by increasing V_{gp} to 0.64 volts and lowering V_{gn} to 1.13 volts. The maximum efficiency achieved with a low swing DC-DC converter is 88%, 3.9% higher than that achieved with a full swing DC-DC converter.

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