Temperature and Process Invariant MOS-based Reference Current Generation Circuits for Sub-1V Operation

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ABSTRACT
Measurements on a prototype chip, implemented in a 150nm logic process technology, validate the theories for two sub-1V MOS reference current generator circuits and show that ~2X reduction in current variation is achievable across extremes of ***both*** process and temperature.

Categories and Subject Descriptors
B.7.0 [**Integrated Circuits**]: General

General Terms
Theory and Measurement.

Keywords
CMOS, reference current, bandgap reference, process and temperature compensation.

1. INTRODUCTION
Designs in low-voltage deep-submicron CMOS technologies require on-chip reference current generators to properly bias various integrated analog circuit components. Scaled-bandgap [1] or MOS-based voltage reference circuits can function with sub-1V supplies. However, they require off-chip precision resistors (one resistor for each bias current generated) and/or on-chip circuitry [7] for voltage-to-current conversion and reference current distribution to different parts of the chip. Off-chip resistors consume I/O pins and increase system cost. Additionally, many of these circuits do not provide sufficient immunity against process variations as they depend on threshold voltage cancellation schemes [2].

Ideally, a current reference generator should be small enough to be instantiated once locally for each analog block. This avoids the IR-drop, noise and/or current mirroring mismatch associated with a chip-wide reference current distribution network. Several sub-1V MOS current reference generators that meet this criterion by avoiding explicit voltage references and off-chip resistors have been reported in the past for providing ***either*** temperature invariance [3-4] ***or*** process compensation [5], but ***not both***.

In this paper, we propose two MOS reference current generator circuits (Fig. 1) to provide immunity against ***both*** temperature and process variations in low-voltage, deep-submicron CMOS technologies. Neither of these techniques requires an off-chip resistor and the reference currents can be generated locally in different parts of the chip. The fixed-voltage (FV) technique uses constant voltage generators derived from scaled-bandgap voltage reference circuits [1]. The scaled-V_{TO} (SV) technique, where V_{TO} is the device threshold voltage at absolute zero temperature, does not require voltage references. Both of these techniques use current-based subtraction. They have been implemented on a prototype chip in a 150nm logic process technology (Fig. 2). Reference current generation theories for both of these schemes are described. The theories are tested and validated using measured device I-V data from the prototype chip.

2. REFERENCE CURRENT GENERATION THEORIES
Long channel devices are used in the reference current generators to provide square-law saturation drain current (I_{DSAT}) characteristics and minimize impact of critical dimension (CD) variations on device parameters. Theory for the FV scheme is illustrated in Fig. 3. Forward body bias is applied to one of the transistors in a matched pair to introduce a "controllable" difference in their threshold voltages (V_T) and effective mobilities (μ_{EFF}). The two devices in the pair, operating in the saturation region, also receive different gate-to-source bias values (V_{GS1} and V_{GS2}) generated by scaled-bandgap voltage references. I_{DSAT} of one of the devices is then scaled by a factor (Z_{RATIO}), and subtracted from that of the other device to produce the reference current (I_{REF}). For a given value of V_{GS2}, V_{GS1} and Z_{RATIO} are solved such that I_{REF} values at opposite corners of temperature (T) and process (P) range are equal, as shown in Fig. 3. This "trimming" of V_{GS1} and Z_{RATIO} values requires I-V (saturated drain current vs. gate voltage) measurements of the matched device pair, one with zero body bias and the other with forward body bias, on two different dies (P_1 & P_2) at two different temperatures (T_1 & T_2).

Fig. 4 describes the theory for the SV technique. Temperature and process compensations are accomplished in two steps. Each device in a matched pair uses a V_{TO}-generator circuit [6] that produces an output voltage $V_{TO} + bT$ with scalable temperature-

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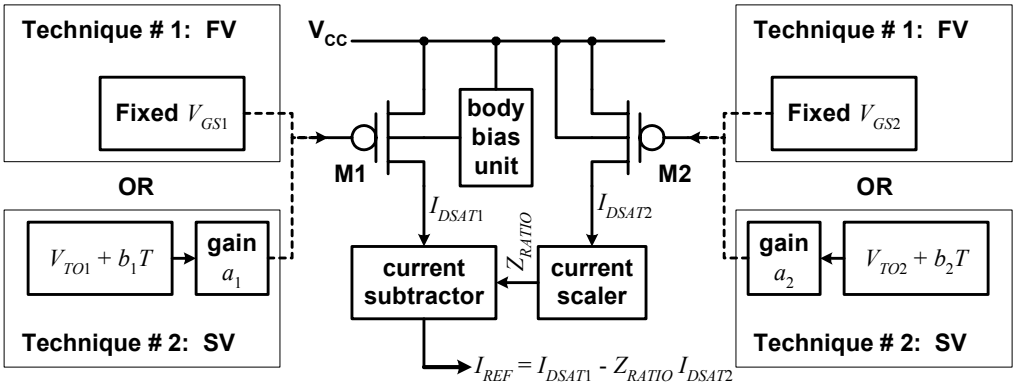


Figure 1 FV and SV techniques for MOS reference current generation.

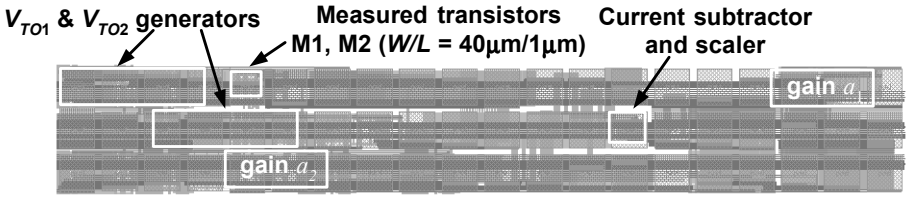


Figure 2 Micrograph of prototype chip.

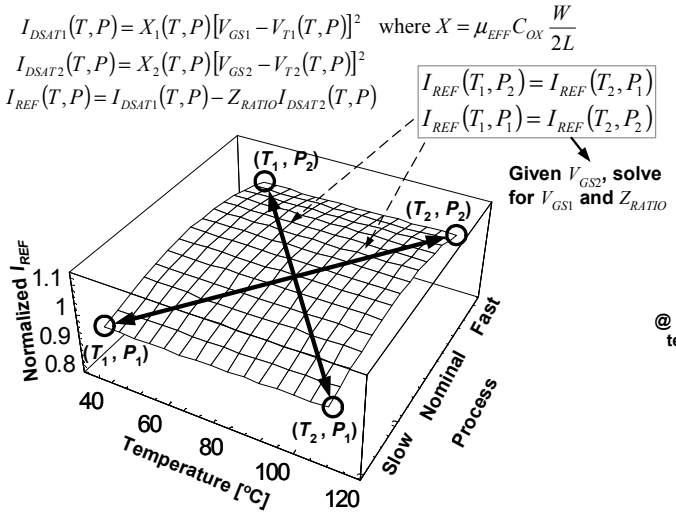


Figure 3 Theory for FV technique.

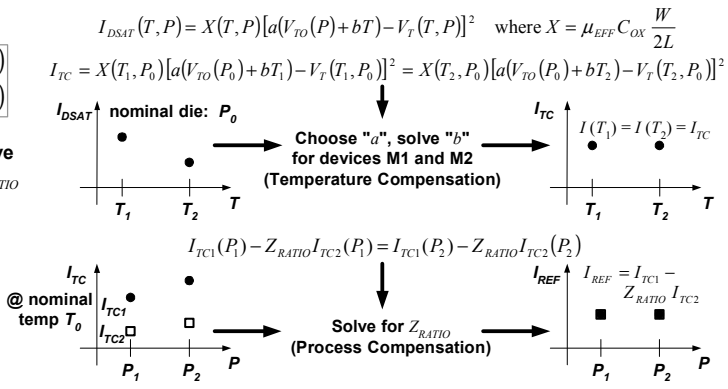


Figure 4 Theory for SV technique.

coefficient b. The output voltage is then scaled by a factor a to generate the gate-to-source bias (V_{GS}) that automatically tracks changes in V_T of the device across process. For a given value of a, the temperature-coefficient b is solved to produce equal I_{DSAT} values at two different temperatures (T_1 & T_2). Both devices in the matched pair have zero body bias, but use different combinations of (a, b) to achieve two temperature-invariant currents. The temperature-compensated current (I_{TC2}) of one of the devices is then scaled by a factor Z_{RATIO} and subtracted from that of the other device (I_{TC1}) to produce the reference current I_{REF}. To achieve process compensation in addition to temperature invariance, we solve for the value of Z_{RATIO} such that I_{REF} values at two different process corners (P_1 & P_2) are equal. This "trimming" of Z_{RATIO} and (b_1, b_2) values for the device pair requires transistor I-V measurements on a nominal die (P_0) at two different temperatures (T_1 & T_2) and on two other dies (P_1 & P_2) at nominal temperature (T_0).

3. MEASUREMENT RESULTS

I_{DSAT} of 40μm/1μm W/L transistors with constant 0.8V V_{GS}, measured on 148 dies across two wafers, show ±11% maximum variation (Fig. 5) across process and temperature (40°C to 110°C). In Fig. 5, the x-axis represents "process" by sorting dies based on their V_T extracted at 80°C from high V_T (slow die) to low V_T (fast die). As expected when gate bias is much larger than V_T, the mobility dominates saturation current and just as mobility decreases with increasing temperature, so does the current.

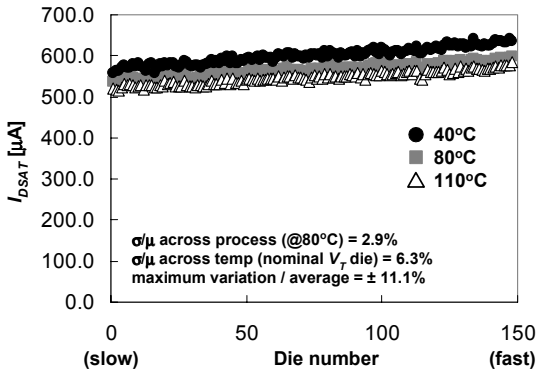


Figure 5 Uncompensated I_{DSAT} data (V_{GS} = 0.8V), with die number sorted in order of decreasing V_T@80°C.

For the FV scheme, 500mV forward body bias is applied to one of the devices in the matched pair. Values of V_{GS1} and Z_{RATIO} are determined from the theory by fixing V_{GS2} (in this case at 0.64V) and solving the two coupled equations in Fig. 3. The V_T and X values to be used are extracted from I-V data measured at 40°C and 110°C on two dies at the extremes of the process range (the dies with the highest and lowest V_T values). Maximum variation of the resulting process- and temperature-compensated reference current is only ±5%, compared to ±11% variation in the uncompensated I_{DSAT} (Fig. 6).

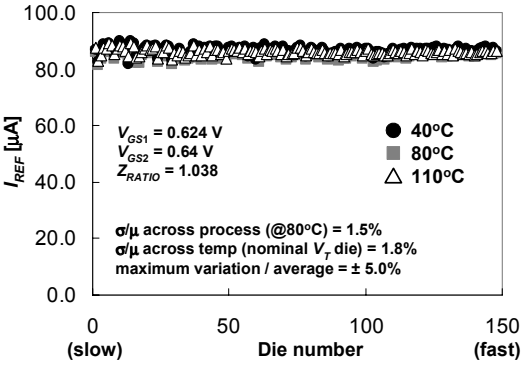


Figure 6 I_{REF} data for FV technique.

In the SV technique, values of b_1 and b_2 for the matched device pair, which are required for temperature compensation, are determined from the theory by choosing values for a_1 and a_2 and solving the quadratic equation for I_{TC} from the top half of Fig. 4. The V_T, V_{TO} and X values to be used are extracted from measured I-V data of devices on a nominal die at 40°C and 110°C. Note that the temperature compensation remains effective for all dies across the process range, even though the "trimming" of b_1 and b_2 values is based on device characteristics of a nominal die. This is most likely due to the fact that the V_{TO}-generator automatically compensates for some process variation and is demonstrated in Fig. 7. For each die, the currents at 40, 80 and 110°C nearly overlap. Because of the near ideal temperature compensation of the SV technique, σ/μ of the resulting I_{TC} is 1% (Fig. 7) across temperature, compared to 6% for the uncompensated I_{DSAT}. To achieve process compensation in the SV technique, the Z_{RATIO} value is determined by solving the equation in the middle of Fig. 4 using the measured I_{TC1} and I_{TC2} from two dies at the extremes of the process range at 80°C. Maximum variation of the resulting process- and temperature-compensated reference current is only ±6% (Fig. 8).

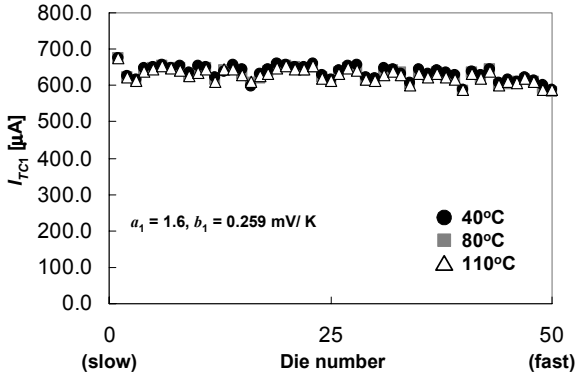


Figure 7 Temperature compensated I_{TC1} data, with the number of dies limited to facilitate viewing.

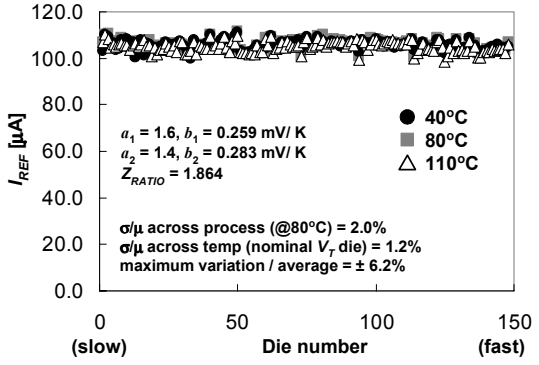


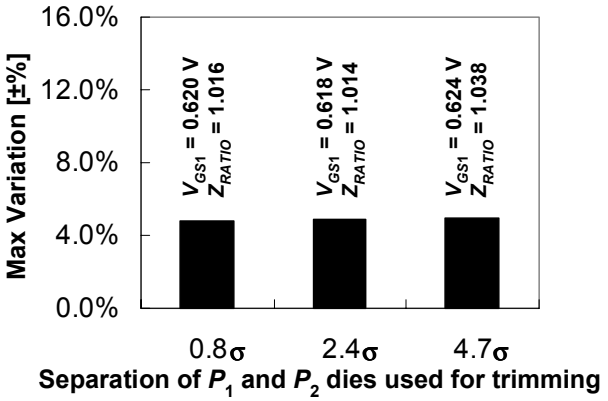
Figure 8 I_{REF} data for SV technique.

4. STATISTICAL ANALYSIS

Both the FV and SV techniques only compensate for linear components of variation across process and temperature. The residual variation is primarily the non-linear component, which can be very sensitive to the choice of dies representing P_1 and P_2. As mentioned in Section 3, a total of 148 dies were measured. The comparisons of the FV and SV techniques to the uncompensated current in Section 3 consider only the best case since they assume that the slowest (P_1, with highest V_T) and fastest (P_2, with lowest V_T) dies in the entire 148-die population are known a priori. Since it is typically impractical to measure the entire population of dies, the dies chosen to represent P_1 and P_2 depend on the available die samples; more samples lead to a wider range and more accurate representation of the process distribution. To simulate the effect a limited number of samples has on the achievable compensation, two arbitrary combinations of P_1 and P_2 were chosen and the spread in V_T of each combination was measured. The resulting I_{REF} variations for the two P_1/P_2 combinations, along with the original best case, are shown in Figs. 9 (for FV) and 10 (for SV). "σ" in the x-axis is the standard deviation of V_T across all 148 dies and is used as the unit for process spread. These figures show little sensitivity of I_{REF} variation to the process spread between P_1 and P_2.

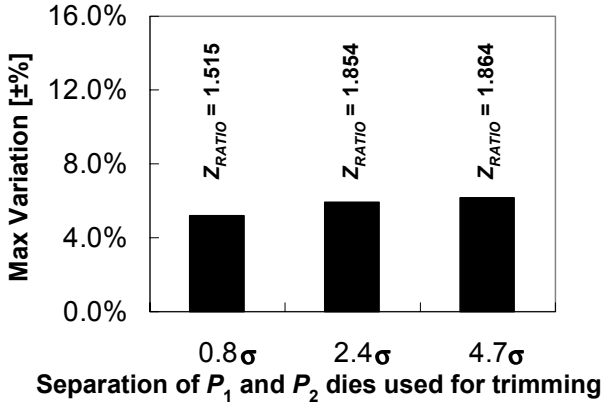
However, Figs. 9 and 10 only show singular examples of P_1/P_2 combinations. 148 dies actually yield 10878 P_1/P_2 combinations. For a statistical study, 5460 of these combinations were chosen. The spread in V_T of each combination was measured and grouped into categories in Table 1. The FV and SV techniques were then applied to the entire 148-die population 5460 times by solving the respective equations for each P_1 and P_2 combination. The resulting distributions of reference current variations for each category are depicted as box-plots in Figs. 11 and 12. Fig. 11 clearly shows that the FV technique continuously lowers I_{REF} variation as the available process spread increases since both the medians and inter-quartile distances reduce. Conversely, there is no trend of improvement for the SV technique as available spread increases. One possible explanation for the difference is that FV performs process and temperature compensation simultaneously, via the coupled equations, whereas SV compensates for temperature and then process in separate steps.

As demonstrated in Figs. 9 and 10, both techniques can succeed if the right P_1 and P_2 combination is chosen fortuitously. In fact, according to the box-plots, there is about a 25% chance that a P_1/P_2 combination will yield less than ±5% variation for both SV and FV (except for categories D, E and F for SV). But statistically, the FV technique is more likely to result in an I_{REF} with low variation. In the SV technique, there is a much higher chance that the resulting I_{REF} could have even larger variation than the uncompensated current (see the top ticks of the box-plots in Fig. 12, which mark the ninetieth percentiles).



P_1 and P_2 separation	σ/μ across process	σ/μ across temperature
0.8σ	1.5%	1.6%
2.4σ	1.5%	1.4%
4.7σ	1.5%	1.8%

Figure 9 Sensitivity of I_{REF} variation in FV scheme to separation between P_1 & P_2 dies used for trimming (V_{GS2} fixed at 0.64V).



P_1 and P_2 separation	σ/μ across process	σ/μ across temperature
0.8σ	2.1%	0.8%
2.4σ	2.0%	1.2%
4.7σ	2.0%	1.2%

Figure 10 Sensitivity of I_{REF} variation in SV scheme to separation between P_1 & P_2 dies used for trimming (a_1, b_1, a_2, b_2 fixed at 1.6, 0.259mV/K, 1.4 and 0.283mV/K, respectively).

Table 1 Breakdown of the 5460 P_1/P_2 die combinations based on spread of V_T in each case.

Category	# of combos	V_T spread of P_1, P_2
A	427	$\Delta V_T < 1\sigma$
B	1764	$1\sigma < \Delta V_T < 1.5\sigma$
C	1527	$1.5\sigma < \Delta V_T < 2\sigma$
D	845	$2\sigma < \Delta V_T < 2.5\sigma$
E	599	$2.5\sigma < \Delta V_T < 3\sigma$
F	298	$\Delta V_T > 3\sigma$

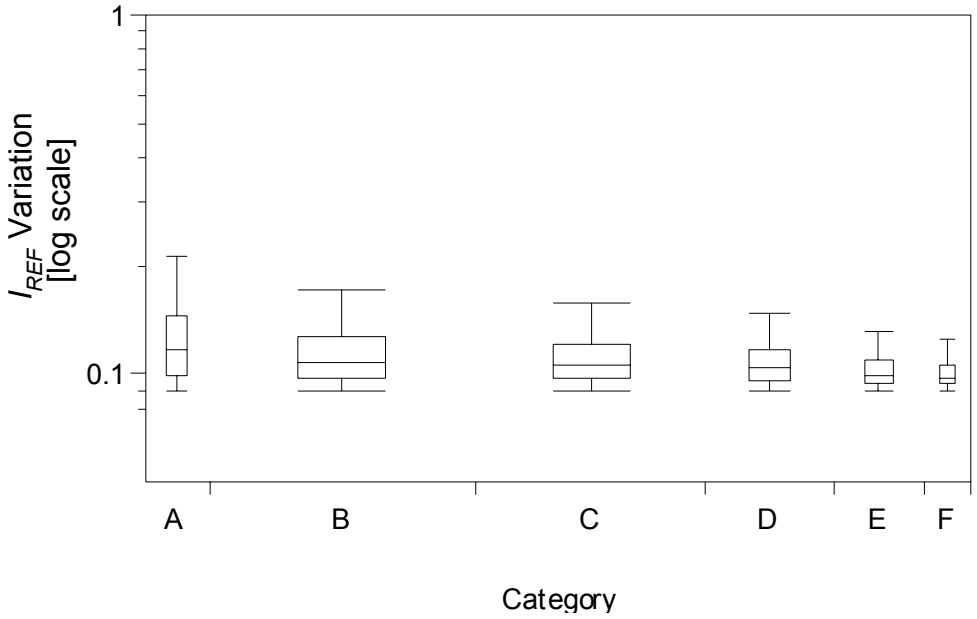


Figure 11 Box-plots of I_{REF} variation for FV technique. See Table 1 for category definition. Width of each box-plot represents number of P_1/P_2 combinations. Variation calculated as (max-min)/average. Multiply y-axis by 100 and divide by 2 to obtain +/-%.

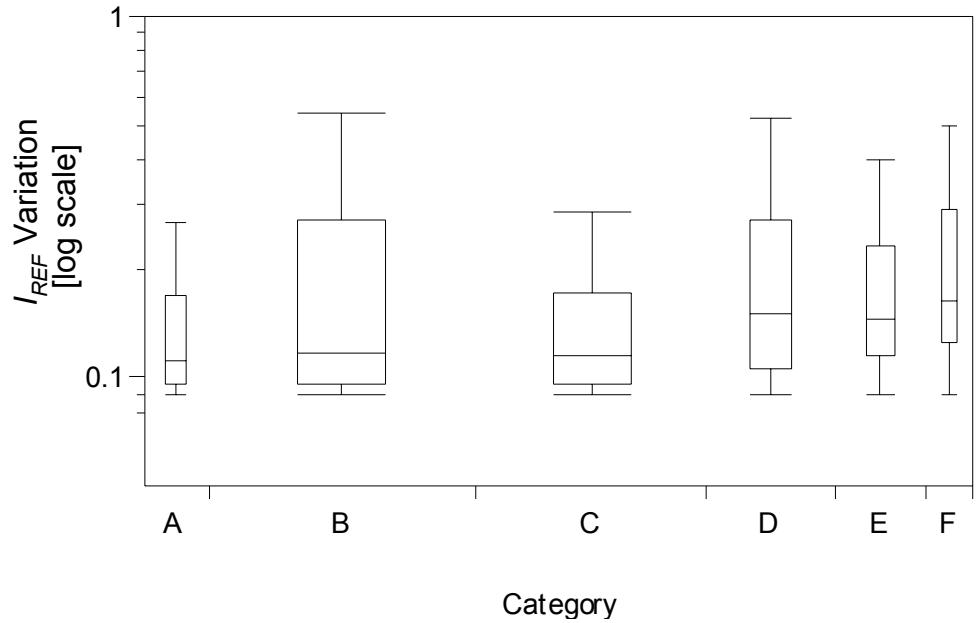


Figure 12 Box-plots of I_{REF} variation for SV technique. See the caption of Fig. 11 for more details on the box plots.

5. CONCLUSIONS

The fixed-voltage (FV) and scaled-V_{TO} (SV) techniques, two sub-1V MOS-based reference current generators, were proposed to provide immunity against ***both*** temperature and process variations. Measurements on a prototype chip, implemented in a 150nm logic process technology, were used to validate the reference current generation theories and show that ~2X reduction in current variation is achievable across extremes of process and temperature. Process compensation was statistically shown to be more robust for FV than for SV.

6. REFERENCES

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