Branch Merge Reduction of RLCM Networks

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***Abstract*—In this paper we consider the problem of finding a smaller RLCM circuit that approximately replicates the behavior (up to a certain frequency) of a given RLCM circuit. Targeted at parasitic extractors for verification of VLSI designs, the proposed algorithm uses a branch merge, node elimination methodology, with the choice of nodes for elimination being guided by time-constant criteria. Reliable, accurate, easy to code, the algorithm works well for coupled buses and clocks, strongly inductive networks, and low-loss transmission lines, as well as for lossy RLC networks.**

***Index Terms*—Parasitic extraction, model order reduction, Gaussian elimination, transmission-line modeling.**

I. Introduction

As circuits get larger, verifying the correctness of a design becomes more difficult. Final timing verification is normally performed using extracted parasitics, and the ability to produce compact interconnect models is important if verification of VLSI designs is to be reasonably efficient.

Model order reduction of RC and RCLM networks has been a vigorous area of research during the last decade. Moment matching, popularized by AWE, has been a dominant theme[1]; PVL and the Arnoldi methods improve numerical conditioning [2][3]; congruence transformations solve stability problems [4]; the culmination in this evolution is Krylov subspace projection methods like PRIMA [5].

But a quit different approach to reduction has also threaded the literature. This approach produces an abridged circuit in the form of a realizable, RLCM network, usually as the result of local circuit transformations by which some nodes or branches are eliminated while others are introduced or modified. If projection methods are the reduction counterpart to the conjugate gradient method, then this alternate approach of **realizable reducers** is the analog of Gaussian elimination. An early instance is [6] , where the ideas of *elimination of nodes* and *capacitance redistribution* are introduced; another early reference is [7]. To control accuracy, Elias and van der Meijs in [8] pioneered the strategy of *selective node elimination*. In TICER [9], Sheehan advocated the criterion of *nodal time constants* and demonstrated that Gaussian elimination of a node and capacitance redistribution produce little error provided the time constant of the node is small compared to the rise and fall times of the circuit.

Realizable reducers have definite advantages. They are highly efficient. Relying as they do on strictly local circuit transformations, they can operate 'on the fly' during scan-line extraction of parasitics. They can handle circuits with many ports—a trouble spot for projection methods, whose subspace size grows with port count. But perhaps realizable reducers' biggest advantage is that they produce engineer-friendly circuit descriptions as output; projection methods, by contrast, manufacture matrices, perhaps poles and residues, but not resistors, capacitors, and inductors. Realizable reducers are the natural choice for extraction tools that must generate SPICE or SPEF files of RLCM components.

The problem of extraction of inductance has recently received a lot of attention, and projection methods formulated in terms of susceptance have been proposed [10][11]. Recently, proposals have also been made for realizable reducers that handle circuits with inductance [12][13]. Following in this vein, the present paper develops a realizable reducer algorithm for RLCM networks by extending the ideas of nodal time constant and node elimination to networks with inductance. Rather than treating the problem in its fullest generality, we restrict topology to an important special case; by compensation, we delve more deeply into the question of validity.

Underlying our approach is the recognition that the amount of reduction that can be imposed on an RLCM network depends on the intended operating range of frequencies. For digital circuits, an approximate operating frequency is

$$f^{\max} \approx 1/4t_r^{\min} \tag{1.1}$$

where $t_r^{\min}$ is the *fastest* rise/fall time in the system.

II. Branch Merging

A. The Neighborhood of a Node

Consider the circuit in Fig. 1. This circuit is to be regarded as part of a much larger network; path 1-N-2 might be three successive nodes of a clock or bus path, for example. We take the perspective of node N, and only show those elements that couple to it. The circuit of Fig. 1 might

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be called the **neighborhood** of node N.

The neighborhood of a node has the following elements (see Fig. 1). First, nodes 1 and 2 are dc connected to N through impedances Z_1 and Z_2, which we assume have the form

$$Z_1 = R_1 + sL_1 \qquad Z_2 = R_2 + sL_2 \tag{2.1}$$

i.e., each consists of a resistor and inductor in series; we call such branches incident **RL branches**. Second, nodes like V_n, V_p, …, V_m capacitively couple to N through capacitors C_{nN}, C_{pN}, …, C_{mN}; we call these capacitors **C branches**. Finally, there may be branches—such as those carrying currents I_q and I_r in Fig. 1—that couple magnetically, through mutual inductances, to Z_1 and Z_2; these we call **M branches**.

Since our purpose is practical, we restrict ourselves in this paper to a simple but important case. *We consider only those nodes that have exactly two incident RL branches*, like N in Fig. 1. The reason for this restriction is several-fold. First, as this configuration is by far the most common, consideration of the errors incurred in this endemic case is merited. Second, eliminating nodes with more than 3 incident RL branches can increase circuit size, contrary to our goal, rather than reduce it, because when a node is eliminated, a complete clique of branches must be introduced between its former neighbors (see [9]). Finally, eliminating nodes with incident RL degrees of 1 or 3 and higher removes key topological features—leaves and junctions—from the circuit. Since a side benefit of this type of reduction is that it can preserve overall topology, it is sensible not to touch leaf and junction nodes.

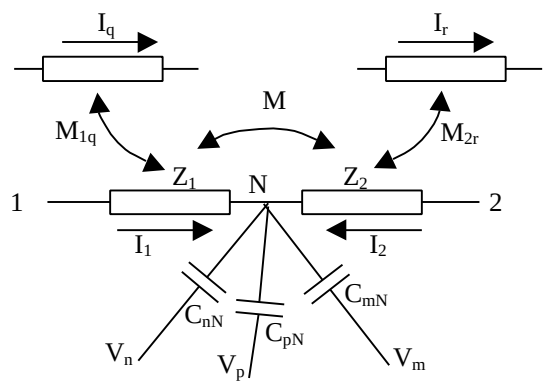

Fig. 1. Neighborhood of Node N

Other than this restriction, the neighborhood of N is arbitrary. N can have any number of C and M branches, so buses with magnetic and capacitive coupling are within the scope of our algorithm. In general, we assume Z_1 and Z_2 can couple magnetically to each other (see M in Fig. 1).

B. Branch Merge Operation

Our algorithm for reducing RLCM circuits consists in repeated application of an 'atomic' operation called a **branch merge**, which: (1) combines impedances Z_1 and Z_2 in series, due account being taken of any mutual M coupling them; (2) changes the sign of mutuals (e.g. $-M_{2r}$) as necessary in accordance with assumed current directions; and (3) reattaches capacitors that had gone to N, a portion going to node 1 and a portion to node 2. Branch merge converts the circuit of Fig. 1 into the circuit of Fig. 2.

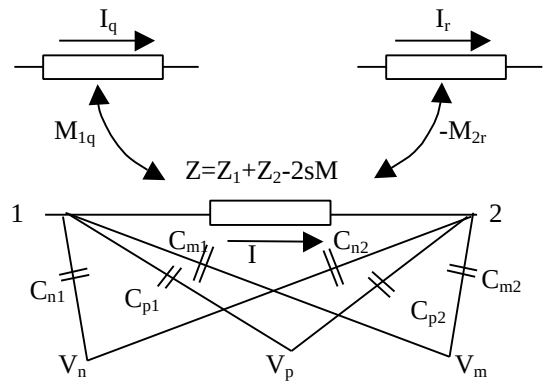

Fig. 2. Same circuit after Branch Merge

In this section, we derive heuristically the branch merge equations; in the next section, we set forth criteria for when branch merge can be applied such that the circuits before and after modification behave nearly the same up to some specified frequency.

C. Branch Impedance

The formula for Z, the impedance of the merged branch, is a direct consequence of the approximation,

$$I_1 \approx -I_2 , \tag{2.2}$$

which follows from the assumption that *the capacitive current at node N (the current flowing to or from N through incident C branches) is small compared to the currents I_1 and I_2 flowing through the incident RL branches.* We will justify this assumption later.

We substitute the branch relations

$$V_{1N} = (R_1 + sL_1)I_1 + sMI_2 + \sum_q sM_{1q}I_q \qquad V_{2N} = sMI_1 + (R_2 + sL_2)I_2 + \sum_r sM_{2r}I_r \tag{2.3}$$

into

$$V_{12} = V_{1N} - V_{2N} . \tag{2.4}$$

and then replace I_1 by I and I_2 by $-I$; the result is

$$V_{12} = ZI + \sum_q sM_{1q}I_q + \sum_r (-sM_{2r})I_r , \tag{2.5}$$

where

$$Z = (R_1 + sL_1) + (R_2 + sL_2) - 2sM \tag{2.6}$$

is the branch impedance and I the branch current (Fig. 2).

Equation (2.5) implies that any M branches coupled to Z_1 or Z_2 before the merge couple to Z after the merge, the sign being changed if the old and new current directions differ. When I_1 and I_2 magnetically couple to the same branch, the corresponding terms in $\sum_q M_{1q}I_q$ and $\sum_r (-M_{2r})I_r$ combine.

D. Capacitance Splitting Operation

In deciding how to handle capacitors, our guiding principle is the requirement that, as far as possible, *the net charge stored by C-branch capacitors before and after branch merge should be the same*.

To see how this principle works out, consider a typical capacitor C_{pN} connecting node p to node N (Fig. 1). Before transformation, the charge on this capacitor will be

$$Q = C_{pN}(V_N - V_p)\,. \tag{2.7}$$

If the circuit is operating at sufficiently low frequencies, *the emf's in branches 1 and 2 due to mutual inductances will be small compared to the voltage drops across the resistors*; in this case,

$$V_N \approx \frac{R_2V_1 + R_1V_2}{R_1 + R_2}\,. \tag{2.8}$$

Placing this expression into (2.7), we get

$$Q = C_{pN}\left(\frac{R_2V_1 + R_1V_2}{R_1 + R_2} - \frac{R_1 + R_2}{R_1 + R_2}V_p\right)$$

$$= \frac{C_{pN}R_2}{R_1 + R_2}(V_1 - V_p) + \frac{C_{pN}R_1}{R_1 + R_2}(V_2 - V_p) \tag{2.9}$$

for the charge on C_{pN} before the merge. Capacitors C_{1p} and C_{2p} in Fig. 2 will store the same charge provided

$$C_{p1} = \frac{C_{pN}R_2}{R_1 + R_2}, \quad C_{p2} = \frac{C_{pN}R_1}{R_1 + R_2} \tag{2.10}$$

This is our formula for capacitance splitting; its legitimacy rests on (2.8). An immediate consequence of (2.10) is

$$C_{p1} + C_{p2} = C_{pN}\,, \tag{2.11}$$

i.e., total capacitance is preserved during a capacitor splitting operation. Another consequence is that the operation preserves Elmore delay. Together, equations (2.5), (2.6), and (2.10) define the branch merge operation.

III. LEGITIMACY CRITERIA

We now shift to a more critical mindset and seek criteria for when the branch merge can be applied with little error.

Definition. The predicate LEGITIMATE(N, $f^{\max}$) is true if and only if the neighborhood circuit before and after a branch-merge at node N has nearly the same currents at neighbor nodes 1 and 2, all other conditions being equal.[1]

A number of legitimacy criteria are possible.

Theorem 1. LEGITIMATE(N, $f^{\max}$)=true if the following conditions all hold up to $s = 2\pi j f^{\max}$:

$$(i)\quad \left|\hat{Z}_1 Y\right| << 1 \quad or \quad \left|\hat{Z}_2 Y\right| << 1$$

$$(ii)\quad \left|YsM\right| << 1$$

$$(iii)\quad \frac{\hat{Z}_1}{\hat{Z}_1 + \hat{Z}_2} \approx \frac{R_1}{R_1 + R_2} \quad and \quad \frac{\hat{Z}_2}{\hat{Z}_1 + \hat{Z}_2} \approx \frac{R_2}{R_1 + R_2} \tag{3.1}$$

where

$$\hat{Z}_1 \equiv R_1 + s(L_1 - M), \quad \hat{Z}_2 \equiv R_2 + s(L_2 - M) \tag{3.2}$$

and

$$Y = sC, \quad C = \sum_p C_{pN} \tag{3.3}$$

Proof: See Appendix.

Two derivative criteria, perhaps more useful in practice, can be stated in terms of the quantities:

$$t_{RC} = \min\{R_1, R_2\}C$$

$$t_{LC}^2 = \begin{cases} (L_1 - M)C & \text{if } R_1 < R_2 \\ (L_2 - M)C & \text{if } R_2 < R_1 \end{cases}$$

$$t_M^2 = MC$$

$$t_{RL} = \max\left\{\frac{L_1 - M}{R_1}, \frac{L_2 - M}{R_2}, \frac{M}{\min\{R_1, R_2\}}\right\} \tag{3.4}$$

Corollary 1. LEGITIMATE(N, $f^{\max}$)=true if all the following conditions hold up to $s = 2\pi j f^{\max}$:

$$(i)\quad \left|t_{RC}s\right| << 1$$

$$(ii)\quad \left|t_{LC}^2 s^2\right| << 1$$

$$(iii)\quad \left|t_M^2 s^2\right| << 1$$

$$(iv)\quad \frac{R_1}{R_1 + R_2} \approx \frac{L_1 - M}{L_1 + L_2 - 2M} \tag{3.5}$$

Proof. We show (3.5) implies (3.1). For definiteness, suppose $R_1 = \min\{R_1, R_2\}$. Then

$$\left|\hat{Z}_1 Y\right| = \left|(R_1 + s(L_1 - M))sC\right| \le \left|t_{RC}s\right| + \left|t_{LC}^2 s^2\right| << 1$$

$$\left|YsM\right| = \left|s^2 MC\right| \le \left|s^2 t_M^2\right| << 1$$

Also, (iv) of (3.5) clearly implies (iii) of (3.1).

Corollary 2. LEGITIMATE(N, $f^{\max}$)=true if both of the following conditions hold up to $s = 2\pi j f^{\max}$:

$$(i)\quad \left|t_{RC}s\right| << 1$$

$$(ii)\quad \left|t_{RL}s\right| << 1. \tag{3.6}$$

Proof. Again, we show (3.6) implies (3.1). Supposing $R_1 = \min\{R_1, R_2\}$, we have

$$\left|\hat{Z}_1 Y\right| = \left|R_1 Cs(1 + s(L_1 - M)/R_1)\right| \le \left|t_{RC}s\right|(1 + \left|t_{RL}s\right|) << 1$$

$$\left|YsM\right| = \left|s^2 CM\right| = \left|(sR_1C)(sM/R_1)\right| \le \left|st_{RC}\right|\left|st_{RL}\right| << 1$$

$$\frac{\hat{Z}_i}{\hat{Z}_1 + \hat{Z}_2} = \frac{R_i(1 + e_i)}{R_1(1 + e_1) + R_2(1 + e_2)} \approx \frac{R_i}{R_1 + R_2}$$

where $e_i = s(L_i - M)/R_i$, $\left|e_i\right| \le \left|st_{RL}\right| << 1$, $i = 1,2$.

The criteria of Corollary 1 and Corollary 2 are both useful in practice, but refer to different situations. Corollary 1 is useful for discretized lines or buses having uniform

[1] 'All other conditions being equal' means V_1, V_2, voltages at the other end of C branches, and currents in M branches, are taken to be the same when making the comparison.

electrical parameters per unit length; the lines can be low loss with inductance predominating over resistance. Corollary 2, on the other hand, does not require uniformity but requires—condition (3.6)(ii)—that resistive drops be more significant than inductive. Note that t_{RC} and t_{LC} scale with the granularity of the extraction; smaller R's, C's, and L's result in smaller t_{RC}'s and t_{LC}'s. Contrarily, t_{RL} is an intrinsic property of the interconnect technology, independent of how finely the circuit is minced during extraction. To get a feel for the magnitude of t_{RL}, consider a VLSI interconnect with $r = 220\Omega/mm,\ Z_0 = 50\Omega,\ t_{pd} = 11ps/mm$ (see [14]):

$$t_{RL} = \frac{l}{r} = \frac{1}{r}\sqrt{\frac{l}{c}}\sqrt{lc} = \frac{Z_0}{r}t_{pd} = \frac{50}{220}11ps = 2.5ps \qquad (3.7)$$

and the condition $t_{RL}s << 1$ becomes—using (1.1)—$\frac{2p}{4}t_{RL} \approx 4ps << t_r^{\min}$. As minimum edge rates are usually much slower than 4ps, (3.6)(ii) is likely to hold in practice.

IV. BRANCH-MERGE ALGORITHM

A simple but effective algorithm based on branch merge is summarized in listing 1. The algorithm makes several passes over the circuit following a schedule of maximum frequencies. On a given pass, each node in the circuit is visited. If the node has more or fewer than *two* incident RL branches, the algorithm skips to the next node; otherwise, it checks if a branch merge can be legitimately done based on the current max frequency; if so, it modifies the circuit as in section II by doing a branch-merge.

```
Algorithm: BMReducer(f^max)
For Pass=1 to NumPasses
{
      f^pass=Multiplier[Pass]* f^max;
      For each node N in circuit
      {
            If RL_Deg(N)!= 2
                  Continue;
            if LEGITIMATE(N, f^pass)
                  BranchMerge(N);
      }
}
```

Listing 1. Model Order Reduction Algorithm

A typical scheduling array might be Multiplier[]= {10,5,2.5,1.5,1}. The idea is simply to ensure that nodes with smaller time constants are eliminated before nodes with larger ones. At the cost of extra bookkeeping, an alternative is to maintain a priority queue sorted by nodal time constants and sequence branch-merges by taking from the top of the queue.

If the number of RL, C, and M branches incident on any node is bounded, the complexity of **BMReducer** is O(n), where n is the number of nodes in the circuit.

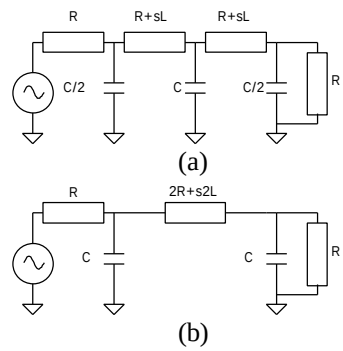

Fig. 3. (a) 2 p section. (b) 1 p section.

V. EXAMPLES

Our first example demonstrates how t_{RC} and t_{LC} demarcate the operating frequencies beyond which branch-merge should not be performed. Fig 3 shows a simple RLC circuit before and after branch merge. For simplicity, R=1Ω, C=1F, L=1H. We see in Fig. 4 that the frequency responses are nearly the same up to about $1/t_{RC} = 1/t_{LC} = 1\,Hz$. Beyond this frequency the 1-π circuit rolls off at 20dB/decade and the 2-π circuit at 40dB/decade. This example suggests that (3.5) can be interpreted as a requirement that the circuit operate below the cutoff or resonant frequency of the local mesh.

Our second example is a unit length transmission line with per-unit length parameters R=1Ω, C=1F, and L=1H. The line is fractured randomly into 500 sections, and each

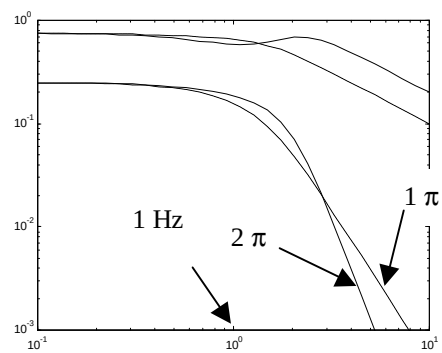

Fig. 4. Frequency Response of 1 and 2 p sections (C=R=L=1).

section is modeled as a RLC π circuit. In Fig. 5 we plot the response of the original circuit and the circuit obtained by applying the branch merge algorithm with $f^{\max} = 5$. The near-end and far-end waveforms of the original and reduced circuits are almost identical. Propagation delay due to inductance, evident in the figure, is faithfully captured by the reduced circuit. This example used a 1Ω driver with rise

time $t_r = 1$ s. Reduction amounts for this and the following examples are in Table 1.

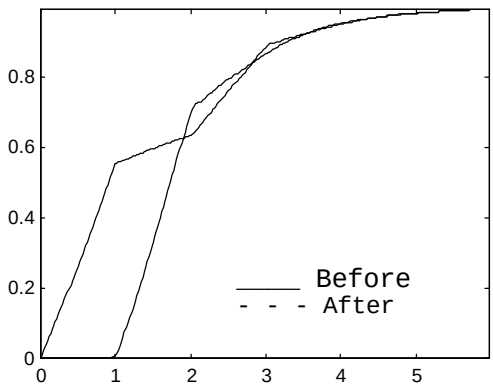

Fig. 5. Uniform T-line, R=1W, C=1 F, L=1 H, f^{max}=5

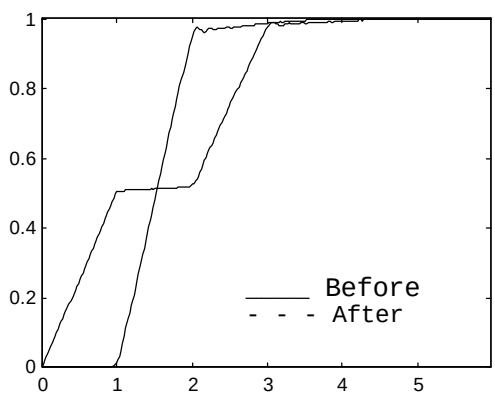

Fig. 6. Low-Loss T-line, R=0.1W, C=1 F, L=1 H, f^{max}=5

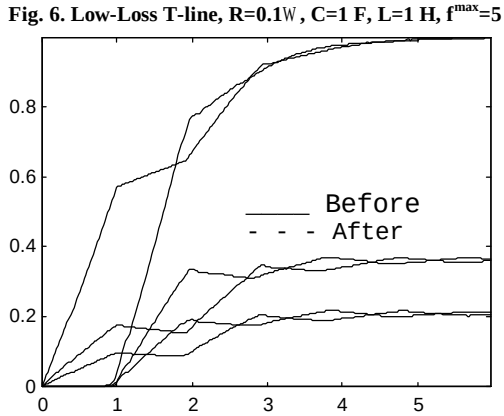

Fig.7. Response of 3 conductor bus, f^{max}=5

Figure 6 gives near and far end waveforms for an identical setup except that now R=0.1Ω/pul instead of 1.0Ω/pul. In this case (3.6) does not hold ($t_{RL}s = 10 >> 1$) but (3.5) does. The responses of the original and reduced circuits are again nearly identical, confirming the applicability of our algorithm to low loss transmission lines.

To indicate the effectiveness of the branch-merge algorithm applied to coupled lines, Fig. 7 plots waveforms for 3 traces of a bus one of which is driven. The bus is modeled by 200 equal-length coupled π sections. The original and reduced responses agree closely both for victims and aggressor.

Fig. 8 shows the results of reducing the same coupled 3 line bus (similar to the circuit of Fig. 7) multiple times using different values of $f^{\max}$. The abscissa is percentage reduction in node count and the ordinate is maximum percentage error in the response voltage when the reduced circuit is simulated with a driver rise time

$$t_r = CF/4f^{\max} \quad . \tag{5.1}$$

In Fig. 8 the constant CF—called the **conservation factor** since it measures the degree of conservatism in the reduction—is set at 20. The numbers annotating points are the values of $f^{\max}$ used in the corresponding reduction.

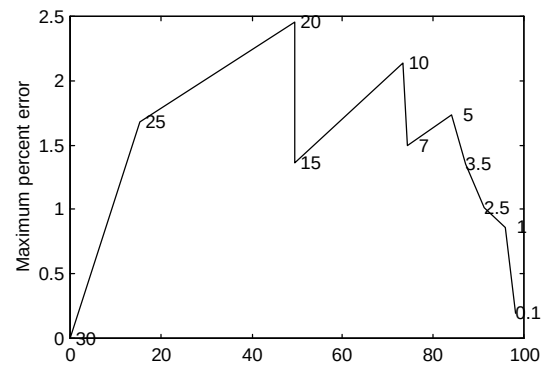

Fig. 8. Reduction of a 3 conductor bus for various fmax values. X-axis is percentage reduction, y-axis percentage error when simulated. Next to each point is the fmax used for that reduction.

A key point illustrated by Fig. 8 is that *reduction amount depend critically on intended operating frequency*. Fig. 8 is typical. One can have arbitrary reduction amounts by making $f^{\max}$ small enough, and the reduced circuit still will be accurate provided the driver's rise time t_r is related to $f^{\max}$ by (5.1). In practice, one starts with a knowledge of the likely t_r for a given technology and then computes from (5.1) a suitable $f^{\max}$ to use in reduction.

Amount of reduction also, of course, depends on the distribution of nodal time constants in the original circuit.

Circuit		Nodes	Branch Count		
			RL	C	M
Fig. 5	BEFORE	501	500	501	0
	AFTER	13	12	13	0
Fig. 6	BEFORE	501	500	500	0
	AFTER	13	12	13	0
Fig. 7	BEFORE	603	600	1206	600
	AFTER	99	96	390	96

Table 1. Circuit element counts before and after reduction.

Table 1 gives node and element counts before and after reduction for the circuit of Figures 5, 6, and 7. In the reductions underlying these figures, as well as in Fig. 8, a node was eliminated if *either* (3.5) or (3.6) was true. In

applying the legitimacy conditions, a test like $|t_{RC}s| << 1$ was replaced by $t_{RC} f^{\max} \le 1$, the 'much less than' requirement being taken into account by providing **BMReducer** with a suitably large $f^{\max}$ (e.g. $f^{\max} = 5$).

VI. Conclusion

This paper proposes an algorithm which, in our view, is ideal for parasitic extraction tools that must convert RLCM networks with broad, unregulated time constant profiles into compact circuits suitable for efficient and accurate simulation at designated edge-speeds.

In many ways the algorithm is an attempt to extend TICER to RLCM circuits—in particular, it extends TICER's idea of nodal time constants that guide nodal elimination. Years of industrial with TICER have shown that this approach works well for RC circuits. But inductance makes the question of time constant definition and legitimacy more delicate. Here we propose several time-constant criteria—e.g. (3.5) and (3.6). Our examples indicate that branch merge using these criteria works well on important practical circuits like low-loss clock lines and buses with significant electric and magnetic coupling. And provided $f^{\max}$ is suitably tied to the circuit-technology's edge-speed, the proposed legitimacy criteria maintain accuracy within a few percent. The algorithm is easy to implement, and very efficient—O(n)—making it applicable to the largest industrial circuits.

VII. Appendix

We prove Theorem 1. Our analysis begins with the modified nodal equations for node N in Fig. 1:

$$\underbrace{\begin{pmatrix} Y & -1 & -1 \\ 1 & Z_1 & sM \\ 1 & sM & Z_2 \end{pmatrix}}_{A} \begin{pmatrix} V_N \\ I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} \sum_p sC_{pN}V_p \\ V_1 - \sum_q sM_{1q}I_q \\ V_2 - \sum_r sM_{2r}I_r \end{pmatrix} \equiv \begin{pmatrix} YV_C \\ V_1 - V_{1M} \\ V_2 - V_{2M} \end{pmatrix}. \quad \text{(A.1)}$$

For brevity, we set

$$V_C \equiv \frac{\sum C_{pN}V_p}{\sum C_{pN}}, \quad V_{1M} \equiv -\sum sM_{1q}I_q, \quad V_{2M} \equiv -\sum sM_{2r}I_r ,$$

and Y is defined by (3.3).

As required by the 'all other conditions equal' clause in our definition of legitimacy, we take V_1 and V_2, all M branch currents, and far-node voltages on C branches as known.

Suppose that conditions (3.1) of Theorem 1 hold, and, for definiteness, suppose that $|\hat{Z}_1 Y| << 1$.

We first consider $|A|$, the determinant of the coefficient matrix in (A.1), for this quantity sets the poles and hence the dynamics of node N. It is straightforward to show that

$$|A| = (\hat{Z}_1 + \hat{Z}_2)(1 + YsM) + \hat{Z}_1\hat{Z}_2 Y , \quad \text{(A.3)}$$

$\hat{Z}_1, \hat{Z}_2$ being defined in (3.2). If (3.1) (i) and (ii) are true,

$$|A| = \hat{Z}_1(1 + YsM) + \hat{Z}_2(1 + YsM + \hat{Z}_1 Y) \approx \hat{Z}_1 + \hat{Z}_2 = Z \quad \text{(A.4)}$$

quantities small compared to 1 being neglected in the final step. If (3.1) holds, the dynamics of the node are largely determined by Z, the impedance of the merged branch.

Next, consider the current flowing, say, at node 1; by our definition of legitimacy, the net current at node 1 should be equal, or nearly equal, for the circuits of Fig. 1 and Fig. 2.

Solving (A.1) for I_1 of in Fig. 1, we get, after manipulation,

$$I_1 = \frac{1}{|A|}\{\overbrace{(V_1 + V_{1M} - V_2 - V_{2M})}^{\text{(1) I in branch Z of Fig. 2}} + \overbrace{Y\hat{Z}_2(V_1 - V_C)}^{\text{(2) Current in C's connected to Node 1 in Fig. 2}} + \underbrace{Y\hat{Z}_2 V_{1M}}_{\text{(3) Not included in branch-merged circuit}} + \underbrace{YsM(V_1 + V_{1M} - V_2 - V_{2M})}_{\text{(4) Small}}\} \quad \text{(A.5)}$$

a similar expression holding for I_2. Consider each of the terms in (A.5). $|A|$ nearly equaling Z of Fig. 2 (by A.4), the first term is substantially *I*, the current through the merged branch in Fig. 2. The second term, by (3.1)(iii) and (A.4), can be written

$$\frac{Y\hat{Z}_2}{|A|}(V_1 - V_C) \approx \frac{YR_2}{R_1 + R_2}(V_1 - V_C) = \sum_p \frac{sC_{pN}R_2}{R_1 + R_2}(V_1 - V_p) \quad \text{(A.6)}$$

use being made of the definitions of Y and V_C; accordingly, this term nearly equals the current in the displaced capacitors of Fig. 2—i.e., the capacitors that have been moved from node N to node 1 as part of the branch merge. The forth term in (A.5) is small compared to the first, by (3.1)(ii), and so may be neglected.

This leaves us with only term (3) to be accounted for. We argue that it is also negligible; for either $|\hat{Z}_1 Y| << 1$ or $|\hat{Z}_2 Y| << 1$ (or both), by (3.1)(i). If $|\hat{Z}_2 Y| << 1$, then term (3)—which has $\hat{Z}_2 Y$ as a factor—is negligible compared to the contribution of V_{1M} in term (1). Suppose instead that $|\hat{Z}_1 Y| << 1$. This means that, measured against Y, R_1 and $s(L_1 - M)$ are small; that is, branch Z_1 models a short piece of metalization; therefore, mutual inductances M_{1q} must also be small (a metal trace cannot have a small self inductance and a large mutual inductance); in other words, $V_{1M} = \sum_q M_{1q}I_q$ will tend to be small compared to Y, and $|Y\hat{Z}_2 V_{1M} / |A|| \le |YV_{1M}| << 1$ will almost always hold in practice though it is not a logical necessity.

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