A Statistical Approach to Estimate the Dynamic Non-Linearity Parameters of Pipeline ADCs

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Abstract

A fully-analytical approach to estimate the statistics of dynamic non-linearity parameters of pipeline analog-to-digital converters (ADCs) in the presence of circuit non-idealities including capacitance mismatches and non-ideal opamps is presented. These parameters include the spurious-free dynamic range (SFDR) and the signal to noise-and-distortion ratio (SNDR). The simple closed-form formulas for SFDR and SNDR presented here are useful for design automation of highly-linear pipeline ADCs in order to extract the required values for the circuit-level specifications of the sub-blocks of converters. Behavioral simulations are presented to show the accuracy of the proposed equations.

1. INTRODUCTION

Linearity is one of the most important specifications of an analog-to-digital converter (ADC), especially in high-speed and high-dynamic-range applications such as cellular base-station transceivers and multi-standard software radios. These modern communication systems with the ultimate goal of directly digitizing the RF signal [1] will require high-resolution highly-linear ADCs [2,3]. This is due to the wide bandwidth of the signal and the density of signal information.

The dynamic range of an ADC is mostly expressed by the spurious-free dynamic range (SFDR) [2], and signal to noise and distortion ratio (SNDR). The SFDR of an ADC is defined as the difference in decibel, between the full-scale fundamental tone and the largest spurious (harmonic) component in the output spectrum. In addition the SNDR is defined as the ratio of the signal power to the total noise and harmonic power at the output, when the input is a sine wave [4].

Pipeline ADCs (Figure 1) are the most popular architecture in high-speed medium-to-high-resolution applications. There have been several approaches proposed in literature for characterizing and calculating the non-linearity parameters of pipeline ADCs. In [5] a complete study of integral non-linearity (INL) and differential non-linearity (DNL) parameters is presented, whereas the dynamic parameters i.e. SFDR and SNDR are not considered. In [6] the total SFDR of a pipeline ADC is roughly approximated; but it does not present an exact relationship for the total SFDR. However, in this paper a comprehensive analysis of the dynamic non-linear effects in a pipeline ADC is presented. A set of accurate closed-form equations for the SFDR and SNDR which can be used in developing automated design CAD tools is also presented. The effects of the non-idealities in the residue-amplifier gain values arisen from circuit imperfections such as mismatch in capacitor values, finite DC gain of the operational amplifiers, and the settling errors of the residue amplifiers, in the SFDR and SNDR values of a pipeline ADC are investigated and the total spurious signal and total noise and distortion power are calculated. Finally, the behavioral Monte-Carlo simulation results are presented that clearly verify the accuracy of the given simple closed-form relations.
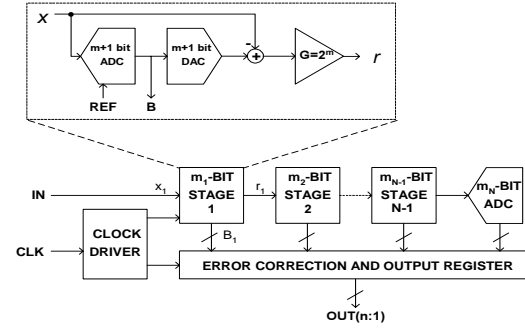
Figure 1. A generic pipeline ADC structure 2.

QUANTIZATION NON-LINEARITY

In an ideal quantizer, when no non-linearity and noise except the quantization non-linearity is existent, it has been shown that the maximum SNDR is [4]

$$SNDR \approx 6.02n + 1.76 \tag{1}$$

where n is the ADC resolution. In this case, the spurious signal is only produced by the quantization non-linearity. If a sine wave is passed through an ideal quantizer, the Fourier series of the output signal leads to the closed-form expression for the magnitudes of the harmonic signals [7] as

$$a_k = \frac{2LSB}{\pi k} \sum_{i=1}^{2^n} \sin(k \cos^{-1}(x_i)) \tag{2}$$

where x_i is the ith quantized level. The largest harmonic component (named H_q) is about $9n\text{-}c$ dB below the fundamental component [7] where the resolution-dependent offset c ranges from 0 for low resolutions to 6 for high resolutions (or even 8 for more than 12-bit resolutions). Thus, the SFDR is approximated by

$$SFDR \approx 9n - c \tag{3}$$

These equations obtained for an ideal quantization system, express that increasing one bit in the ADC resolution results in a 6dB increase in the SNDR value and a 9dB improvement in the SFDR value.

3. EFFECTS OF NON-IDEALITIES IN ADC LINEARITY

In a pipeline ADC shown in Figure 1, circuit imperfections such as capacitor mismatches, finite opamp DC gains, and incomplete settling of the residue amplifiers deteriorate the linearity of the ADC transfer function.

For every stage of an ADC, with 1 bit of resolution (m_i=1), one can write [8]

$$B_i = \begin{cases} -1 & x_i < 0 \\ 1 & x_i > 0 \end{cases} \tag{4}$$

$$r_i = \begin{cases} \left(1 - \frac{1}{a_i f_i} - e^{-T/\tau_i} + \frac{\Delta C_i}{2C_i}\right)2x_i + \left(1 - \frac{1}{a_i f_i} - e^{-T/\tau_i} + \frac{\Delta C_i}{C_i}\right) \cdot V_{ref} & x_i < 0 \\ \left(1 - \frac{1}{a_i f_i} - e^{-T/\tau_i} + \frac{\Delta C_i}{2C_i}\right)2x_i - \left(1 - \frac{1}{a_i f_i} - e^{-T/\tau_i} + \frac{\Delta C_i}{C_i}\right) \cdot V_{ref} & x_i > 0 \end{cases} \tag{5}$$

where B_i, r_i, a_i, f_i, T, τ_i, $\Delta C_i/C_i$ are the output digit, the output residue signal, the gain, the feedback factor, the dedicated time for settling, the time constant of the system, and the normalized capacitance mismatch of the ith residue stage. With these definitions, it is assumed that the sampling and amplification capacitors of the 1-bit stage have the deterministic values of $C+\Delta C/2$ and $C-\Delta C/2$, respectively, and the statistical behavior of the capacitive mismatch and gain are not considered yet. x_i is the input signal of the ith stage that is also the residue signal of the previous stage. In order to have shorter expressions for the equations, we define

$$\delta g_i = -\frac{1}{a_i f_i} - e^{-T/\tau_i} \quad \text{and} \quad \delta C_i = \frac{\Delta C_i}{C_i} \quad (6)$$

and assuming $V_{ref}=1$, we can rewrite (5) as

$$r_i = \begin{cases} \left(1+\delta g_i + \frac{1}{2}\delta C_i\right)2x_i + \left(1+\delta g_i + \delta C_i\right) & , x_i < 0 \\ \left(1+\delta g_i + \frac{1}{2}\delta C_i\right)2x_i - \left(1+\delta g_i + \delta C_i\right) & , x_i > 0 \end{cases} \quad (7)$$

Assuming that r_1 i.e. the residue of the first stage is perfectly digitized by the following stages and no error is added to its value, it can be stated that the digital equivalent value for the output word of the ADC, is obtained from

$$X_1 = \left(B_1 \times 2^{-1} + r_1/2\right) \quad (8)$$

Making use of (4) and (7) in (8) result in

$$X_1 = \left(1+\delta g_1 + \frac{1}{2}\delta C_1\right)x_1 + \begin{cases} +\frac{1}{2}\left(\delta g_1 + \delta C_1\right) & x_1 < 0 \\ -\frac{1}{2}\left(\delta g_1 + \delta C_1\right) & x_1 > 0 \end{cases} \quad (9)$$

In an ideal ADC the input-output transfer curve is a straight line with a gain of unity (Figure 2(a)). However, as shown in (9), a non-ideality in the first stage leads to a total gain error of $(1+\delta g_1+\frac{1}{2}\delta C_1)$ instead of 1 and a breaking point at zero in the input-output curve as shown in Figure 2(b). This breaking point caused by the first stage non-ideality leads to a non-linearity in the entire ADC. Of course, the jump value at this breaking point located at zero in a practical converter is also affected by the non-ideality of the succeeding stages. In order to investigate this effect, consider that the second stage has a non-ideal transfer characteristics expressed by (4) and (5). The digital equivalent of the second stage input, r_1, can be determined as follows

$$X_2 = \left(1+\delta g_2 + \frac{1}{2}\delta C_2\right)r_1 + \begin{cases} +\frac{1}{2}\left(\delta g_2 + \delta C_2\right) & , r_1 < 0 \\ -\frac{1}{2}\left(\delta g_2 + \delta C_2\right) & , r_1 > 0 \end{cases} \quad (10)$$

Hence, the second stage non-ideality leads to 3 breaking points as depicted in Figure 2(c). It can be easily shown that the height of the jump at the middle breaking point, located at zero, is equal to $+\frac{1}{2}\delta g_2$. The height of the breaking point at zero for the combination of two non-ideal stages will be determined by the sum of the effects of both stages as $(\delta g_1+\delta C_1+\frac{1}{2}\delta g_2)$. The effect of other two breaking points arisen from the second stage will be discussed when the second stage non-linearity effects are discussed.

In a 1.5-bit residue stage considering the fact that the amplifier's gain is again equal to 2, it can be easily shown that (7) can be rewritten as [8]

$$r_1 = \begin{cases} \left(1+\delta g_1 + \frac{1}{2}\delta C_1\right)2x_1 + \left(1+\delta g_1 + \delta C_1\right) & , x_1 < -\frac{1}{4} \\ \left(1+\delta g_1 + \frac{1}{2}\delta C_1\right)2x_1 & , -\frac{1}{4} < x_1 < \frac{1}{4} \\ \left(1+\delta g_1 + \frac{1}{2}\delta C_1\right)2x_1 - \left(1+\delta g_1 + \delta C_1\right) & , x_1 > \frac{1}{4} \end{cases} \quad (11)$$

Therefore, in the input-output transfer curve, a similar gain error to what extracted for the 1-bit case and two breaking points at $-\frac{1}{4}$ and $\frac{1}{4}$ occur as shown in Figure 2(d). For the digital equivalent output of the ADC, similar to what expressed for (9), one can write

$$X_1 = f(x_1) = \left(1+\delta g_1 + \frac{1}{2}\delta C_1\right)x_1 + \begin{cases} +\Delta e_1/2 & , x_1 < -\frac{1}{4} \\ 0 & , -\frac{1}{4} < x_1 < \frac{1}{4} \\ -\Delta e_1/2 & , x_1 > \frac{1}{4} \end{cases} \quad (12)$$
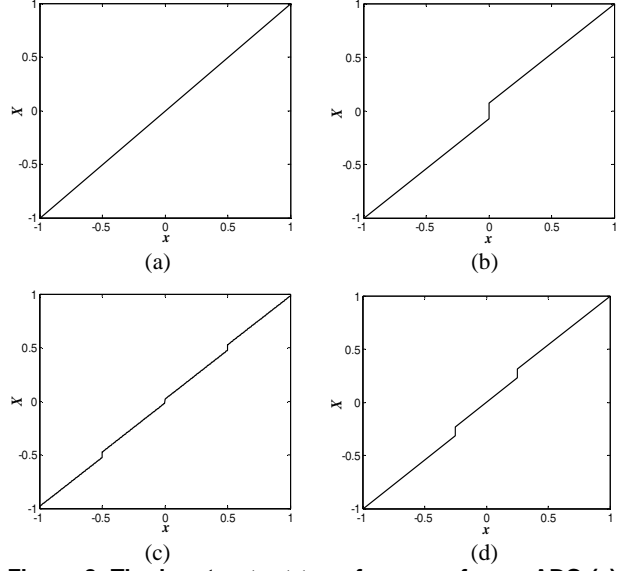

Figure 2. The input-output transfer curve for an ADC (a) ideal, (b) with a non-ideal first stage of 1-bit (Gain<2), (c) with two successive 1-bit stages in front-end with non-ideality only in the second stage, (d) with non-ideal first stage of 1.5-bit.

where $\Delta e_1/2$ is the jump at $-\frac{1}{4}$ and $\frac{1}{4}$. Since this jump will be affected by its following stage, using similar strategy stated for the 1-bit case, it can be shown that for a 1.5-bit stage Δe_i is equal to

$$\Delta e_i = \delta g_i + \delta C_i - \frac{1}{2}\delta C_{i+1} \quad (13)$$

It is evident that (13) is obtained assuming a deterministic behavior for capacitive mismatches and also gain errors. To have a statistical approach, assume that the δg_i and δC_i are normally-distributed variables with variance of $\sigma^2_{\delta g_i}$ and $\sigma^2_{\delta C_i}$, respectively. Therefore, Δe_i will be a normally-distributed variable with the variance value of

$$\sigma^2_{\Delta e_i} = \sigma^2_{\delta C_i} + \sigma^2_{\delta g_i} + \sigma^2_{\delta C_{i+1}}/4 \quad (14)$$

Here it is assumed that the mean values of δg_i and δC_i are zero.

In order to determine the power of the total harmonics of such an ADC, an ideal n-bit quantizer following a non-ideal system with a transfer function of $f(x)$ expressed in (12) is considered. Assuming a sine-wave input $x(t)=\cos(t)$, using Fourier series expansion, one can write

$$f(x(t)) = \frac{a_0}{2} + \sum_{k=1}^{\infty} (a_k \cos(k \cdot t) + b_k \sin(k \cdot t)) \quad (15)$$

The amplitude of the kth harmonic signal is obtained from

$$a_k = \begin{cases} \frac{1}{k\pi}\left[\cos(k\alpha_1) - \cos(k\alpha_2)\right] \cdot \Delta e_1 & k > 1 \\ \left(1+\delta g_1 + \frac{1}{2}\delta C_1\right) + \frac{1}{\pi}\left[\cos(\alpha_1) - \cos(\alpha_2)\right] \cdot \Delta e_1 & k = 1 \\ 0 & k = 0 \end{cases} \quad (16)$$

where $\alpha_1 = \sin^{-1}(\frac{1}{4})$, $\alpha_2 = \pi - \sin^{-1}(\frac{1}{4})$ and $b_k=0$ for all ks.

From (16), it is observed that the magnitudes of the even harmonic components are zero and the largest harmonic component is found to be the third one, approximately equal to

$$a_3 \approx 0.155\Delta e_1 \quad (17)$$

The third harmonic component due to the ith stage can be similarly extracted. For a sine wave applied to its input, the largest harmonic component in the digital equivalent of the input of the ith stage, is obtained from

$$a_{3,i} = 0.155\Delta e_i \qquad (18)$$

In order to calculate the effect of this harmonic component in the digital equivalent of the input of the entire ADC, the magnitude of the harmonic component is divided by the voltage gain of the preceding stages as

$$a_{3-input\ reffered} = 0.155 \times 2^{-(i-1)}\Delta e_i \qquad (19)$$

In the entire ADC, with non-idealities in all stages, it can be stated that the third harmonic component is derived from the summation of the third harmonic components of all residue stages, therefore

$$a_3 = 0.155 \times \sum_{i=1}^{n} 2^{-(i-1)}\Delta e_i \qquad (20)$$

As Δe_is are stochastic variables with normal distribution, the third harmonic of the converter is also a normally-distributed variable with the variance value of

$$\sigma_{a_3}^2 = 0.155^2 \times \sum_{i=1}^{n} 2^{-2(i-1)}\sigma_{\Delta e_i}^2 \qquad (21)$$

Since Δe_is are not totally uncorrelated, for (21) to be true, it can be shown that $\sigma^2_{\Delta e_i}$ should be changed as

$$\sigma^2_{\Delta e_i} = \sigma^2_{\delta C_i} + \sigma^2_{\delta g_i} - \sigma^2_{\delta C_{i+1}}/4 \qquad (22)$$

4. SFDR CALCULATION

4.1 Residue Stages of 1.5 Bits

In order to calculate the spurious-free dynamic range of the pipelined ADC composed of 1.5-bit residue amplifiers, the largest harmonic component should be determined. It is known that the largest harmonic component caused by the quantization non-linearity (named H_q) is certainly not the third harmonic component [7] and its magnitude is $9n\text{-}c$ dB below the fundamental component [7]. Therefore, it can be concluded that the magnitude of the largest spurious signal is the maximum value of either a_3 determined in (20) or H_q. As a result, the spurious-free dynamic range is obtained from

$$SFDR = \min\{9n-c, 20 \cdot \log(1/a_3)\} \qquad (23)$$

As mentioned before, a_3 is a random variable where its variance value was derived in (21). In order to estimate the one-sigma SFDR, one can show that the corresponding a_3 is obtained from

$$a_{3,one-sigma} = \sigma_{a_3} \qquad (24)$$

Using (21), (23) and (24) it can be concluded that the total SFDR is

$$SFDR = \min\{9n - c, 16.2 - 10 \cdot \log(\Delta E)\} \qquad (25)$$

where $20\log(0.155) = -16.2$, and

$$\Delta E = \sum_{i=1}^{n} 2^{-2(i-1)}\sigma_{\Delta e_i}^2 \qquad (26)$$

As can be seen from (25) and (26), every halving ΔE results in 3dB improvement in SFDR. Besides, the non-idealities of the front-end stages have bigger effect on the total SFDR.

4.2 Residue Stages of more than 1.5 Bits

In order to determine the SFDR in an ADC with stage resolutions of more than one effective bit, the input-output transfer function for a residue amplifier of m effective bits should be calculated. In a conventional m-effective-bit residue stage with 2^m equal capacitors, the input-output transfer function of the residue amplifier is obtained from [9]

$$r = (1+\delta g)\left(\left(1 + \sum_{k=1}^{2^m-1}\frac{C_{S,k}}{C_F}\right)x + \sum_{k=1}^{2^m-1}\frac{d_k C_{S,k}}{C_F}\right) \qquad (27)$$

where d_k is either 0 or ± 1, depending on the sub-ADC outcome. C_F is the feedback capacitor and $C_{S,k}$ is the kth sampling capacitor in the residue amplifier.

The mismatch for the kth capacitor of the residue stage is defined as

$$\delta C_k = \frac{C_{S,k} - C_F}{C} \qquad (28)$$

So (27) can be rewritten as

$$r = \left(1 + \delta g + \sum_{k=1}^{2^m-1}\frac{\delta C_k}{2^m}\right)2^m x + \sum_{k=1}^{2^m-1}(1+\delta g + \delta C_k)\cdot d_k \qquad (29)$$

Such non-idealities in the m-bit residue stage, result in a total

gain error of $\left(1 + \delta g + \sum_{k=1}^{2^m-1}\dfrac{\delta C_k}{2^m}\right)$ and $(2^{m+1}\text{-}2)$ breaking points

with heights of

$$\Delta_k = (\delta g + \delta C_k)\Big/ 2^m \qquad (30)$$

In order to estimate the harmonic component of such an input-output transfer curve, a sine wave is applied as the input and the harmonic component of the output wave is analyzed.

Using similar strategy utilized in deriving (16), it can be shown that the even harmonic components are zero and the odd harmonic components are obtained from

$$a_K = \frac{4}{K\pi}\sum_{k=1}^{2^m-1}\cos\left(K\sin^{-1}\left(\frac{2k-1}{2^{m+1}}\right)\right)\Delta_k \qquad K>1 \quad (31)$$

It can be seen that the biggest harmonic component is the third one. As Δ_ks are normally-distributed variables, the third harmonic component of the converter has also a normal distribution with the variance value of

$$\sigma_{a_3}^2 = \frac{1}{2^{2m}}\left(\frac{4}{3\pi}\right)^2 \cdot \Bigg\{ \sum_{k=1}^{2^m-1}\cos^2\left(3\sin^{-1}\left(\frac{2k-1}{2^{m+1}}\right)\right)\cdot\sigma_{\delta C_k}^2 $$
$$+ \left(\sum_{k=1}^{2^m-1}\cos\left(3\sin^{-1}\left(\frac{2k-1}{2^{m+1}}\right)\right)\right)^2 \cdot \sigma_{\delta g}^2 \Bigg\} \qquad (32)$$

In this residue amplifier, all Cs have the same mean value. Therefore the capacitor mismatches have similar variances, to be named $\sigma^2_{\delta C}$. For ith residue stage we name it as $\sigma^2_{\delta C_i}$.

Using some simplifications in (32), and considering the next stage effect on the heights of the previous stage break points, the input-referred variance value for the third harmonic component for the ith stage of a pipeline ADC, is approximated by

$$\left(\sigma_{a_3}^2\right)_i = 0.155^2 \cdot 2^{2\left(1-\sum_{j=1}^{i} m_j\right)}\left(\sigma_{\delta g_i}^2 + \left(2^{m_i}-1\right)\sigma_{\delta C_i}^2 - \frac{1}{2^{2m_{i+1}}}\sigma_{\delta C_{i+1}}^2\right) \qquad (33)$$

So, in the entire pipeline ADC, one can write

$$SFDR = \min\{9n - c, 16.2 - 10 \cdot \log(\Delta E)\} \qquad (34)$$

$$\Delta E = \sum_{i=1}^{N} 2^{2\left(1-\sum_{j=1}^{i} m_j\right)}\left(\left(2^{m_i}-1\right)\sigma_{\delta C_i}^2 + \sigma_{\delta g_i}^2 - \frac{1}{2^{2m_{i+1}}}\sigma_{\delta C_{i+1}}^2\right) \qquad (35)$$

where N and m_j are the number of residue stages and the effective resolution of jth residue stage (see Figure 1), respectively.

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5. SNDR CALCULATION

The total input-referred distortion of the converter can be obtained from

$$P_{dstr} = \sum_{i=2}^{\infty} \left(a_i / \sqrt{2} \right)^2 \tag{36}$$

where a_i is the magnitude of the ith input-referred harmonic component of the entire converter. As the harmonic components of the converter stages are assumed uncorrelated, in order to estimate the average power of the spurious signals due to circuit imperfections, the input-referred spurious power of each stage should be calculated (using (31) and (36)) and then added to estimate that of the entire ADC. This will lead to an estimation of the total spurious power as

$$P_{dstr} = 0.02 \left(\sum_{i=1}^{N} (2f)^{2\left(1-\sum_{j=1}^{i} m_j\right)} \left(\begin{array}{l} \left(2^{m_i}-1\right)\sigma_{\delta C_i}^2 + \sigma_{\delta g_i}^2 \\ + \dfrac{1}{2^{2m_{i+1}}}\sigma_{\delta C_{i+1}}^2 \end{array} \right) \right) \tag{37}$$

where f is a fitting parameter equal to 0.95.

This distortion power is added to what arises from quantization non-linearity, thus

$$P_{dstr,TOTAL} = P_{dstr} + \frac{(V_{FS}/2^n)^2}{12} \tag{38}$$

and V_{FS} is the full-scale (reference) voltage of the converter.

As considered in (15), the amplitude of the input sine wave is 1 and so V_{FS}=2 . Therefore

$$\frac{V_{FS}^2}{12 \times 2^{2n}} = 0.333 \times 2^{-2n} \tag{39}$$

By using (38) and (39), the total distortion plus noise is obtained from

$$P_{D+N} = P_{dstr} + 0.333 \times 2^{-2n} + \alpha(kT/C) \tag{40}$$

Having known P_{signal}=1/2, the total SNDR is obtained from

$$SNDR = 6.02n - 10\log\left(2^{2n+1}\left(P_{dstr} + \alpha kT/C\right) + 0.667\right) \tag{41}$$

6. SIMULATION RESULTS

A complete ADC circuit has a great number of devices and a comprehensive Monte-Carlo SPICE simulation through a large number of points (to extract the exact value of the SFDR and SNDR) is time consuming. Hence, in order to model the behavior of a pipeline ADC, using MATLAB a behavioral simulation tool of such an ADC in which the non-ideal agents of the residue stages are taken into account, is developed. In order to simulate the residue stages behaviorally, equations (11) and (27) were employed. In order to estimate the value of SFDR and SNDR when the statistical behavior of δg and δC are known, a Monte-Carlo simulation with normal distribution for δg and δC is performed and then the average power of the largest spurious signal and the average value of the total spurious power is used to extract the value of the SFDR and SNDR, respectively.

Figure 3 shows the dependency of the total SFDR and SNDR of a 12-bit 1.5-bit/stage pipeline ADC on the values of $\sigma_{\delta g}$ for two values of $\sigma_{\delta C}$. Note that δg and δC for all stages are taken with similar variance yet uncorrelated. It shows a very good agreement between the Monte-Carlo simulation results and the proposed equations. Figure 4 shows the dependency of the total SFDR and SNDR of a 12-bit pipeline ADC with a first-stage resolving 3-effective bits and 1.5 bits for all other stages on the values of $\sigma_{\delta g}$ for two values of $\sigma_{\delta C}$. A good agreement between the proposed formulas and simulation results is again achieved.

7. CONCLUSION

In this paper, a fully analytical approach to the estimation of the statistics of SFDR and SNDR for a pipeline ADC is presented. Using the proposed simple closed-form formulas for SFDR and SNDR, the required accuracies of the residue-amplifiers gain

values as well as the mismatches in the capacitors to satisfy a particular SFDR and a specific distortion budget can be extracted. The Monte-Carlo simulation results confirm the accuracy of the proposed formulas. These formulas can be employed in CAD tools as well as hand calculation in pipeline ADC designs.
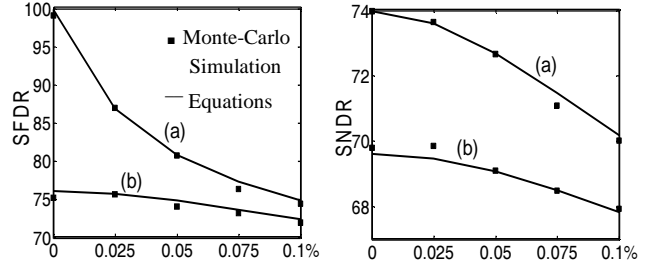

Figure 3. Values of SFDR and SNDR of a 12-bit 1.5-bit/stage pipeline ADC versus $\sigma_{\delta g}$ of all stages for (a) $\sigma_{\delta C}$=0, (b) $\sigma_{\delta C}$ =0.1%.
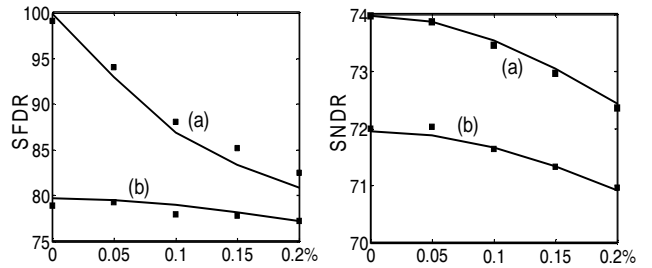

Figure 4. Values of SFDR and SNDR of a 12-bit pipeline ADC with a first-stage resolving 3-effective bits and 1.5 bits for all other stages versus $\sigma_{\delta g}$ of all stages for (a) $\sigma_{\delta C}$=0, (b) $\sigma_{\delta C}$ =0.1%.

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