# TAM Optimization for Mixed-Signal SOCs using Analog Test Wrappers

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## Abstract

*We present a new approach for TAM optimization and test scheduling in the modular testing of mixed-signal SOCs. A test planning approach for digital SOCs is extended to handle analog cores in a plug-and-play fashion. A test wrapper based on an ADC/DAC pair and a digital configuration circuit is designed for analog cores such that these cores can be accessed through digital TAMs. In this way, there is no dependence on an analog test bus and expensive mixed-signal testers. Experimental results are presented for several ITC'02 SOC test benchmarks to which three analog cores are added. The results show that the testing of analog cores can be interleaved with the testing of digital cores to reduce the overall testing time for a mixed-signal SOC.*

## 1 Introduction

Modular testing of embedded cores in a system-on-a-chip (SOC) is being increasingly advocated to simplify test access and test application [1]. Test wrappers are used to isolate a core, while test access mechanisms (TAMs) transport test patterns and test responses between SOCs pins and core I/Os. Prior research on modular testing of SOCs has focused almost exclusively on the digital cores in an SOC. However, most SOCs in use today are mixed-signal circuits containing both digital and analog cores [2, 3]. Therefore, an effective modular test methodology should be capable of handling both digital and analog cores

In traditional mixed-signal SOC testing, tests for analog cores are applied either from chip pins through direct test access methods, e.g., via multiplexing, or through a dedicated analog test bus [4, 5], which requires the use of expensive mixed-signal testers. For mid- to low-frequency analog applications, the data is often digitized at the tester, where it is affordable to incorporate high quality data converters. In most mixed-signal ICs, the total production testing cost is dominated by analog testing costs. This is because of the fact that expensive mixed-signal testers are employed for extended periods of time. A natural solution to this problem is to implement the data converters on-chip. Until recently, such an approach has not been deemed desirable due to its high hardware overhead. However, as the cost of on-chip silicon is decreasing, and the functionality and the number of cores in a typical SOC are increasing, the addition of data converters on-chip for testing analog cores now promises to be cost-efficient. These data converters eliminate the need for expensive mixed-signal test equipment.

In this work, we focus on the optimization of a unified test access architecture that is used for both digital and analog cores. In this way, we formulate a global test resource optimization problem for the entire SOC, instead of treating the digital and analog portions separately. In order to provide an efficient interface mechanism, we propose to wrap each analog core by an DAC-ADC pair and a digital configuration circuit. We describe how existing SOC test planning methods can be augmented to handle analog cores in a plug-and-play fashion. Experimental results are presented for three SOCs from the ITC '02 test benchmarks that have been augmented with three analog cores: an I-Q transmit path pair and an audio CODEC path used in cellular phone applications. These results show that for "big D/small A" SOCs, the testing time and test cost can be reduced considerably if the analog cores are wrapped, and the test access and test scheduling problems for the analog and digital cores are tackled in a unified manner.

## 2 Review of Prior Work

TAM optimization has been the focus of a considerable amount of research recently, and a number of techniques have been proposed for designing efficient test access architectures and for test scheduling [6]-[8]. A method to solve the TAM optimization problem for fixed-width test buses was presented in [9]. The TAM optimization problem was formulated as follows.
Determine (i) the number $B$ of TAMs for the SOC, (ii) a partition of the total TAM width $W$ among the TAMs, (iii) an assignment of the $N$ cores to TAMs, and (iv) a wrapper design for each core, such that SOC testing time is minimized.
This was shown to be an $\mathcal{NP}$-hard problem in [9].

The problem of wrapper design was solved using the *Design_wrapper* algorithm based on the Best Fit Decreasing heuristic from Bin Packing [9]. The core assignment problem was solved using an ILP model constructed as follows.
Consider an SOC consisting of $N$ cores and $B$ TAMs of widths $w_1, w_2, \ldots, w_B$. The time taken to test Core $i$ assigned to TAM $j$, given by $T_i(w_j)$ clock cycles, is calculated using *Design_wrapper*. Binary variables $x_{ij}$ where $1 \leq i \leq N$ and $1 \leq j \leq B$, are used to determine the assignment of cores to TAMs in the SOC. The $x_{ij}$ variable is 1 if Core $i$ is assigned to TAM $j$, otherwise it is 0. The time needed to test all cores on TAM $j$ is given by $\sum_{i=1}^{N} T_i(w_j) \cdot x_{ij}$. Since all the TAMs can be used simultaneously for testing, the system testing time equals $\max_{1 \leq j \leq B} \sum_{i=1}^{N} T_i(w_j) \cdot x_{ij}$. The ILP model for core assignment can be formulated as follows.
Objective: Minimize testing time $\mathcal{T}$, subject to
1. $\mathcal{T} \geq \sum_{i=1}^{N} T_i(w_j) \cdot x_{ij}, 1 \leq j \leq B$, i.e., $\mathcal{T}$ is the maximum testing time on any TAM.
2. $\sum_{j=1}^{B} x_{ij} = 1$, $1 \leq i \leq N$, i.e., every core is assigned to exactly one TAM.
In [7], a fast three-step heuristic method was presented to design TAM architectures for large SOCs containing multiple TAMs. In the first step, a heuristic algorithm *Core_assign* for core assignment to TAMs is used. In the second step, width partitions for a large number of TAMs are enumerated and evaluated. The algorithm termed *Partition_evaluate* employs several levels of solution-space pruning during width partition evaluation. This result is improved by performing a third optimization step using the ILP model for core assignment.


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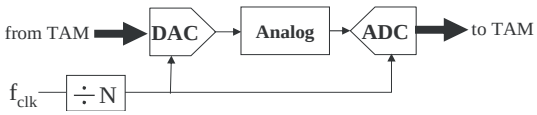


**Figure 1.** On-chip digitization of analog test data.

In the analog domain, most of the test research has concentrated on defining core-level measurement and test methods. In order to reduce the overall test time for analog circuits, a subset of specifications to be tested is selected based on parameter correlations [10, 11].

Automated generation of test stimuli is the aim of approaches outlined in [12], which employ output signal sensitivity to circuit parameters. Test inputs are defined as single tone sinusoidal signals with frequency as an unknown parameter. The frequency at which the sensitivity of the (voltage gain) is highest to a given component is selected to test it.

In order to obviate the need for analog testers, the use of on-chip data converters has been proposed [13, 14]. In [13], the outputs of several single-tone signal generators based on digital filtering are added to generate a multi-tone signal; this signal generator then is used to measure inter-modulation distortion and frequency response through an on-chip signal processor [15].

In [14], the analog circuitry is assumed to be placed between an ADC and a DAC, and is tested through pseudo-random digital patterns. Such pseudo-random digital patterns are considered to have similar characteristics as white noise which covers a wide frequency spectrum. The correlation between the output samples and the discretized transfer function is then utilized to determine the pass/fail criteria.

# 3 Test Wrapper for Analog Cores

In order to facilitate a unified test access mechanism for the overall SOC, it is necessary to convert analog test signals and responses into the digital domain. Each analog core has to be provided a test wrapper where the test information includes only digital test patterns, clock frequency, the test configuration, and pass/fail criteria. This analog test wrapper converts the analog core to a virtual digital core with strictly sequential test patterns, which are the digitized analog signals. In order to utilize test resources efficiently, the analog wrapper needs to provide sufficient flexibility in terms of required resources with respect to all the test needs of the analog core. One way to achieve this uniform test access scheme for analog cores is to provide an on-chip ADC-DAC pair that can serve as an interface between each analog core and the digital surroundings, as shown in Figure 1.

In the design of the analog test wrapper, issues regarding the test needs of the analog cores and flexibility in terms of test resource utilization need to be properly addressed in order to achieve efficient test schedules.

Analog tests are provided by the core vendor to the system integrator. In case of analog testers, these signals are digitized at the high precision ADCs and DACs of the tester. In case of on-chip digitization, the analog wrapper needs to include the lowest cost data converters that can still provide the required frequency and accuracy for applying the core tests. Thus, on-chip conversion of each analog test to digital patterns imposes requirements on the

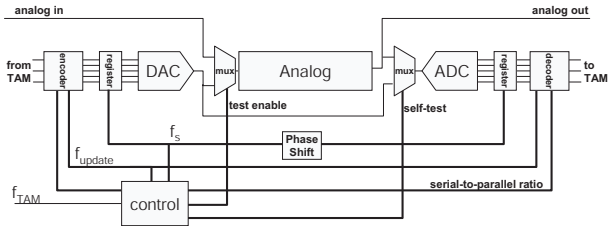


**Figure 2.** Block diagram of the analog test wrapper.

frequency and resolution of the data converters of the analog wrapper. These converters need to be designed to accommodate all the test requirements of the analog core.

Analog tests may also have a high variance in terms of their frequency and test time requirements. While tests involving low-frequency signals require low bandwidth and high test times, tests involving high-frequency signals require high bandwidth and low test time. Keeping the bandwidth assigned to the analog core constant results in under-utilization of the precious test resources. The variance of analog test needs have to be fully exploited in order to achieve an efficient test plan. Thus, the analog test wrapper has to be designed to accommodate multiple configurations with varying bandwidth and frequency requirements.

Figure 2 shows the block diagram of the proposed analog wrapper that can accommodate all the abovementioned requirements. The control and clock signals generated by the test control circuit are highlighted. The registers at each end of the data converters are written and read in a semi-serial fashion depending on the frequency requirement of each test. The digital test control circuit selects the configuration for each test. This configuration includes the divide ratio of the digital TAM clock, the serial to parallel conversion rate of the input and output registers of the data converters, and the test modes.

## 3.1 Analog Test Wrapper Modes

In the normal mode of operation, the analog test wrapper is completely by-passed; the analog circuit operates on its analog input/output pins. During testing, the analog wrapper has two modes, a *self-test* mode and a *core-test* mode. Before running any tests on the analog core, the wrapper data converters have to be characterized for their conversion parameters, such as the non-linearity and the offset voltage. The self-test mode is enabled through the analog multiplexer at the input of the wrapper ADC, as shown in Figure 2. The parameters of the DAC-ADC pair are determined in this mode and are used to calibrate the measurement results. Once the self-test of the test wrapper is complete, core test can be enabled by turning off the *self-test* bits.

For each analog test, the encoder is set to the corresponding serial-to-parallel conversion ratio ($cr$), where it shifts the data from the corresponding TAM inputs into the register of the ADC. Similarly, the decoder shifts data out of the DAC register. The update frequency of the input and output registers, $f_{update} = f_s \times cr$, is always less than the TAM clock rate, $f_{TAM}$. For example, if the test bandwidth requirement is 2 bits and the resolution of the data converters is 12 bits, the input and output registers of the data converters are clocked at a rate 6 times less than the clock of the encoder, and the input data is shifted into the encoder and out of the decoder at a 2-bits/cycle rate. The complexity of the encoder and the decoder depends on the number of distinct bandwidth and

TAM assignments (the number of possible test configurations). In order to limit the complexity of the encoder-decoder pair, the number of such distinct assignments have to be limited. This requirement can be imposed in the test scheduling optimization algorithm.

### 3.2 Design of Wrapper Data Converters

As in the digital case [1], analog wrappers can be designed either by the core provider or by the system integrator. In the first scenario, the system integrator only needs to know the clock frequency and test patterns. This approach provides the system integrator high flexibility in terms of test resource partitioning, and the core provider the chance to fine-tune the converter design with respect to the core test needs. However, it also results in high test hardware overhead. A more frugal approach is to let the system integrator design the data converters, which can be shared by several cores. In this case, each core provider supplies the information about the performance requirements of the data converters, such as maximum frequency of operation, or resolution. With the added flexibility of sharing data converters among several analog cores, the hardware overhead can be greatly reduced.

The design of data converters used in SOC applications is challenging due to the need to optimize for speed, resolution, and power consumption. However, designing test wrappers is expected to be easier as power consumption is of lesser concern for test hardware since these converters are turned off during the normal mode of operation.

## 4 Analog Tests and Test Requirements

In order to utilize a ADC-DAC pair as an interface mechanism for an analog core, its operational frequency must be within the Nyquist frequency of the data converters. In addition, the data converters must provide adequate resolution to apply and observe the weakest test signal given by the core providers. Data converters with 10-bit resolution that can work at several hundred MHz are available in CMOS technology today [16]. Thus, the conditions on the frequency and the resolution of the data converters preclude only RF applications from the unified TAM architecture. This is not a stringent limitation since most SOC analog data acquisition and processing is limited to low- to mid-frequencies [2]. An analog test can be represented in terms of a sampling frequency and a number of samples to be taken. The sampling frequency has to be adjusted so as to meet the Nyquist criterion for the highest frequency signal component. The number of samples need to be set so that at least several full periods of the lowest frequency signal component are sampled. If an analog test contains frequencies ranging from $f_{min}$ to $f_{max}$, the sampling frequency $f_s$ has to be higher than $2f_{max}$. The test time has to be long enough to cover at least two full periods of the lowest frequency signal, thus it has to be higher than $2/f_{min}$.

In order to prevent any signal distortion, the analog signal has to be sampled at uniform intervals. As a result, an analog core requires a TAM with a bandwidth that is capable of providing data at the required sampling frequency $f_s$. In order to incorporate this condition into the test resource allocation algorithm described in Section 2, the cost of assigning a smaller bandwidth to the analog core is set to be infinite. If a TAM with adequate bandwidth is available, the cost is defined in terms of the test time. The test time is expressed as the digital clock cycles, and depends on the frequency ratio of the TAM clock and the sampling frequency. As a result, the resource requirements of the analog core are given by: $T = N_s \cdot f_{TAM}/f_s; \quad w \geq f_s/f_{TAM} \cdot max(R_{ADC}, R_{DAC})$ where $T$ is the time in clock cycles, $f_s$ is the sampling frequency, $f_{TAM}$ is the TAM clock frequency, $N_s$ is the number of samples to be collected, $w$ is the required TAM width, and $R_{ADC}$ & $R_{DAC}$ represent the number of bits of the data converters. While each analog test has to be applied in a non-preemptive manner, individual tests can be applied at distinct points in time, providing greater flexibility in test scheduling.

| Cores: I-Q transmit | | | | |
|---|---|---|---|---|
| | $f_{min}$ | $f_{max}$ | $f_s$ | $T$ |
| $G_{pb}$ | 50kHz | 50kHz | 1.5MHz | 50,000 |
| $f_c$ | 450kHz | 550kHz | 15MHz | 13,653 |
| $G_{1MHz}$ & $G_{2MHz}$ | 1MHz | 2MHz | 8MHz | 12,643 |
| $IIP_3$ | 50kHz | 250kHz | 8MHz | 26,973 |
| $V_{off_{DC}}$ | DC | DC | 10kHz | 700 |
| $\Phi_{off}$ | 200kHz | 400kHz | 15MHz | 32,000 |
| Core: CODEC Audio | | | | |
| $G_{pb}$ | 20kHz | 20kHz | 640kHz | 80,000 |
| $f_c$ | 45kHz | 55kHz | 1.5MHz | 136,533 |
| $THD$ | 2kHz | 31kHz | 2.46MHz | 83,252 |

**Table 1.** Test requirements for the analog cores.

## 5 Experimental Results

There are two advantages of using the proposed analog test wrapper in conjunction with the unified test resource optimization approach. First, by obviating the need for mixed-signal testers, the test equipment cost can be reduced. Second, by exploiting the variance in analog test needs in terms of the sampling frequency and the bandwidth, the overall test time can be reduced. We have taken a two step approach in comparing the results of the proposed method with the baseline cases. First, we compare the total test equipment cost of using a number of analog busses with the use of on-chip data converters. Even though our approach is not the first technique that makes use of on-chip data converters for testing [13, 14], a quantitative analysis of test cost helps in justifying the additional hardware for these data converters. Next, we consider this to be the baseline case and compare the test time of the proposed method with the baseline.

For our experimental set-up, we have used three digital SOCs from the ITC'02 SOC test benchmarks, namely p22810, p34392, and p93791, and we have added three analog cores to each SOC. We refer to the mixed signal SOCs as p22810m, p34392m and p93791m, respectively. The analog cores consist of a pair of baseband I-Q transmit path with a bandwidth of 500kHz, and a CODEC audio path with a bandwidth of 50kHz. These analog cores are taken from a commercial baseband cellular phone chip. The set of tests for these three analog cores is given in Table 1. Due to the lack of an accepted analog test generation tool, analog tests are defined manually based on the core specifications. For the I-Q transmit path pair, six distinct specification-based tests are defined. These include the pass-band gain ($G_{pb}$), the cut-off frequency ($f_c$), the attenuation levels at 1MHz and 2MHz ($G_{1MHz}$ and $G_{2MHz}$), the third order input intercept ($IIP_3$), and the DC offset ($V_{off_{DC}}$), and the phase mismatch ($\Phi_{off}$). For the audio CODEC path, the specifications include $G_{pb}$, $f_c$, and the total harmonic distortion ($THD$). With respect to the signal observability

and Nyquist sampling requirements of each test, the resolution of the data converters is set to be 12 bits, and the maximum sampling frequency is 15MHz.

In order to compare the test equipment cost, we make the following assumptions. First, we assume that the digital tester costs 33% less than the mixed-signal tester with all other attributes being equal. This assumption is moderate compared to industrial reports indicating that the mixed-signal tester cost per unit time can be more than twice as much as the digital tester cost [17]. Second, for a fair comparison, we assume that the total pin count allocated for testing stays the same for each experimental case.

Table 2 compares the test time and cost results for the three SOCs and for various available TAM widths. The cost is calculated as the product of test time with the tester cost per unit time and normalized with respect to the baseline case. We make the comparison of test time in terms of the cycles of a 50MHz clock. For each of the three SOCs we consider using 1 or 2 separate analog test busses (1-abus or 2-abus) with a mixed-signal tester, and a 12-bit digital test bus with on-chip data converters and a digital tester (d-bus). As the tests for one analog core cannot be parallelized, there is no advantage of increasing the number of analog test busses beyond 2 in the case of using a mixed-signal tester. In order to highlight the comparison, we normalize the test cost to a baseline case of using a mixed-signal tester. The baseline case for each value of $W$, denoted by 100% refers to the use of either one or two analog test busses (1-abus or 2-abus), whichever yields a smaller testing time. The testing time is normalized with the relative tester cost to obtain the overall test cost.

These experimental results indicate that for smaller SOCs, such as the p22810m, where the analog test time dominates, using two analog test busses and a mixed-signal tester results in a lower cost. As indicated in Section 1, pushing the signal digitization on-chip is advantageous for SOCs with large digital and small analog content. For SOC, such as p34392m and p93791m, it is clear that using on-chip data converters results in appreciable reduction in the overall test cost.

In order evaluate the proposed analog test wrapper and the unified optimization approach, we have compared the test time of using the proposed approach with the test time of a baseline case where only on-chip data converters are used. In the baseline case, a TAM width of 12 bits has to be allocated to analog tests for the duration; the remaining available bits are used for digital TAM optimization. In our approach, the analog test requirements are integrated into a global optimization flow where the minimum bandwidth requirements of each analog test is taken into account, and the DAC and ADC registers are updated in a semi-serial fashion as explained in Section 3.

In Section 2, we reviewed the TAM optimization problem and described a heuristic algorithm to solve it. Since the analog cores are wrapped, we can proceed to solve the TAM optimization problem in a manner identical to that explained in Section 2. We use the *Partition_evaluate* heuristic, to arrive at TAM partitions, and the *Core_assign* heuristic to find near optimal core assignments to TAM partitions.

Table 3 shows a comparison of test time using the proposed analog wrapper and the global optimization algorithm with the test time when only data converters are used. The results are tabulated for a total of five ($B = 5$) and six ($B = 6$) fixed-width TAMs. As

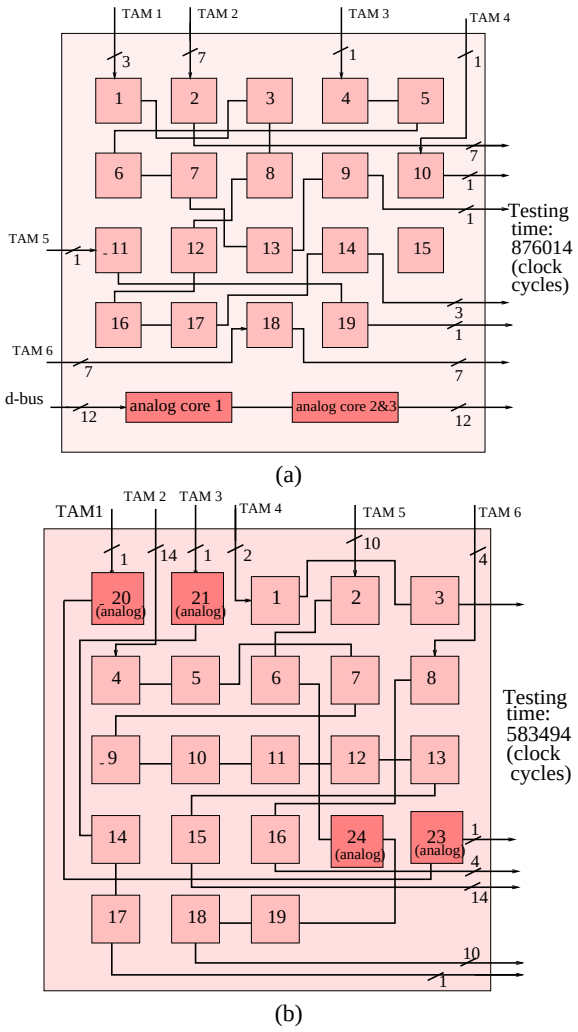


**Figure 3.** Core/TAM assignments in p34392 for $W$ = 32 (a) using digitized approach, (b) using proposed approach.

can be seen in Table 3, the testing time is lower when the digital and analog cores are provided as inputs to the unified optimization procedure. The decrease in testing time is especially significant for small values of TAM width $W$. The TAM width requirements of the analog cores are much smaller in comparison to the TAM width requirements of the digital cores. Most analog core tests do not require a TAM width greater than four. Note that the decrease in testing time is an added advantage on top of the test cost reduction achieved due to the elimination of the expensive mixed signal tester.

In Figure 3, the core assignments for the 19 digital cores of the SOC p34392 and the 3 analog cores is shown. It highlights the differences in the test schedules and the test access architectures for the two scenarios, corresponding to using only on-chip data converters and using the proposed approach. It can be easily seen that in the digitized approach, the digital cores can use only 20 of the 32 top level TAM wires, whereas in the global optimization approach, the analog tests need not be scheduled on a separate digital bus. In Figure 3, the "blocks" numbered 20, 21 and 23 cor-

| | SOC p22810m | | | SOC p34392m | | | SOC p93791m | | |
|---|---|---|---|---|---|---|---|---|---|
| TAM width $W$ (bits) | 1-abus | 2-abus | d-bus | 1-abus | 2-abus | d-bus | 1-abus | 2-abus | d-bus |
| 24 | 571823 | 454282 (100%) | 600940 (88%) | 876014 (100%) | 1033209 | 1566081 (119%) | 1415649 (100%) | 1865474 | 2381317 (112%) |
| 32 | 571723 | 299785 (100%) | 571723 (127%) | 584524 (100%) | 663193 | 876014 (100%) | 1008643 (100%) | 1244785 | 1415649 (94%) |
| 40 | 571723 | 299785 (100%) | 571723 (127%) | 583494 (100%) | 583494 | 584524 (67%) | 803188 (100%) | 934369 | 1008643 (84%) |
| 48 | 571723 | 299785 (100%) | 571723 (127%) | 571723 | 544579 (100%) | 583494 (71%) | 639689 (100%) | 702075 | 803188 (84%) |
| 56 | 571723 | 299785 (100%) | 571723 (127%) | 571723 | 544579 (100%) | 571723 (70%) | 571723 (100%) | 609494 | 639989 (75%) |
| 64 | 571723 | 299785 (100%) | 571723 (127%) | 571723 | 544579 (100%) | 571723 (70.0%) | 571723 | 518058 (100%) | 571723 (73%) |

**Table 2.** Comparison of test time (in clock cycles) in using analog versus digital bus. The normalized test cost, including the test equipment cost, is shown in parenthesis.

| | Number of TAMs $B = 5$ | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | p22810m | | | p34392m | | | p93791m | | |
| TAM width ($W$) | Proposed approach | Digitized approach | Improvement (percent) | Proposed approach | Digitized approach | Improvement (percent) | Proposed approach | Digitized approach | Improvement (percent) |
| 24 | 348803 | 571723 | 38.9 | 663193 | 1292071 | 48.7 | 1247493 | 2409601 | 48.2 |
| 32 | 278641 | 571723 | 51.3 | 583494 | 876014 | 33.4 | 955346 | 1438121 | 33.5 |
| 40 | 236997 | 571723 | 58.5 | 544579 | 584524 | 6.8 | 791408 | 996651 | 20.5 |
| 48 | 214585 | 571723 | 62.5 | 544579 | 583494 | 6.6 | 672450 | 796375 | 12.4 |
| 56 | 199820 | 571723 | 65.1 | 544579 | 571723 | 4.7 | 593599 | 639079 | 7.1 |
| 64 | 193081 | 571723 | 66.2 | 544579 | 571723 | 4.7 | 520059 | 571723 | 9.0 |
| | Number of TAMs $B = 6$ | | | | | | | | |
| 24 | 535807 | 600940 | 10.83 | 663193 | 1566081 | 57.6 | 1358456 | 2381317 | 42.9 |
| 32 | 261613 | 571723 | 54.2 | 583494 | 876014 | 33.4 | 942698 | 1415649 | 33.4 |
| 40 | 226269 | 571723 | 60.4 | 544579 | 584524 | 6.8 | 765449 | 1008643 | 24.1 |
| 48 | 198707 | 571723 | 65.2 | 544579 | 583494 | 6.6 | 651823 | 803188 | 18.8 |
| 56 | 180142 | 571723 | 68.5 | 544579 | 571723 | 4.7 | 571531 | 639989 | 10.7 |
| 64 | 171302 | 571723 | 70.0 | 544579 | 571723 | 4.7 | 511815 | 571723 | 10.5 |

**Table 3.** Testing time (in clock cycles) and percentage improvement using the proposed approach.

respond to tests for I-Q transmit paths and the block numbered 24 corresponds to the test for the audio CODEC analog core. Since, the two cores are wrapped, the proposed architecture allows us to schedule their tests on different TAMs as can be seen in Figure 5 (b). Using the global optimization approach, an improvement of 33.4% is achieved in the testing time.

# 6 Conclusions

We have presented a new approach for reducing the testing time and test cost for mixed-signal SOCs containing both analog and digital cores. The proposed approach is based on the use of a novel test wrapper for analog cores. To the best of our knowledge, this work represents the first attempt to develop a TAM optimization and test scheduling approach that can handle wrapped analog and digital cores in a unified manner at the SOC level. In addition to reducing testing time, the proposed approach obviates the need for expensive mixed-signal testers. We have presented experimental results for three ITC'02 SOC test benchmarks that have been augmented with three analog cores. The results demonstrate that for "big D/small A" SOCs, the testing time and test cost are reduced significantly using the proposed optimization method.

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