A Dual band CMOS VCO with a Balanced Duty Cycle Buffer

Yun Cheol Han, Kwang il Kim, Jun Kim, Kwang Sub Yoon
System LSI Division, Samsung Electronics co., Yongin-City, Gyeonggi-Do, Korea
82-031-209-4105
hanssen@samsung.co.kr

Dept. of Electronic Engineering, Inha University
Yong-Hyun Dong, Nam-Gu, In-chon, Korea
82-032-860-7419
ksyoon@inha.ac.kr

ABSTRACT

This paper proposes a dual band VCO with a standard 0.35 ㎛ CMOS process to generate 1.07GHz and 2.06GHz. The proposed VCO architecture with 50% duty cycle circuit and a half adder(HA) is able to produce a frequency two times higher than that of the conventional VCOs. The measurement results demonstrate that the gain of VCO and power dissipation are 561MHz/V and 14.6mW, respectively. The phase noises of the dual band VCO are measured to be -99.05dBc/Hz and -94.9dBc/Hz at 2MHz offset from 1.07GHz and 2.06GHz.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles - *Advanced technologies, VLSI (very large scale integration)*

General Terms

Measurement

Keywords

Dual band, VCO

1. INTRODUCTION

In recent years, the mobile communication market has been growing rapidly. The rapid growth in the use of wireless communication systems has been met through steady reductions in cost, size, and power consumption.

High-speed, low-power phase-locked loops (PLL's) find wide applications in clock recovery, clock generator and frequency synthesizers. Several critical parameters of the PLL, such as speed, timing jitter, spectral purity, and power dissipation, strongly depend on the performance of the VCO. Recently, a design of the high performance voltage-controlled oscillator (VCO) such as LC-tank VCO [1] and differential ring oscillator has demanded a higher operational frequency and a lower phase noise [2].

The proposed VCO structures are explained in the next section. Section 3. presents simulation and measurement results. Section 4. describes conclusions.

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2. VCO ARCHITECTURE WITH BALANCED DUTY CYCLE

This paper proposes a CMOS VCO circuit based on a differential ring oscillator to produce two frequencies with a balanced duty cycle.

A total phase delay of a four-stage ring oscillator is 180°, thus the phase delay of each one stage becomes 45° [3]. The oscillation frequency from VCO can be given as;

$$f_{osc}=\frac{1}{2\pi \cdot N \cdot R_o \cdot C_o} \quad (1)$$

, where N is a number of the delay cell, R_o is an output resistance of each delay cell inversely proportional to a magnitude of the current, and C_o is a total capacitance at the output node of each delay cell [4]. In Fig. 4, R_o is also expressed as

$$R_o = R_{op} \;//\; R_{on} \quad R_{op} = g_{m2} \cdot r_{o2} \cdot (\frac{1}{g_{mp3}} // r_{o4}) \approx \frac{g_{m2}}{g_{mp3}} \cdot r_{o2}$$

$$R_{on} = \frac{1}{2} g_{m3} \cdot r_{on3}{}^2$$

$$R_0 = \left(\frac{g_{m2}}{g_{mp3}} \cdot r_{o2}\right) // \left(\frac{1}{2} g_{mn3} \cdot r_{on3}{}^2\right) \approx \frac{g_{m2}}{g_{mp3}} \cdot r_{o2} = \sqrt{\frac{\left(\frac{W}{L}\right)_{p2}}{\left(\frac{W}{L}\right)_{p3}}} \cdot r_{o2} \quad (2)$$

, where R_{op} and R_{on} are the output resistances of PMOS and NMOS at the V_{out}+ node. g_{m2}, g_{mp3} and g_{mn3} are the transconductances of M2, Mp3, Mn3. r_{o2}, r_{on3} are the output resistances of M2, Mn3. The output capacitance is described by

$$C_0 = C_{gdp4} + C_{bdp4} + C_{bdp3} + C_{gdn3} + C_{bdn3} + C_{gdn4} + C_{bdn4} \quad (3)$$

, where C_{gdi} is the gate-drain parasitic capacitance, C_{bdi} is the bulk-drain parasitic capacitance.

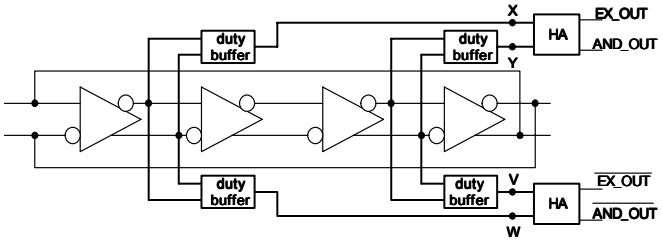

Fig. 1 Circuit diagram of the proposed VCO with an arithmetic functionality

Fig. 1 shows the block diagram of the proposed VCO. The circuit comprises a four-stage ring oscillator, differential to single ended buffers, and half-adder. The phase of the duty cycle balanced

buffer circuit is equivalent to that of each ring stage associated with it.

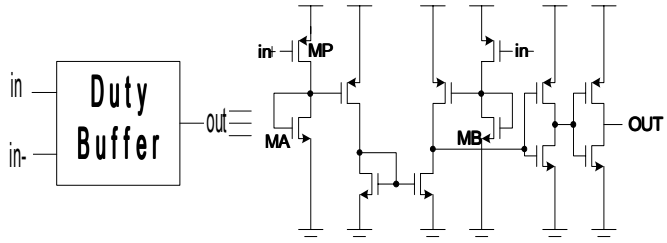

Fig. 2 Circuit schematic of the 50% duty cycle buffer

Duty cycles on the output node of the first ring stage and the third ring stage are not 50% precisely.

The circuit schematic of the differential to single ended buffer circuit is depicted in Fig. 2. It is followed by two inverter stages, which shape up waveforms. It also provides a precise 50% duty cycle through a design of device aspect ratios of transition, MA and MB given by (4) – (8);

Because MP is operated Saturation region,

$$I_{MP} = \frac{K_P\left(\frac{W}{L}\right)_{MP}\left(V_{sgMP} - |V_{tMP}|\right)^2}{2} \tag{4}$$

and the range of IN, Voltage of drain to source

$$\Delta V_{sgMP} = \sqrt{\frac{2\Delta I_{MP}}{K_{MP}\left(\frac{W}{L}\right)_{MP}}} + |V_{tMP}| \tag{5}$$

$$\Delta V_{DS} = \Delta V_{gsMA} = \sqrt{\frac{2\Delta I_{MP}}{K_{MA}\left(\frac{W}{L}\right)_{MB}}} + |V_{tMA}| \tag{6}$$

$$\sqrt{\frac{2\Delta I_{MP}}{K_{MB}\left(\frac{W}{L}\right)_{MB}}} + |V_{tMB}| = \sqrt{\frac{2\Delta I_{MP}}{K_{MA}\left(\frac{W}{L}\right)_{MB}}} + |V_{tMA}| \tag{7}$$

Finally,

$$\left(\frac{W}{L}\right)_{MA} = \frac{K_{MB}}{K_{MA}}\left(\frac{W}{L}\right)_{MB} \tag{8}$$

The half adder circuit (HA), as shown in Fig. 3 enables the proposed VCO to generate two oscillation frequencies of EX-OR gate output and AND gate output.

The phase delay between node X and node Y shown in Fig. 1 is 90^o. As these signals at node X and node Y become high and low, respectively, the output signal of EX-OR gate becomes high. As the signals at node X/Y becomes high/high, it allows the output signal of EX-OR gate to become low. Therefore it results in doubling the output frequency of EX-OR with respect to that at node X and node Y.

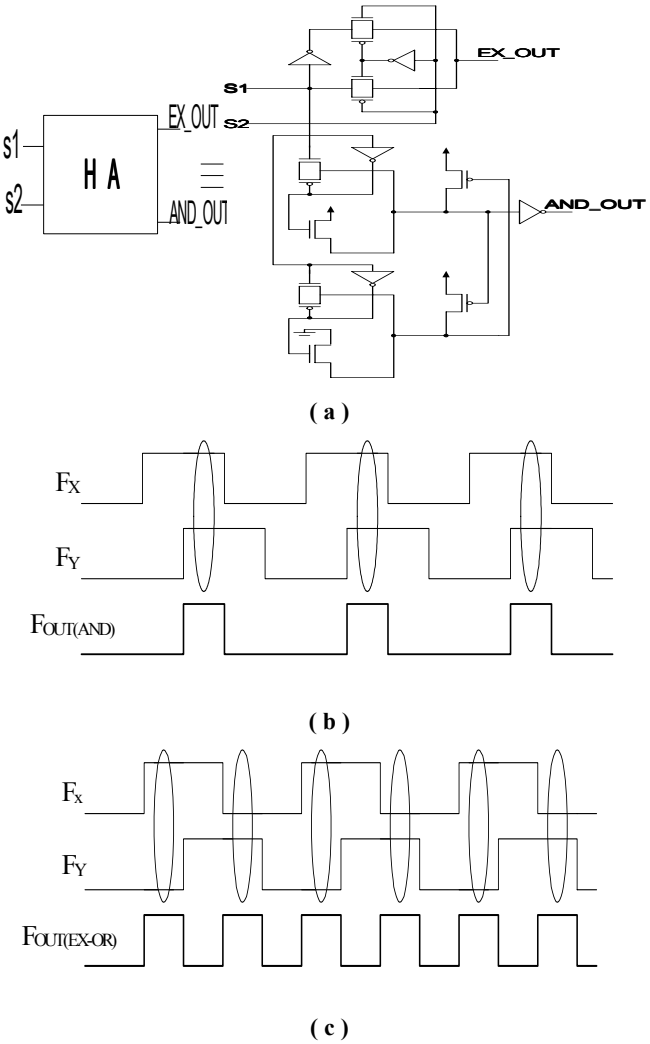

Fig. 3 Diagram of (a) Half Adder circuit (b) signal from AND gate and (c) signal from EX-OR gate of the proposed VCO with an arithmetic functionality

The proposed VCO with Duty cycle balanced Buffer and Half Adder consists of four delay cells whose circuit is shown in Fig. 4.

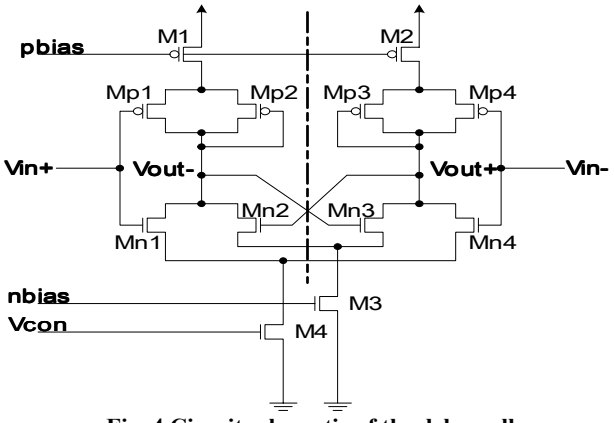

Fig. 4 Circuit schematic of the delay cell

The architecture of the designed differential delay cell is symmetrical with respect to the dotted line. [2] Each half delay cell circuit consists of one inverter (Mp1/Mn1 and Mp4/Mn4) with a latch circuit (Mn2 and Mn3), an active load (Mp2 and Mp3), and bias circuits (M1, M2, M3, M4).

V_{con} is the control voltage to adjust the bias current and consequently, to change the output resistance, R_0. nbias turns on latch circuits(Mn2 and Mn3) and pbias is the output voltage of replica biasing circuits [5]. In equation (1), oscillation frequency, f_{osc} is inversely proportional to R_O. Thus, increasing each device aspect ratio of active loads(Mp2 and Mp3) enhances the oscillation frequency.

3. MEASUREMENT RESULTS

The conventional and proposed VCO are implemented with a 0.35 ㎛ standard CMOS n-well process at a single power supply of 3.3V. The die photo of the proposed CMOS VCO is shown in Fig. 5. The measured voltage gain and power dissipation of the proposed VCO are 561MHz/V and 14.6mW at 2.06GHz, respectively.

Comparison of the measured phase noise between the conventional VCO and the proposed VCO at 2MHz offset from 1.07GHz and 2.06GHz are illustrated in Table 1.

Table 1. Summary of the performance of the proposed VCO

Technology	0.35-㎛ Standard CMOS (2-poly 4-metal)		
Operating Frequency	1.07GHz / V_{CON} = 3.0V (Conventional)	2.06GHz / V_{CON} = 3.0V (Proposed_EX-OR)	1.05GHz / V_{CON} = 3.0V (Proposed_AND)
Phase Noise	-99.05dBc/Hz @2MHz	-94.9dBc/Hz @2MHz	-92.18dBc/Hz @2MHz
Power Dissipation	14.59mW @2.06GHz		
VCO gain	561MHz/V		

Fig. 7 demonstrates that the measured phase noise of the proposed VCO, -92.18dBc/Hz is larger than that of the conventional VCO, -99.05dBc/Hz. However, the phase noise of the proposed VCO at 2.06GHz is measured to be -94.9dBc/Hz. The phase noise of the proposed VCO at 2.06GHz is enhanced in 2.72dBc with respect to the phase noise at 1.05GHz.

Table 2. illustrates the comparison of several VCOs from the literature with the proposed VCO.

Table 2. Performance comparison of the VCO circuits

Year	Process	Power Supply	VCO	Phase Noise	Operating Frequency	Power Dissipation
1998 CICC	0.35 ㎛ CMOS	1.8V	Ring	-72dBc/Hz @150kHz	1.1GHz	3.5 ㎽ (VCO)
1998 VLSI	0.25 ㎛ CMOS	2.5V	Ring	-121dBc/Hz @600kHz	1.8GHz	6 ㎽ (VCO)
1999 JSSC	0.6 ㎛ CMOS	3.0V	Ring	-101dBc/Hz @100kHz	0.75-1.2GHz	30 ㎽ (VCO)
This paper	0.35 ㎛ CMOS	3.3V	Ring	-99.05dBc/Hz @2MHz -94.9dBc/Hz @2MHz -92.18dBc/Hz @2MHz	1.07GHz(con) 2.06GHz(pro_ex) 1.05GHz(pro_and)	14.59 ㎽ (VCO)

The measurement setup is shown in Fig. 6.

4. CONCLUSIONS

A CMOS VCO circuit with a duty cycle balanced buffer and half adder is proposed to be able to generate dual band frequencies (1.05GHz and 2.06GHz) simultaneously. The proposed VCO draws a 14.6mW at 3.3V. The measured phase noise of the dual band VCO are -92.18dBc/Hz and -94.9dBc/Hz at 1.05GHz and 2.06GHz at 2MHz offset. This measured phase noise is assembled onto PCB test circuit.

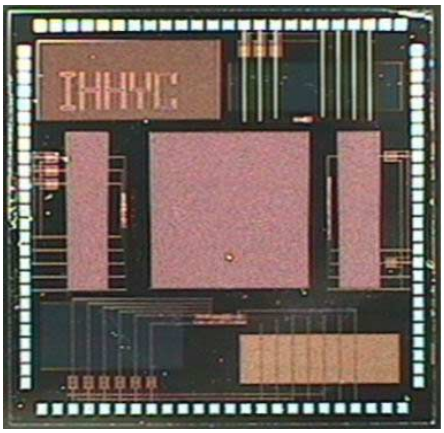

Fig. 5 Die photo of the proposed VCO

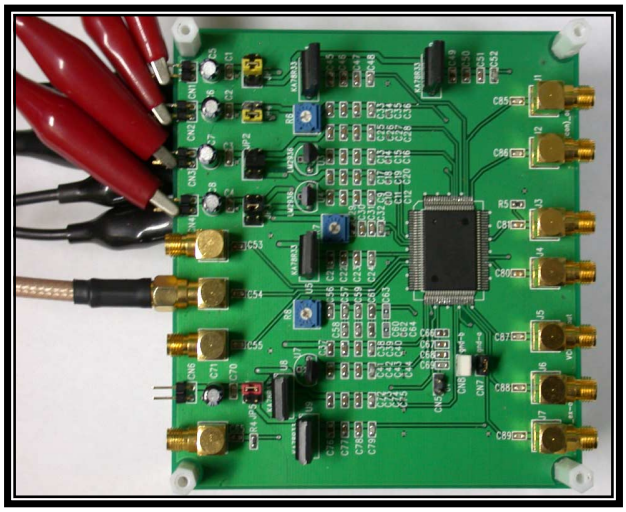

Fig. 6 Measurement setup

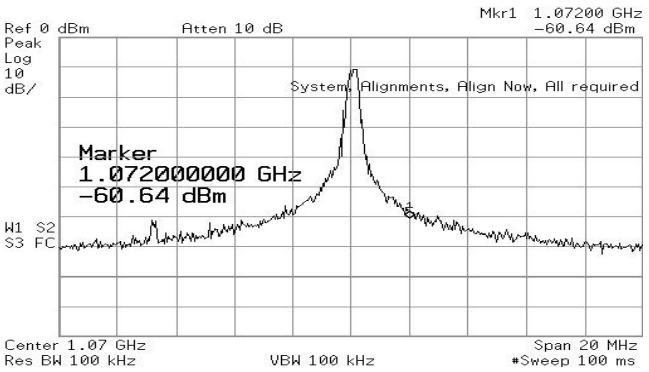

Fig. 7(a)

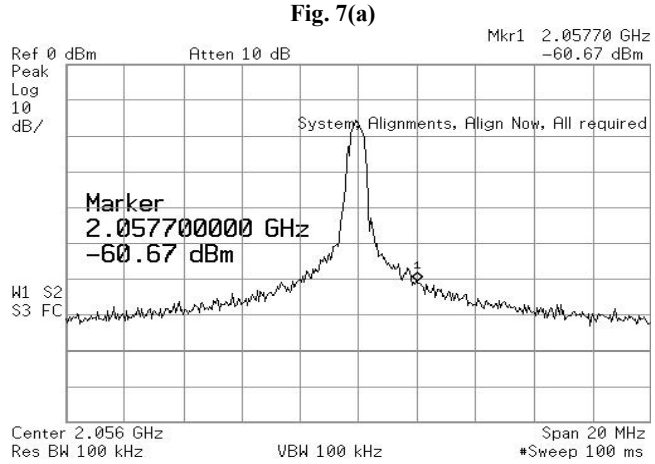

Fig. 7(b)

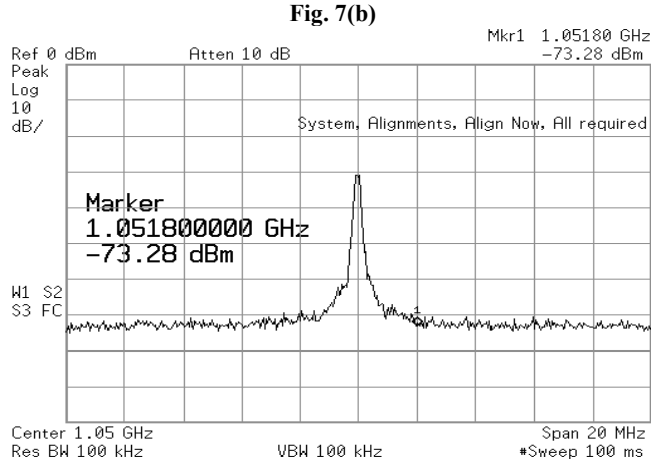

Fig. 7(c)

Fig. 7 The output spectrum plots of the measured VCO

(a) Conventional VCO: center frequency=1.07GHz

(b) Proposed VCO(EX-OR): center frequency=2.06GHz

(c) Proposed VCO(AND): center frequency=1.05GHz.

5. ACKNOWLEDGMENTS

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