Variable Gain Amplifier with Offset Cancellation

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ABSTRACT

In this paper, the design of variable gain amplifier (VGA) for wireless receiver applications is presented. The VGA uses ac coupling (highpass filter) for dc offset rejection, while each VGA stage is designed to have constant output offset to overcome the slow response of the highpass filter. Due to the architecture chosen, The VGA has a fairly constant bandwidth in the entire gain range, and therefore it has constant settling time. It has been simulated and laid out using IBM SiGe BiCMOS $0.25\mu m$ process. The VGA is OpAmp-R based and has gain range of $-4 \rightarrow 64dB$ with 2dB steps. It has about 35MHz bandwidth and consumes 1.5mA from $2.5V$ supply.

Categories and Subject Descriptors

A.m [**General Literature**]: Miscellaneous

General Terms

Design

Keywords

Variable gain amplifiers, offset cancellation

1. INTRODUCTION

Throughput is one of the main parameters in any wireless communication system. In order to increase throughput, minimum possible overhead should be used while maintaining the robustness of the wireless connection. One of many ways, is to reduce the time required for the receiver to be ready to receive and decode information. If the receiver has no prior information regarding the incoming signal level, it has to figure it out by itself when it receives the first bits of the incoming stream and then adapts itself as fast as possible to receive and decode the information. The overall receiver gain is adjusted, depending on the signal level, to keep almost constant signal level at the ADC input through the VGA [1-5]. The most important factor that determines the response time of the receiver is the settling time of its VGA, which is inversely proportional to the VGA bandwidth. A number of wideband VGA designs can be found in the literature [2, 5]. The problem becomes even more difficult for direct-conversion receivers where the dc offset due to mismatches is a serious issue. In general, the output dc offset of a VGA depends on its gain, and therefore, has to be corrected each time the VGA gain is changed. Another requirement in the VGA is to have constant bandwidth (and therefore, constant settling time) versus gain. In this paper, a $-4 \rightarrow 64dB$ VGA is presented with 2dB gain steps, dc offset cancellation and constant bandwidth. The design is simulated using IBM SiGe BiCMOS $0.25\mu m$ technology. The VGA is intended to be used in a multi-standard Bluetooth/802.11b receiver. The BiCMOS process is used to save power consumption in the receiver. However, the VGA design has been done using only CMOS transistors which means that it can also be implemented in a CMOS process.

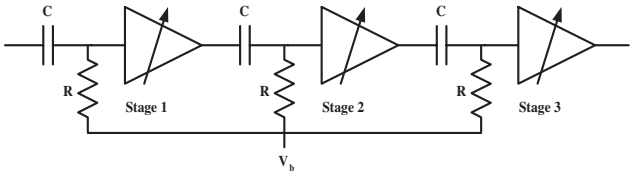

Figure 1: DC offset correction using passive HPF

Since the maximum gain of the VGA is $64dB$, a 3-stage VGA is used with about $20dB$ gain/stage. The VGA is used in a direct conversion receiver, and therefore, dc offset generated by mismatches in the baseband blocks (including the VGA itself) may saturate the stages of the VGA unless this offset is cancelled before it gets amplified by the VGA stages. The dc offset can be cancelled between VGA stages by using simple RC highpass filters with low cutoff frequency ($< 10kHz$ is used in this design, but it depends on the signal spectrum in the wireless application) as in Fig. 1 to avoid losing significant part of the signal spectrum. This solution will only work if the dc offset remains constant while the signal is being received. However, since the gain of the VGA is adjusted during the preamble period, the output offset of each VGA stage may change if its gain is altered. This is because the capacitor in the HPF takes time (which is inversely proportional to the HPF bandwidth) to charge/discharge to the new offset value.

2. SOLUTIONS FOR SLOW HPF RESPONSE

The proposed solution to the slow response of the HPF to dc offset variations is to design the VGA stages such that its

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output referred offset is constant regardless of its gain setting. To illustrate how to design such a VGA, consider first the OpAmp-R based VGA shown Fig. 2(a). Single ended topology is shown for simplicity. Differential architecture is used in all VGA stages. The OpAmp input referred offset is represented by the voltage source V_{OS} at the non-inverting terminal. The gain of the VGA stage is controlled by the digital bit d_1. The output of the VGA in Fig. 2(a) is given by:

$$V_{out} = -\frac{G_{11}+d_1G_{12}}{G_2}V_{in} + (1+\frac{G_{11}+d_1G_{12}}{G_2})V_{OS} \quad (1)$$

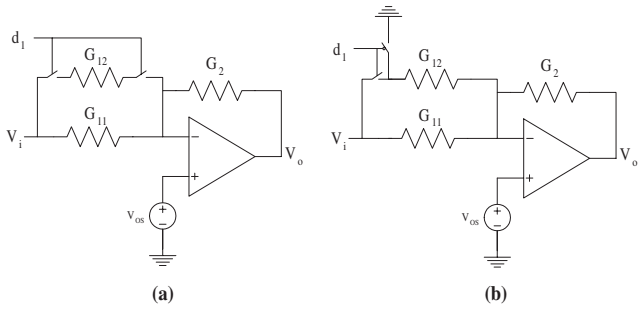

Figure 2: (a)Conventional OpAmp-R VGA (b)Proposed constant-offset VGA circuit

Note that the second term in the above equation, which represents the output referred offset, depends on the digital control input d_1. Therefore, the output dc offset of this VGA circuit depends on its gain. To keep the output dc offset independent of gain, the VGA stage shown in Fig. 2(b) is proposed. The output voltage of the modified VGA stage is expressed as:

$$V_{out} = -\frac{G_{11}+d_1G_{12}}{G_2}V_{in} + (1+\frac{G_{11}+G_{12}}{G_2})V_{OS} \quad (2)$$

In this case, the resistor G_{12} is always included in the feedback loop and therefore, the output referred offset is constant as indicated in equation (2). The gain is changed by switching only the input terminal of the resistor G_{12} to the input or to ac ground. Note that the output dc offset is constant only if the offset from the previous stage is completely rejected.

The circuit in Fig. 2(b) has constant feedback factor regardless of its gain. This means that the bandwidth of the VGA will be independent of its gain. This is a very important property in a VGA design. The main drawback in this circuit is its finite input resistance which is also variable. Since each VGA stage is preceded by a passive HPF that uses large resistance and capacitance values to achieve the required low cut-off frequency, the output of this passive HPF has to be buffered before it's applied to the VGA input. The buffer is implemented using a source follower with reduced output resistance (to be discussed later) and therefore can generate its own offset that will be multiplied by the variable gain of the VGA and produce a variable offset at the VGA output. To circumvent this problem, a separate buffer is used for each resistor in the bank of resistors at the VGA input and the gain is controlled by the switching the input of the buffer, not the output as shown in Fig. 3. Therefore the buffer offset is always included in the circuit and the VGA output offset is kept constant.

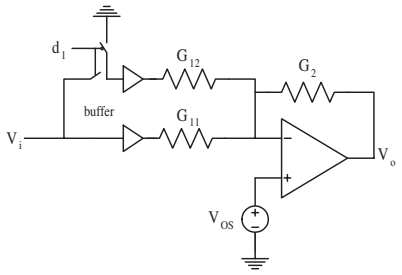

Figure 3: Proposed constant-offset VGA circuit using OpAmp-R and passive HPF

3. OPAMP AND BUFFER DESIGNS

To achieve a gain of about $20dB$ in a VGA stage, a 3-stage OpAmp architecture has been chosen, as shown in Fig. 4. The input and output common mode voltages are set to $1.5V$. Simulations showed that the OpAmp dc gain is more than 70dB and the phase margin is more than 60^o at $20dB$ gain. The 3rd stage of the OpAmp is the buffer stage, which drives only the feedback resistor G_2 as shown in Fig. 3, and the resistors R_{CM} used to sense the common mode output of the OpAmp in the common mode feedback (CMFB) circuit (Fig. 5). The compensation capacitor C_C is used to stabilize the differential mode (DM) and common mode (CM) loops. Although the OpAmp is always used in a high DM gain configuration, the CM loop uses unity gain and its stability has to be enhanced by adding a degeneration resistor R_{CMFB} in the CMFB transconductor shown in Fig. 5. It's also worth to emphasize the advantage of using the configuration in Fig. 2(b) that the feedback factor is always constant and therefore, the OpAmp will have the same phase margin for all gain settings. This allows us to use fixed compensation capacitor while keeping the OpAmp bandwidth constant for all VGA gains. The buffers though,

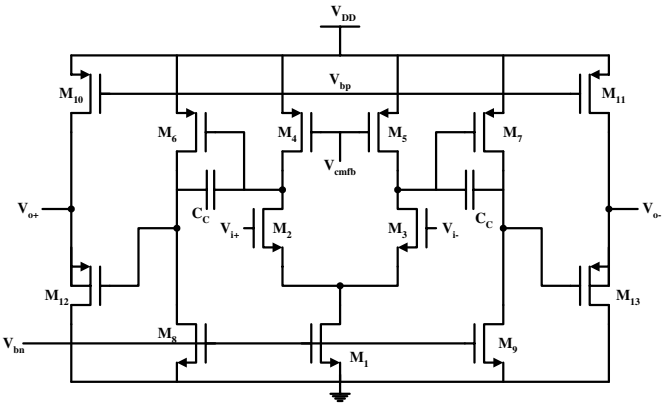

Figure 4: 3-stage OpAmp schematic

have to drive the input resistors of the VGA stage which are smaller or equal to the feedback resistor. Since inter-stage HPF's are used, the input CM voltage of the buffers doesn't have to be the same as the output CM voltage, and therefore simpler buffers with dc level shift can be used. To improve linearity and gain accuracy, a buffer with reduced output resistance, as shown in Fig. 6, is used. The low frequency output resistance of the buffer is approximately given by:

$$R_{out} \approx \frac{g_{d1}+g_{d3}}{g_{m2}g_{m3}} \quad (3)$$

Where g_{mi} and g_{di} are the small signal transconductance and output conductance of the transistor M_i.

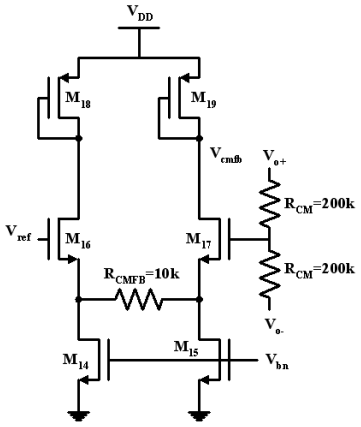

Figure 5: CMFB circuit

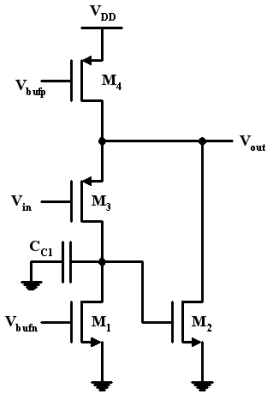

Figure 6: The buffer circuit

4. VGA GAIN LINEUP

The VGA gain has been distributed among the 3 stages such that all the stages have almost the same maximum gain (about $20dB$ gain/stage). In the first stage, the gain can be either 0 or 20dB. Fine gain control is achieved through the second and third stages. The third stage has 5 possible gain settings from 0 to 24dB with 6dB gain steps. The second stage has 6 possible gain settings which are -4, -2, 0, 16, 18, 20dB. This gain control distribution allows the overall VGA gain to be controlled from -4 to 64dB with 2dB steps. The gain control is distributed such that the number of gain steps/stage is reduced to avoid the design complexity in each stage. 6dB steps are used in the last stage to allow using R2R ladder network for gain control as will be discussed later. The following sections describe the design of the VGA stages.

4.1 First stage design

The first stage of the VGA has the most stringent requirements in terms of noise and linearity. This is because the noise of this stage is multiplied by the gain of the other two stages. On the other hand, the minimum gain for this stage is 0dB, which means that the signal can be at full scale voltage ($1V_p$). The first stage VGA circuit is similar to the circuit shown in Fig 3 with $G_2 = G_{11} = G_{12}/9 = \frac{1}{50k}$. Again, single-ended topology is shown for simplicity. The gain of the first stage is $0dB$ when $d_1 = 0$ and $20dB$ when $d_1 = 1$.

Table 1: 2nd stage VGA gain settings

G_2 in dB	d_2	d_3	d_4	d_5	d_6
-4	0	0	0	0	0
-2	0	1	0	0	0
0	1	1	0	0	0
16	0	0	0	0	1
18	0	1	0	1	1
20	1	1	1	1	1

4.2 Second stage design

The second stage of the VGA has more relaxed noise requirements than its first stage. Therefore, in order to reduce the power consumption in the OpAmp, the input and feedback resistors are scaled up to reduce the loading on the OpAmp. To have about the same circuit bandwidth, all the transistors sizes as well as dc currents are scaled down by the same factor. Therefore, the power consumption of the second stage is lower than that of the first stage by the same factor. Since the resistors values in the first stage are already high ($50k\Omega$), the resistor values in the second stage cannot be increased much higher because of area limitation. Fig. 7 shows the second stage VGA circuit. The gain of the second stage is controlled with the digital inputs d_2 to d_5. Gain values and the corresponding digital inputs are listed in the table 1.

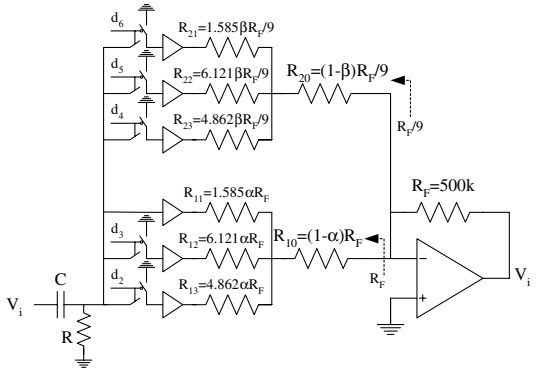

Figure 7: Second stage VGA circuit

The values of R_{i1}, R_{i2}, and R_{i3} (where i=1,2) are chosen such that:

$$20log(\frac{R_{i1}}{R_{i1}+R_{i2}+R_{i3}}) = -4dB \quad (4)$$

$$20log(\frac{R_{i1}+R_{i2}}{R_{i1}+R_{i2}+R_{i3}}) = -2dB \quad (5)$$

The parameters α and β in Fig. 7 are used to scale the input resistance seen by the buffers. Note that the equivalent resistance of the resistors R_{1i} $(i = 0, \cdots, 3)$ is equal to R_F and is independent of the value of α. Similarly, the equivalent resistance of the resistors R_{2i} $(i = 0, \cdots, 3)$ is equal to $R_F/9$ and is independent of β. The lower the values of α and β, the lower the total resistance area, and the higher the

Table 2: 3rd stage VGA gain settings

G_3 in dB	d_7	d_8	d_9	d_{10}	d_{11}
0	0	0	0	1	0
6	0	0	1	0	0
12	0	1	0	0	0
18	1	0	0	0	0
24	1	1	1	1	1

required driving capability in the buffers, and therefore the higher the current drain. This is an example of power-area trade-off in this design. Note that in order to have positive resistance values, α and β are positive numbers less than 1.

4.3 Third stage design

The third stage of the VGA is designed to have $6dB$ gain steps from $0dB$ to $24dB$. Therefore, a resistive ladder network can be used at the input to realize the required gains. Fig. 8 shows the third stage VGA circuit. Gain values and the corresponding digital inputs are listed in the table 2.

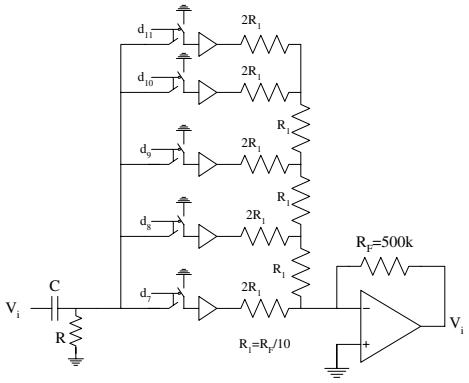

Figure 8: Third stage VGA circuit

5. SIMULATION RESULTS

Since there are 35 VGA gain settings in the $-4 \rightarrow 64dB$ gain range, 6 control bits are needed to control the gain. A decoder should be built to decode the gain control bits into the d_i $(i = 1, \cdots, 11)$ bits required for the switches in the VGA stages. One bit control is saved by using only the gain range $0 \rightarrow 62dB$. Therefore, only 5 control bits are used in simulations. The proposed design has been simulated using Spectre. The layout in $0.25\mu m$ process occupies $0.7mm \times 0.5mm$. Post-layout simulations show that the VGA bandwidth varies from $33MHz$ to $36MHz$ in the entire gain range. The input referred noise density is $26nV/\sqrt{Hz}$ at maximum gain and the output $1dB$ compression point is more than $15dBV$. The VGA consumes $1.5mA$ from $2.5V$ supply. Fig. 9 shows the gain of the VGA (in dB) versus the digital control word. Fig. 10 shows the $1dB$ compression curve for the maximum (62dB) and minimum (0dB) gains of the VGA.

6. CONCLUSIONS

A variable gain amplifier with offset cancellation and fast settling time is presented. The amplifier is suitable for wireless applications with short preamble time where the VGA has to settle within short time. Inter-stage low cut-off HPF's are used in combination with constant output offset VGA

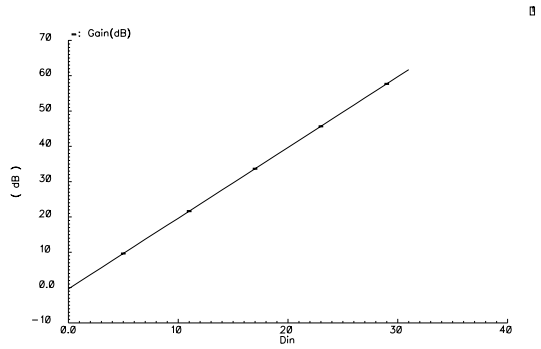

Figure 9: The gain (in dB) of the VGA versus the input digital word

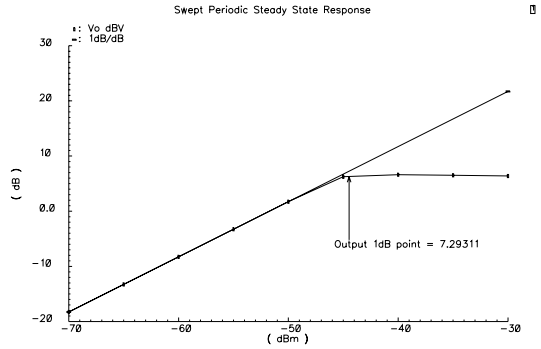

Figure 10: 1dB compression curves for maximum and minimum gains

stages to build the proposed VGA. The use of constant-output-offset VGA stages helps to overcome the sluggish response of the HPF.

7. ACKNOWLEDGMENTS

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8. REFERENCES

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