RF CMOS Circuit Optimizing Procedure and Synthesis Tool

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ABSTRACT

In this paper, we discuss a methodology to design and synthesize analog CMOS components such as RF amplifiers. The inputs of the synthesis tool are the circuit specifications described at high-level of abstraction, fabrication dependent technology parameters and un-sized circuit topologies. The output is a sized net list, which meets the user constraints.

The synthesis environment considers user-defined performance parameters into account, and it relies on a genetic algorithm based heuristic method to search for a solution in a large design-space. The synthesis tool determines a solution set of design parameters such that the circuit satisfies the overall design constraints.

Categories and Subject Descriptors

B.6.3 [**Logic Design**]: Design Aids – *automatic synthesis, simulation.*

B.7.3 [**Integrated Circuits**]: Types and Design Styles – *standard cells, VLSI.*

General Terms: Algorithms, Performance, Design.

Keywords: CAD, RF, analog, genetic algorithm, electronics.

1. INTRODUCTION

The constantly growing market for wireless communication devices such as cellular phones, pagers and global positioning system receivers (GPS) is moving the industry towards integrating whole systems into single-chip solutions. Conventional wireless architectures consist of a front-end section and a back-end section. The front-end section processes analog signals in the radio frequency (RF) range, while the back-end processes analog and digital signals in a base band low frequency range [1]. Although RF components constitute a very small fraction of the whole system, the design time and cost of analog blocks are relatively higher than the base band counterparts. This is mainly due to the fact that systematic design methodologies for analog components are still in their infancy. Compared to digital and low frequency mixed-signal circuits, designers of analog circuit are lacking the support of design automation tools.

Besides, circuits operating at high frequencies are susceptible to noise and distortion effects, which increase the analysis and design complexities of such devices. Time-to-market and the increasing complexity of these systems are urging for developing new design methodologies to speed up the design process and make it more tractable. The use of computer-aided analysis and synthesis tools for analog, digital and RF integrated circuits are therefore required.

The design automation of analog and mixed-signal CMOS circuits has recently received increased attention from the research community [2][3][4][5]. However, most of the work has been limited to base band applications. RF experts are still designing radio frequency electronics. High quality RF devices under existing technologies are designed by try-and-error procedures [6]. Therefore, it is clear that CAD tools for synthesis of RF circuitry must be developed to deal with the complexity of RF electronics and with the requirement for rapid design times.

In this paper, we describe a methodology to analyze the performance trade-offs, and present a synthesis environment for CMOS electronics considering both the low and high frequency constraints. The specifications depend on the application and the chosen system topology. Some specifications are performance parameters such as distortion, noise, gain, frequency of operation, silicon area and power consumption of analog and RF circuits. Analog circuits become obsolete very fast. A net list of circuits can cover a large domain of applications. In order to reduce the time and cost of development of analog circuits, analog standard cell libraries have been used [7]. Building blocks are stored in the form of entries of net lists. The problem with the analog domain is that it is difficult to configure a rich enough set of library cells for the wide spectrum of possible applications. Performance specifications for analog building blocks are much more complicated than those for digital blocks.

A combination of knowledge-based and optimization-based approach is used in the design methodology. Circuit performance estimations are hard-coded for the low-level circuit components, while a genetic algorithm is used to search different solutions at the system level.

The tool maintains a dynamic library of topologies for various sub-circuits. When a component is needed, first a correspondent sub-circuit that meets the design constraints is search in the library. If the circuit is found, no new components are generated; only new components are generated if the no library component meets the specifications. All new topologies are constantly added to the library.

In the following sections we will preset related work and the overview of design methodology. Then, experimental results are presented to show the effectiveness of the tool. Finally, the limitations and further scope for development will be discussed.

2. RELATED WORK

This work was derived from previous works in design automation of analog and mixed-signal circuits such as IDAC [8], OPASYN

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[9], STAIC [10], OASYS [11], DONALD [12], OPTIMAN [13] and SRFCC [14]. These tools can be categorized into knowledge-based or optimization-based analog sizing approaches. Knowledge-based systems use heuristic and encode circuit knowledge from analog designers to obtain a solution. Optimization-based approaches use numerical optimization techniques to implicitly to solve for the degrees of freedom in analog design while optimizing the performance of the circuit under the given specification constraints.

3. RF DESIGN CONSTRAINTS

The design of RF electronics involves a trade-off of several performance parameters such as linearity, power, noise, frequency of operation, power supply, and gain. In contrast, synthesis tools for low frequency analog circuits usually ignore the nonlinearity and noise effects because the degradation produced is insignificant at low frequencies. The analysis of nonlinearity and noise in RF circuits typically require simulation tools for spectral domain, which are computationally expensive.

Gain Compression. In nonlinear systems, the higher order harmonics can compress or saturate the circuit gain. The 1-dB compression point typically measures this effect, called gain compression. The 1-dB compression point is defined as the amplitude of the input signal that causes the small-signal gain to drop 1 dB with respect of the ideal linear system [15].

Inter-modulation. Inter-modulation is the effect generated by mixing two signals at different frequencies due to the multiplication produced by the nonlinear system. The inter-modulation effect corrupts the transmitted/received signals when a generated mixed-frequency signal of two nearby strong interfere signals lies in the operating bandwidth. The inter-modulation is typically measured by the input third-order intercept point (IIP3). IIP3 measures the corruption in the received signal due to the inter-modulation produced by two close in frequency interfere signals [16].

Noise. The presence of electrical noise in RF devices in general limits the ability to respond to lower levels of signal amplitudes [16]. Hence, RF synthesis tools should try to minimize the effects of all sources of noise. Several researchers have investigated the fundamental sources of noise in CMOS circuits [17]. Thermal noise, shot noise, and flicker noise are the most common known sources of noise. However, RF systems are mainly concerned with thermal noise.

4. DESIGN OVERVIEW

We begin by outlining the common approaches for automatically synthesize analog integrated circuits developed by different researchers. Then, we describe the general components of the proposed methodology. The presented methodology has many similarities to typical optimization-based analog circuit synthesis tools; our methodology has been targeted to analog components and RF circuits.

Each stage has a number of possible topologies and the user has to select a topology for each stage. Each sub-block will need some performance parameters from the user and the topology to be used. The program will start from an initial point to optimize each sub-block for the parameters given. This is done using the equations that are built into the program. The accuracy of the output is no way related to the accuracy of the equations.

However as the topology changes the equations required for calculating the sizes also change and so new equations have to written in place of the old ones i.e. the library needs to be constantly updated in order to give results close to the correct value.

The tool cannot completely rely on the equations, as it is humanly impossible to keep updating the library as the equations may sometimes take weeks or sometimes months to be written accurately. Hence some basic equations are written to determine approximately the range of the sizes. Using those values the sizes are calculated for the transistors. Then the sizes meeting the specifications are iteratively determined. Once the window is determined the range is given to a genetic algorithm, which searches for different values and forms the net list for the required sub-circuit.

5. SYNTHESIS STRATEGY

As mentioned in previous sections, the design of RF circuits involves a trade-off of several performance parameters. Optimal solutions for an individual performance parameter in general yield to worst-case scenarios for whole systems. On the other hand, optimal solutions involving several design constraints are hard to achieve, and currently much of the effort is based on experience [6]. Also, as the design solution space increases exponentially with the size of the circuit and design parameters, the circuits become hard to be analyzed in a closed analytical form. These factors motivate us to use a heuristic optimization-based approach.

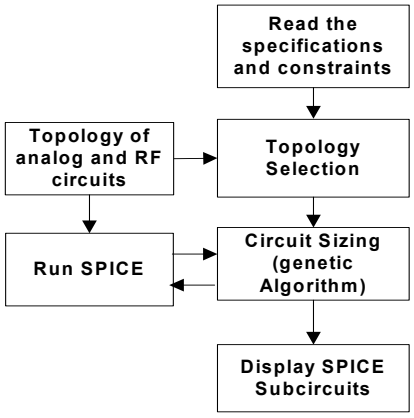

Figure 1. Overview of the tool

Figure1 depicts the block diagram of the synthesis methodology presented in this paper. The circuit specifications and a set of user constraints are the inputs to the synthesis environment. The synthesis process starts by selecting a circuit topology from the library of RF circuit blocks according to the circuit specifications. Then, an optimization-based process sizes the selected topology. The analog and RF performance is verified by spice and is integrated within an overall optimization loop. The optimization tool determines a solution set of design parameters such that the RF circuit satisfies the overall circuit constraints. The performance of the given topology for the specified input condition set is evaluated during each iteration for different design parameters with the spice tool.

5.1 Circuit Sizing:

After a topology has been selected, the circuit sizing starts. We have adopted a synthesis by optimization using a genetic algorithm technique. The optimization method is based on a performance estimation tool for analog and RF circuits embedded in a GA [18] searching tool. The task of the GA is to find a solution for all design parameters such that: (1) all design parameters are lying within the circuit domain space, and (2) all performance constraints are met. The sizing methodology presented in this paper is focused in finding a solution in reasonable time rather than an impracticable optimal solution.

The cost function to be minimized is:

$$1/W_{total} * \sum_{i=1}^{N} Wi * Fi \quad (6)$$

where N represents the number of design parameters, Wi is the weight associated with the performance specification, Wtotal the total weight of all performance specifications, and Fi is defined as follows:

Fi = 0, *if Pi_est satisfies Pi_constraint* (7a)

Fi=‖(Pi_est-Pi_constraint)/Pi_constraint‖, *Otherwise* (7b)

Pi_est is the value for the performance parameter in the current solution, and Pi_constraint is the user specified constraint on that performance parameter. Such a cost function is typical of GAs that handles multiple constraints. The performance parameters are evaluated using the analog and RF performance estimator described in previous section.

The sizing methodology starts by defining a solution representation, and GA tuning parameters. First, a single solution representation of the problem is defined in a data structure, which will be used in the GA optimization loop. The chromosome consists of a set of design parameter values and design domain spaces. The speed of convergence and quality of finally results are dependent of these GA parameters. Therefore, a tuning process is required to meet the design expectations.

5.2 GENETIC ALGORITHM:

In order to use a genetic algorithm [19][20] to solve an optimization problem, it must be possible to represent a single solution to the problem in a single data structure. The algorithm will create a population of solutions based on the sample data structure given. When properly implemented, this algorithm is capable of both exploration (broad-search) as well as exploitation (local-search) of the search space.

The genetic algorithm will decide which individual should survive to the next generation, which ones should reproduce and which ones should die. Typically such an algorithm has no stopping criteria. The user must specify when to stop. Often the number-of-generations is used as a stopping measure, but goodness-of-best-solution, convergence-of-population, or any problem-specific criterion mate individuals to produce offspring can also be used.

Hence, the mechanism of a genetic algorithm can be stated as follows:

- Maintain a population of solutions coded as artificial chromosomes
- Select the better solutions for the recombination (crossover) of the mating chromosomes
- Perform mutation and other variation operators on the chromosomes
- Use these offspring to replace the poorer solutions or create a new generation altogether

Theory and empirical results demonstrate that these algorithms lead to improved solutions in many problem domains. A well-designed algorithm can be guaranteed to solve a broad class of provably hard problems quickly, reliably and accurately.

Many different fields in research are benefiting from this approach. Problems such as jet engine design, analog and logic electronic circuit synthesis, control system synthesis, image processing and automated programming have been successfully tackled.

6. EXPERIMENTAL RESULTS

We estimated several low noise amplifiers to verify the accuracy and speed of the nonlinearity estimation technique. We synthesized the circuits using the HP0.5mm fabrication process parameters. Table 1 and Table 2 present the synthesis and simulation results of all RF circuit design examples. From the results, it should be noted that the synthesis tool tries to match as close as possible all the design constraints rather than optimizing some of the constraints.

The total average estimation error considering the third intercept point IIP3, frequency of operation F0, and amplifier gain at the frequency of operation was 6.12. Specifically, the IIP3 estimation error was 8.0%, the F0 estimation error was 2.7%, and the Gain F0 estimation error was 7.7%.

Table 1. Synthesis results for the Low Noise Amplifier circuit

Ckt	Synthesis Results						CPU
	BW (MHz)	Go (dB)	Z_{in} (ohms)	Power (mwatts)	IIP3 (dB)	NF	Time (Sec)
1	912	22	42	6.8	6.2	1.7	133
2	950	22	46	5.1	6.3	1.5	121
3	1215	22	40	4.7	6.3	1.5	136
4	1261	20	44	4.5	7.3	1.8	159
5	1514	15	148	1.8	5.9	1.1	202

Table 2. Simulation results for the Low Noise Amplifier circuit

Ckt	Simulation Results					
	BW (MHz)	Go (dB)	Z_{in} (ohms)	Power (mwatts)	IIP3 (dB)	NF
1	917	20	47	6.4	6.8	1.1
2	931	21	50	2.0	7.0	1.1
3	1222	22	44	4.3	6.9	1.1
4	1257	20	40	4.7	7.6	1.1
5	1491	15	155	1.7	5.3	1.1

Also, to demonstrate the effectiveness of the presented estimation techniques and synthesis tool for radio frequency circuits, we designed several LNAs, mixers and oscillators. Three different fabrication process parameters form MOSIS were used during the

simulations: HP 0.35microns, HP 0.5microns, and HP 0.8microns.

7. CONCLUSION

We recognize that a standard cell approach is not the optimal way for analog ASIC design. A study of the latest tools will reveal that research has now moved towards optimization-based approach from the knowledge-based approach. More and more tools are trying to capture the knowledge of the designer within the system to make it into a smart tool.

We have presented a methodology to synthesis radio frequency devices considering low frequency and high frequency performance parameters. The synthesis tool relies on a hierarchical analog performance estimator that has been integrated within an overall optimization loop. The optimization loop is used to determine a solution set of design parameters such that the RF circuit satisfies the overall circuit constraints. A prototype system has been implemented to automatically synthesize RF circuits from performance specifications and fabrication process parameters. Several configurations of low noise amplifiers, mixers and oscillators for different fabrication process parameters were synthesized and verified to prove the accuracy and speed of the tool.

In developing this tool, we have gained some insight into the thought process that goes into making a CAD tool. This exposure gives us an idea on where the major development in this area is taking place and what are all the possible alternatives being explored.

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