TEM-Cell and Surface Scan to Identify the Electromagnetic Emission of Integrated Circuits

Timm Ostermann
Institute for Integrated Circuits
University of Linz
Altenberger Str. 69
+43 732 2468 7119
oster@riic.at

Bernd Deutschmann
austriamicrosystems AG
Schloss Premstaetten
+43 3136 500 5971
bernd.deutschmann@
austriamicrosystems.com

ABSTRACT
The characterization as well as the control of the electromagnetic emission of integrated circuits is an important step in the design process of state of the art integrated circuits. In the present paper we describe the use of the TEM-cell and the surface scan method according to a standard from the IEC as well as a combined version of these two methods. We present how these methods could be used in the characterization of test chips. We also present how the combined method was used to reduce the electromagnetic emission of a state of the art integrated circuit for automotive applications.

Categories and Subject Descriptors
B.7.2 [**Integrated Circuits**]: Design Aids; B.8.1 [**Hardware**]: Reliability, Testing and Fault-Tolerance

General Terms
Measurement, Performance, Design, Reliability, Standardization

Keywords
Electromagnetic emission (EME), TEM-Cell method, surface scan method

1. INTRODUCTION
In state of the art integrated circuit (IC) design, like complex mixed-signal IC or system on chip (SoC) design, the increase of the complexity, the operating frequency, and the miniaturization of ICs as well as the decrease of the power supply lead to an increasing number of electromagnetic compatibility (EMC) problems in analog and mixed analog-digital circuits. In general ICs are able to rectify a radio frequency signal and to react to demodulated signals. This often causes failures in the functionality of the IC and may be safety critical.

GLSVLSI'03, April 28-29, 2003, Washington, DC, USA.

On the other hand ICs usually do not radiate significantly, but they are often the source of the radiated energy and therefore the source of EMC problems in electronic application. But there is still a missing link between EMC problems on chip-level and EMC problems on the final application- (or device-) level. Moreover, a large amount of research work has to be done in the near future to fill this gap in the design flow.

It is considered as a common fact so far, that dynamic switching currents on the supply lines are one of the main sources for the electromagnetic emission (EME) of ICs. These high current peaks cause voltage swings on the supply lines due to the inductances of the interconnections and the bond wires as well as the lead frames. This is exemplified with an inverter, representing the last inverter in a typical inverter chain of an output buffer cell, in figure 1. Due to the parasitic elements of the package (resistors, inductances, and capacitances) the internal voltage levels (die VDD and die ground) differ from the external voltage levels (PCB VDD and PCB ground). E.g. there is no single ground or reference ground.

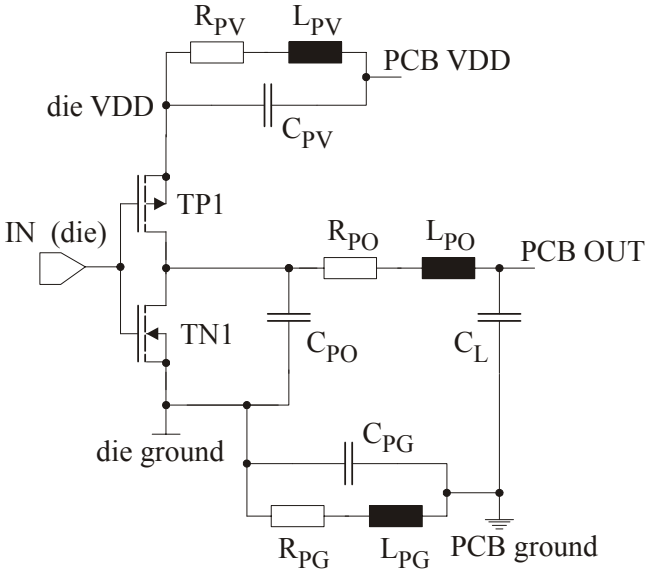

Figure 1. Simple CMOS output driver with parasitic package model.

A common method to reduce these voltage swings on the supply lines, are the use of off- and on-chip decoupling capacitors, although the optimal placement of the on-chip capacitors are not well known up to now [8]. The capacitors are connected between "die VDD" and "die ground" or "PCB VDD" and "PCB ground", respectively. The latter placed as close as possible to the IC on the PCB. Another method to reduce the switching currents and therefore the voltage swings is the eliminating of the crowbar currents in the output cells. A temporary power down (shut-down) of circuit parts during non-use is also a possible solution. There are some other methods, but all of these methods have one common aspect in mind, the improvement of the EMC of the IC.

To verify the improvements in the design for EMC special measurement techniques are needed, which were currently available through two standards, described briefly in the following section. We present in this contribution, how two special methods could be successfully combined in the redesign process for the reduction of the EME of an IC. With these two methods, we were able to identify the region within the IC, which was responsible for the higher emission and therefore we were able to redesign the chip accordingly.

2. MEASUREMENT METHODS

For the EMC characterization on chip-level the subcommittee 47A (Integrated Circuits) of the IEC (International Electrotechnical Commission) is working towards two standards – the "IEC 61967: Integrated circuits – Measurement of electromagnetic emissions 150kHz to 1GHz" [3] and the "IEC 62132: Integrated circuits - Measurement of electromagnetic immunity" [7].

The current version of the IEC 61967 is split in 6 parts: general conditions and definitions (part 1), measurement of radiated emissions – TEM-cell method (part 2), measurement of radiated emissions – surface scan method (part 3), measurement of conducted emissions – 1Ω/150Ω direct coupling method (part 4), measurement of conducted emissions – workbench Faraday cage method (part 5) and measurement of conducted emissions – magnetic probe method (part 6). The two parts related to this work are the part 2 [4] and part 3 [5].

Any of these measuring methods, which are described in the standards, can be used as a basis for the specification of the emission of an IC. All these methods have their advantages and limitations. Therefore one should carefully select those measuring method, which best fits the demanded requirements.

2.1 The TEM-Cell Method

The TEM-cell (**t**ransverse **e**lectro**m**agnetic transmission cell [1]) method is used to measure the electromagnetic radiation from an IC [2], [4]. The IC acting as device under test (DUT) is mounted on a special test printed circuit board (PCB) which has to be designed according the standard [4], [6]. The test PCB is clamped to a mating port, which is cut in the top or bottom of a TEM-cell. The test PCB therefore becomes a part of the cell wall and the IC (DUT) is within the cell. This test PCB has to be designed in a way that all connecting leads within the cell are eliminated. All the connecting leads should be located on the backside of the board outside the cell. So only the operating IC (DUT) is allowed to be inside the cell (see figure 2).

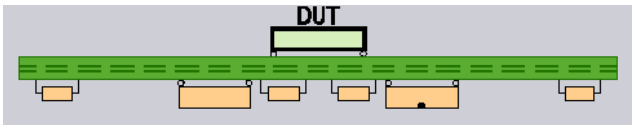

Figure 2. Test PCB with DUT and other circuitry.

The TEM-cell has two 50Ω ports. One of these ports is terminated with a 50Ω load. The other 50Ω port of the TEM-cell is connected to the input of a spectrum analyser to measure the RF emissions emanating from the IC and impressed onto the septum of the cell. An EMI receiver can also be used instead of a spectrum analyser. The TEM-cell is shown in figure 3.

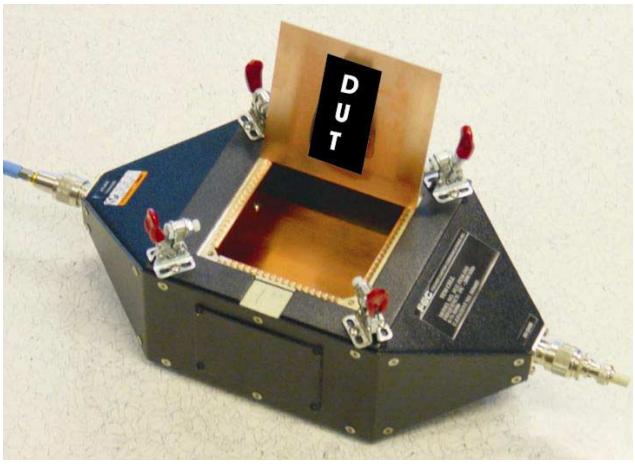

Figure 3. TEM-cell with test PCB and device under test (DUT).

2.2 The Surface Scan Method

The surface scan method described in IEC 61967-3 [5] is used for evaluating the near electric (E) field or the near magnetic (H) field component at the surface of an IC. This method can be used over the frequency range from 10MHz to 3GHz. To measure the distribution of these fields an E- or an H-field probe (an example is shown in figure 4) is mechanically moved over the surface of the IC, where the probe can be placed in a parallel or perpendicular plane to the IC surface.

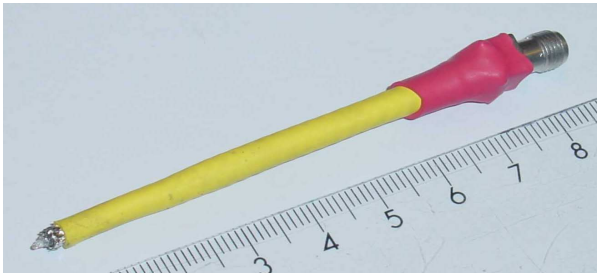

Figure 4. H-field probe for the surface scan method.

The measured data can be computer processed and the field strength at a specific scan frequency can be visualized in a colored representation. The resolution reachable with this method is closely linked to the precision of the mechanical probe

positioning system and the size of the used probes. In the laboratory of the austriamicrosystems AG the probes are moved by a micropositioner (figure 5).

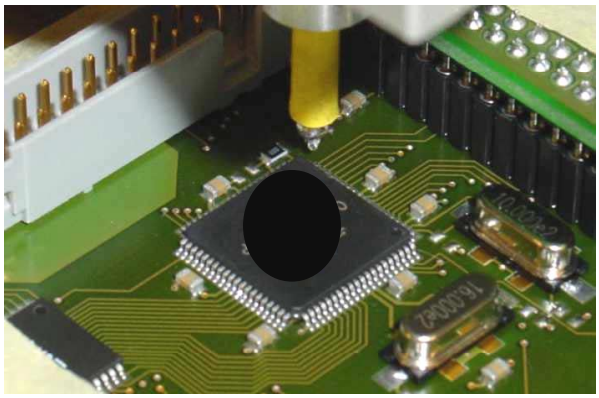

Figure 5. Surface scan setup (IC with H-field probe).

The surface scan method can be applied to any IC mounted on a PCB that is accessible to the probe. For comparison measurements between different chip architectures, a standardized test PCB shall be used. The electric and magnetic field scan over the surface of the IC yields information of the relative strength of the sources of the EME.

2.3 The Use of the Methods during the Design

During the IC design process the two described measurement methods could be used in different ways. According to the standard the TEM-cell and the surface scan method will be used over a well-defined frequency range. Both methods could be used for a characterization of the EME of the IC as a single measurement method.

On the other hand a combination of both methods could be an interesting way to find out, where the problems in the EME of an IC exist in detail. An example will be given later in this paper. This measurement strategy works in the following way: First, a TEM-cell measurement is carried out to find critical frequencies with to high values of EME. Second, a surface scan only at this selected frequency is done to check which areas of the IC contribute most to the EME of the IC. This detailed information is very helpful for a redesign to improve (reduce) the EME. The advantage of this combined method is to shorten the time for the surface scan method without loosing too much of the detail information from this method.

3. DESIGN EXAMPLES

3.1 IC for Automotive Applications

The combined method was used for the redesign of an IC for automotive applications. First, the TEM-cell method was performed to detect the frequencies with to high EME. The measurement result of the TEM-cell method is shown in figure 6.

To compare the results of different measurements the emission level scheme could be used. The typical description of the maximum emission level consists of two letters and one number always following the same sequence. Assuming that one of the three slopes is not needed then the corresponding letter or number will be left off. The capital letter is first and represents the position of the horizontal line with 0dB/decade slope. Second is the number, which defines the position of the -20dB/decade slope. The third and small letter defines the position of the -40dB/decade slope. The maximum emission level in figure 6 is therefore “F3”. It has to be mentioned, that within the scope of this paper and for relative comparison, we didn’t extracted the influence of the measurement equipment (e.g. an amplifier was used) for the following measurement results. The absolute EME of the IC is accordingly lower, but due to the use of dB values, this is only a linear subtraction with always the same factor for all our results.

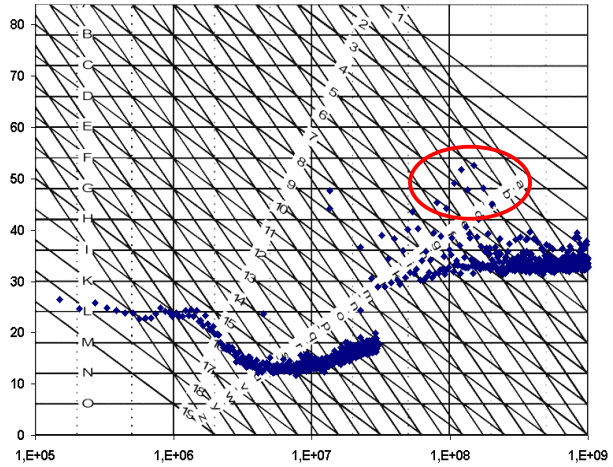

Figure 6. Result of the TEM-cell first design.

As can be seen, the frequency with the highest EME is in the frequency range about 149MHz (circle in figure 6). Next, a surface scan was performed in a chosen bandwidth around the frequency of 149MHz. For the surface scan only the magnetic field distribution was measured. The result of the surface scan is shown in figure 7. The area of highest magnetic field was found in the upper right corner. The circuit parts, which were responsible for the high emission, were therefore being located immediately.

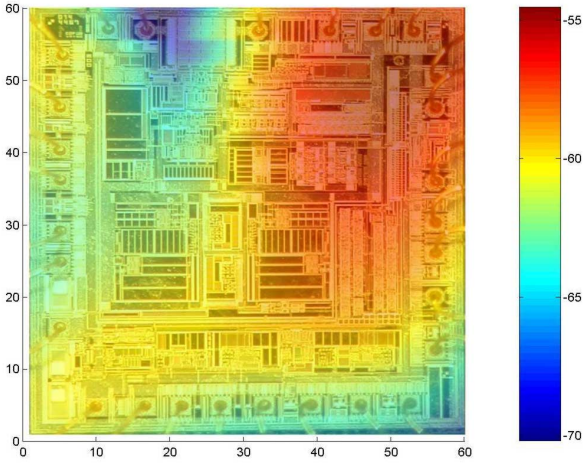

Figure 7. Magnetic field at the surface of the die.

From this investigation a redesign of these circuit parts was possible to reduce the EME. A surface scan from the redesign is shown in figure 8.

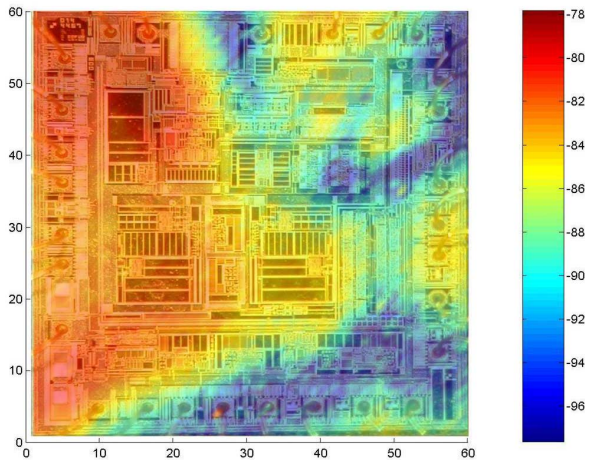

Figure 8. Magnetic field at the surface of the redesign.

For the comparison of figure 7 and 8 it is important to know, that the scale of the right column in figure 7 has the range –70 to –55dBm and in figure 8 –98 to –78dBm. So the surface scan from the redesign shows that the max. EME of the IC was reduced by at least 15dB. To verify the reduction of the EME over the full frequency range a TEM-cell measurement of the redesigned IC was performed again. The result is shown in figure 9. From this measurement it could be seen, that the electromagnetic emission of the IC was reduced to "H4".

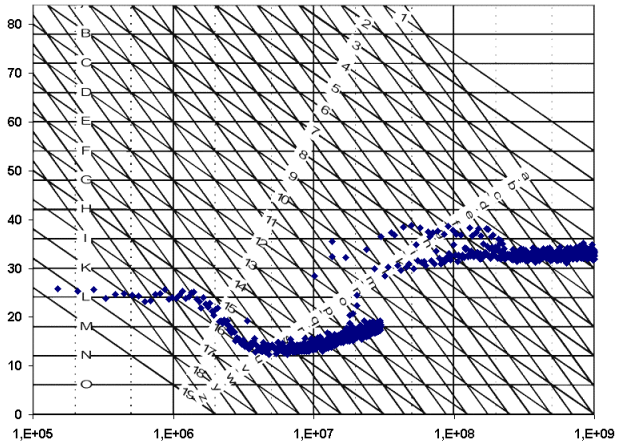

Figure 9. Result of the TEM-cell redesign.

The comparison of figure 6 and 9 shows again the reduction of the EME of 15dB in the considered frequency range around 149MHz, which was possible by using one of the design methods, mentioned in the introduction section.

4. CONCLUSION

To fully understand the electromagnetic emission of integrated circuits, especially to understand how these emissions can be reduced over a great frequency range, a lot of work will still have to be done. But now with two of the electromagnetic emission measurement methods for ICs, which are described in IEC 61967, measurement strategies are available to support this work. We have shown that the combination of the TEM-cell and the surface scan method is a useful instrument during the redesign process for improved EMC behavior of ICs. With one of those methods mentioned in the introduction of this paper a perceptible reduction of the electromagnetic emission is possible and could be observed.

5. ACKNOWLEDGMENTS

The authors like to thank Roland Jungreithmair from austriamicrosystems AG for his support in the measurements.

6. REFERENCES

[1] M. L. Crawford: "Generating of Standard EM Fields Using TEM transmission cells.", IEEE Trans. on Electromagnetic Compatibility, vol. EMC-16, no.4, nov. 1974, pp. 189-195

[2] R. De Smedt, S. Criel, F. Bonjean, G. Spildooren, G. Monier, B. Demoulin, and J. Baudet, "TEM Cell Measurement of an Active EMC Test Chip," in Proceedings of the IEEE International Symposium on EMC, Washington DC, USA, pp. 903-908

[3] IEC 61967-1, Ed.1: Integrated circuits – Measurement of electromagnetic emissions, 150kHz to 1GHz – Part 1: General conditions and definitions, Final Draft International Standard 47A/61967-1/Ed.1, 47A/632/FDIS, 2001-12-14

[4] IEC 61967-2, "Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz –Part 2: Measurement of radiated emissions, TEM-cell method and wideband TEM-cell method (150 kHz to 8 GHz)", 47A/619/NP, New Work Item Proposal, Date of proposal: Jul. 2001

[5] IEC 61967-3: "Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz –Part 3: Measurement of radiated emissions, surface scan method (10 kHz to 3 GHz)", 47A/620/NP, New Work Item Proposal, Date of proposal: Jul. 2001

[6] IEC 47A/552/NP, "Universal testboard for measurement of EMC of ICs", SC47A/WG9, New Work Item Proposal, Date of proposal: Feb. 1999

[7] IEC 62132-1: "Integrated circuits - Measurement of electromagnetic immunity, 150 kHz to 1GHz - Part 1: General and definitions", 47A/618/CD

[8] T. Ostermann, D. Schneider, C. Bacher, B. Deutschmann, R. Jungreithmair, W. Gut, C. Lackner, R. Koessl, R. Hagelauer: „Characterization of the influence of different power supply styles on the electromagnetic emission of ICs by using the TEM cell method (IEC 61967-2)" 3rd International Workshop on Electromagnetic Compatibility of Integrated Circuits, 14-15. Nov. 2002, Toulouse, France, pp. 57-60