Optimization of a fully integrated Low power CMOS GPS receiver

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Abstract

This paper describes an optimization technique able to optimize a complete wireless receiver architecture in a reasonable amount of time. The optimizer alternates between spice level optimizations of simple building blocks and a full architecture optimization of the whole based on accurate models of the building blocks. The models of the building blocks are interpolated over the data points acquired in the Spice level simulations. The optimizer technique has been applied to the optimization of an architecture for a GPS receiver. The optimal design has been implemented in a standard $0.25\mu m$ CMOS process.

1 Introduction

The full Spice level optimization of a complete wireless receiver architecture is with present day computing technology virtually impossible in terms of computation times. Many of the optimization problems in wireless IC design suffer from the presence of signals with a wide range of frequencies. Simulating this kind of systems with an acceptable level of accuracy usually leads to very long computation times. This will render full Spice RF optimizations very difficult if not impossible.

New techniques to overcome this problem were searched and different solutions arose. On one hand the Smart evolutionary algorithms[1] yield a general speed-up of the Spice level optimization process, while different mathematical techniques tend to improve the simulation speed of circuit level simulations by exploiting typical effects present in RF circuits[2]. still these techniques were only able to cope with the optimization of sub-blocks of a reasonable size and complexity.

If the "Divide and Conquer" principle is applied to this optimization problem, it becomes an attainable target to optimize a wireless receiver architecture for a given set of specifications. In this case the full optimization is split up in the optimization of the sub-blocks. During these optimizations, accurate models for the sub-block performance are generated. These models can be used for a high level full receiver optimization and trade-off study. This approach can yield an important improvement in optimization speed in case where the evaluation time of the approximating models is small in comparison to the full Spice level optimization.

2 Optimizer

The Optimization problem can be defined as follows:

Given a set of performance specifications for a GPS receiver architecture (noise level, distortion level, dynamic range, frequency,....), find the optimal parameter set for which the overall power consumption is minimized.

This optimization problem is split up in several sub-block optimization problems where a specific sub-block of the receiver (eg. LNA, mixer, AD, PLL,...) is optimized using a speed improved optimization routine [1]. The final result of these optimizations is a set of optimal parameters for each sub-block satisfying its performance requirements and a set of fitted mathematical models able to accurately describe the relationship between the design parameters and the performance of the sub-block in a certain validity region around the optimal point.

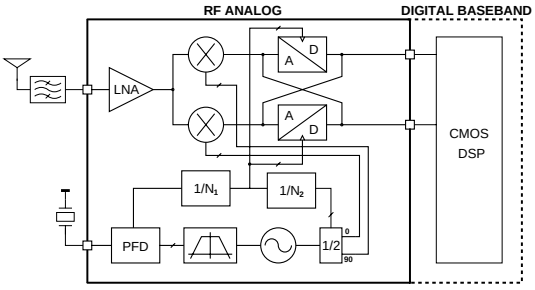

Figure 1. GPS receiver architecture

After all the sub-blocks have been optimized, their models can be used in the full architecture optimization. Since this only requires the optimization of mathematical models, this can be done with low CPU overhead as compared to the Spice level evaluations, while still achieving the required accuracy. In case the optimization leads to a point outside of the accurate region of the sub-block model, the model fitting of the sub-block has to be redone. This process is repeated until an optimal point is achieved.

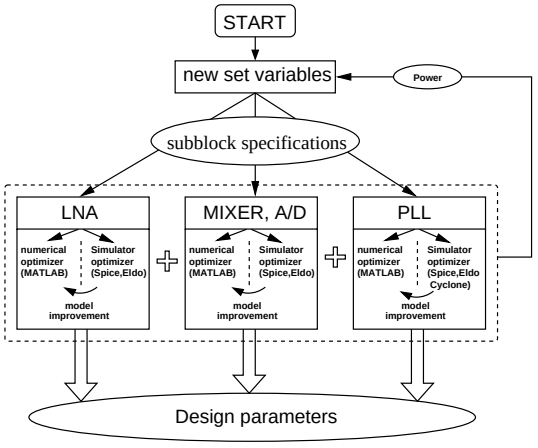

Figure 2. Optimization process with the separate sub-block optimization routines

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This optimization technique has been applied to the optimization of the architecture shown in fig.1. The architecture is split up in a set of sub-blocks which have a low degree of interaction. At the input, the LNA amplifies the input signal. This is mixed to the IF frequency by the input mixer. The IF frequency is A/D converted by the $\Delta\Sigma$ converter with a complex bandpass filter. the LO signals driving the mixers are derived from a Phase Locked Loop (PLL). The full optimization process is depicted in fig.2. Here, the set of design variables determining the architecture, is generated by the optimizer. The optimizer for each sub-block gets its appropriate design parameters from the top-level architecture optimizer. Based on the level of model fitting in each sub-block, the sub-block optimizer decides to use a Spice level simulation or a model evaluation. The decision between both evaluations is done, based on the algorithm described in [1].
At the end of the optimization process, the outcome is a set of optimal parameters and a set of fitted sub-block models.
In the next sections, each of the sub-block optimizers and the models they are based upon, are described in further detail.

3 Optimization of the LNA

3.1 Basic operation

The LNA subblock optimizer interacts with the global optimizer in the following way. As input, the LNA optimizer receives certain performance parameter values that need to be attained. The optimizer will check if the set of specifications lies within the realizable design space of the amplifier. If so, it will output the required power consumption, allowing a global minimization of the power consumption.
Three performance parameters are conveyed by the global optimization algorithm to the LNA optimizer. The degradation in SNR is communicated by means of the Noise Figure (NF). The signal degradation due to distortion is passed to the algorithm in the form of the IIP3. Finally, also the required voltage gain, G_v, is fed to the LNA optimizer.

3.2 Simplified models

The LNA topology is based on the cascoded common source configuration with inductive source degeneration. This type of structure has been shown to be able to provide very low noise figures and high gain at a low level of power consumption [3].
The behavioral model describing the LNA performance is mostly based on the following approximative models.3

$$I_{ds} = \frac{KP}{2}.\frac{W_{eff}}{L_{eff}}.\frac{V_{GST}^2}{1+\Theta.V_{GST}}.(1+\lambda V_{ds}) \quad (1)$$

$$G_v = g_{m,eff}.R_{load} \quad (2)$$

$$F = 1+\frac{R_{gate}}{R_S}+\left(\frac{\omega_0}{\omega_T}\right)^2\frac{\gamma}{\alpha}g_m R_{eq}+\left(\frac{\omega_0}{\omega_T}\right)^2\frac{\gamma}{\alpha}\frac{2}{\kappa}+\frac{\alpha\delta}{\kappa g_m R_{eq}} \quad (3)$$

$$IIP3 = 11.25+10\log\left(\frac{V_{GST}(1+\Theta.V_{GST})^2(2+\Theta.V_{GST})}{\Theta.Q_{in}^2}\right) \quad (4)$$

In these equations, Θ models the mobility degradation in the MOST channel. Q_{in} and $g_{m,eff}$ are the quality factor and the effective transconductance of the input stage. R_{eq} represents the equivalent source resistance at the gate of the input transistor. Equations 1 to 4 give expressions for the power consumption, voltage gain, noise factor and IIP3 of the LNA.

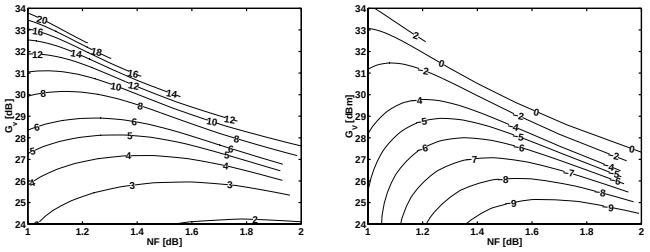
3.3 Specifications

Some specifications set the boundaries for the complete design space. Other specifications are passed by the global optimization algorithm to the LNA optimizer which than locates the point in the design space satisfying these specifications with minimum power cost. The first category includes:

$$S_{11} < S_{11,spec} \qquad Q < Q_{spec} \qquad Freq == Freq_{spec}$$

The first equation stems from the input matching requirement. The second specification takes care of possible shifts in resonance frequency due to process variations.
The second category consists of:

$$NF < NF_{spec} \qquad IIP3 > IIP3_{spec} \qquad G_V == G_{V,spec}$$



(a) (b)

Figure 3. (a) LNA power consumption and (b) IIP3 as function of noise figure and voltage gain

3.4 Simulation

The LNA optimizer calculates the power consumption from the given specifications: NF, IIP3 and G_V. This calculation is done from a first order numerical model based on the previous equations. If this model is not sufficiently accurate, it is modified based on spice level simulations. The algorithm keeps a list of the different models and the regions in the design space where they are valid. If the global optimizer requires a design point not covered by the existing models, the algorithm will interpolate or extrapolate from the existing models and do a spice level verification. In this way the total region in the design space covered by numerical models increases as the global optimization progresses. Hence, fewer and fewer spice level simulations are required and simulation time drastically decreases. Furthermore the fitted models may be reused in future optimizations.
Figure 3 show contour plots of the power consumption and IIP3 as a function of the noise figure and voltage gain, considered as independent variables. These plots are generated at the end of the global optimization. They show a selected region within the LNA design space, fully covered by the numerical models.The latter plot shows that the IIP3 of the LNA will not be a binding constraint since only values larger than about -15dBm are required.

4 Optimization of the PLL

The PLL optimizer takes a maximum allowable SNR degradation in the receiver due to the PLL as input from the global optimizer and returns the minimum necessary power consumption in the PLL to guaranty this maximum degradation as output.
The PLL used in this design is a fourth-order type II charge-pump PLL [4]. Due to the phase noise sidebands in the PLL, noise is folded back in the signal band. This gives rise to some extra noise which is represented as an SNR degradation factor. The extra noise generated by the PLL can be calculated with the following equation:

$$ExtraNoise = \int_{-1MHz}^{1MHz}\int_{0}^{2MHz}\Theta_{PLL}(\lambda)\cdot\Theta_N(s-\lambda)\,d\lambda\,ds \quad (5)$$

The extra noise is the convolution of the PLL with the noise in the signal band (5), which is 2MHz wide for civilian GPS systems. For simplicity, we assume that we have a very narrow-band bandpass filter in front of the receiver, so that only the 2MHz signal band passes through the filter. This way we can limit the convolution to the 2MHz band.
The PLL is characterized by three parameters: the VCO phase noise

level, the charge pump current and the loop filter bandwidth. The first two parameters are used in the optimizer while the latter sets the design space boundaries. The maximum bandwidth is determined by stability constraints and the minimum bandwidth is determined by the maximum capacitance which can be integrated on chip.
Once an optimal set of parameters is calculated, we still need to optimize the VCO given the phase noise level in the VCO. This is done with an in-house designed VCO-optimizer program CYCLONE [5]. It automatically performs finite element simulations and the optimization of RF-coils combined with VCO circuit sizing.

5 Optimization of the mixer-ADC

5.1 Topology and Basic Operation

The down-conversion is performed by differential I-Q switching mixers in series with the resistors in front of the ADC, driven by square waves derived from the PLL. The input resistance in series with the mixer ensures very linear mixing. The first filter block also provides a virtual ground for summation of the mixer and DAC pulse currents. This incorporation of the mixer within the ADC structure permits block reuse and thus power saving.
In figure 4 the mixer-ADC architecture is depicted. This architecture is discussed in detail in [6].

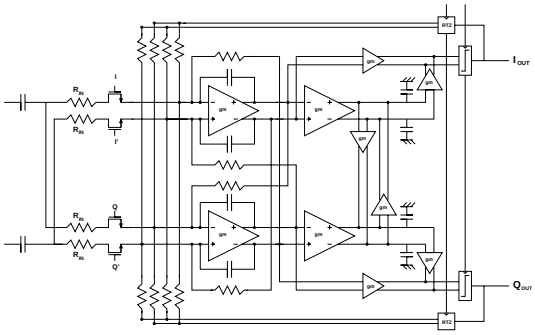


Figure 4. Mixer-ADC Architecture

5.2 Low Level Optimization

5.3 Simulation and High Level Optimization

After choosing an appropriate ADC structure, high level simulations provide the most suitable coefficients of the different AD blocks to attain the wanted SNR which provide sufficient noise shaping while still guaranteeing the loop stability. These parameters are translated to circuit level specifications for the different building blocks and a first set of design constraints (ie. the GBW of the filters OTA's) are fixed. A second set of specifications is given by the tolerated thermal noise floor and higher order distortion components of the ADC. Due to the $\Delta\Sigma$ with a 1-bit DAC implementation, the noise and linearity performance of the loop filter directly determines the overall performance of the ADC. The 1 bit DAC is inherently linear and has no distortion contribution.
Simulations are performed in different stages. Behavioral high level simulations of the entire ADC present a first step in the design with help of the mathematical toolkit Matlab. On one hand, the simulation of ideal blocks gives an indication of the theoretical maximal SNR attainable for a chosen $\Delta\Sigma$ configuration. On the other hand, non-idealities are systematically inserted to investigate the SNR degradation. The behavioral performance is measured by performing an FFT on the converter output. The ADC basically consists of a continuous time filter, a sampler/comparator and a 1bit DAC. Therefore the transient time response of the filter to the different input signals permits to calculate the voltages on the different filter nodes and comparator output. Three input contributions are distinguished: first a sine wave input with certain frequency and phase, secondly and thirdly the time response contribution after one clock period of the DAC output pulse and the values at the previous time sample (begin conditions). These transient time functions are first mathematically calculated using the toolkit Maple which allows an algebraic expression of the models. Using the DE Generic Algorithm the optimal ADC parameters are derived. Transient time step simulation using transistor models performed in Eldo confirm a mathematical approach and permits the incorporation of more non-idealities like distortion and parasitic effects. Finally the mixer-ADC is fully simulated on transistor level with Eldo to check the functionality also considering probable process variations.

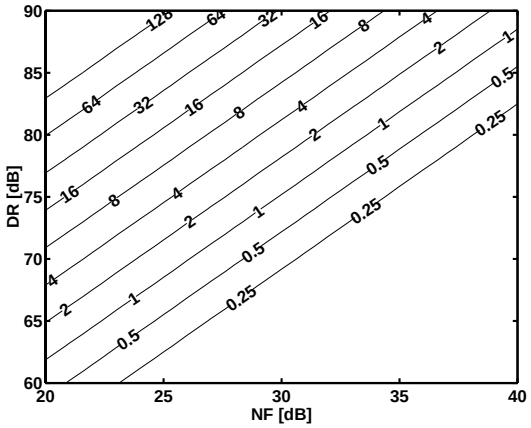


Figure 5. ADC Power as function of DR and NF

5.4 Low Level Optimization

The filter is a 2nd order continuous time complex bandpass filter. Because of the continuous time filter type and the aim of integration of the mixer within the ADC the first filter block is implemented as an RC active continuous time lossless integrator [7]. The external resistance degenerates and linearizes the MOS transconductance. The value of this resistor *Rin* determines the NF of the entire $\Delta\Sigma$ architecture. The linearity is determined by the level $gm*Rin$ of degeneration of the input transistors [8]. This implies that for a certain NF, the power drain in the filter opamp is proportional to the desired DR. The following formula is used to describe the power consumption of the mixer-ADC in function of DR en NF, both in dB.

$$P \sim Vgst^{1/2} * 10^{\left(1/10*\left(DR-(NF*4/3)\right)\right)} \quad (6)$$

Vgst is the Vgs-Vt of input transistor of the first filter block. Figure 5 shows the power consumption of the ADC in function of the DR and NF. The first filter block is implemented as an RC filter and is the most important block in the loop-filter for noise and linearity considerations. A sufficient degeneration satisfies both the strength of the virtual ground and the linearization of the transconductance. The filter GBW is determined by the *RC* time constant and not gm/C and can thus be set more accurately [9]. On the contrary the requirements for the second filter are much more relaxed in comparison to the first, particularly the noise and linearity specifications are lowered by the gain of the previous block. A simple low power gmC filter implementation with a minor internal degeneration is suitable.

6 Architecture trade-off

The full architecture has been optimized using the discussed technique and sub-block models. An appropriate starting point for the optimization was chosen based on design experience of the building blocks. the optimization resulted in an optimal design point for the given specifications and trade-off models for each of the building blocks.

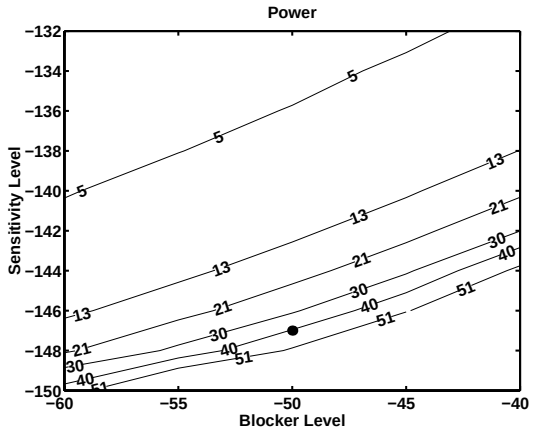


Figure 6. GPS receiver power trade-off versus sensitivity level and blocker power at the architecture level

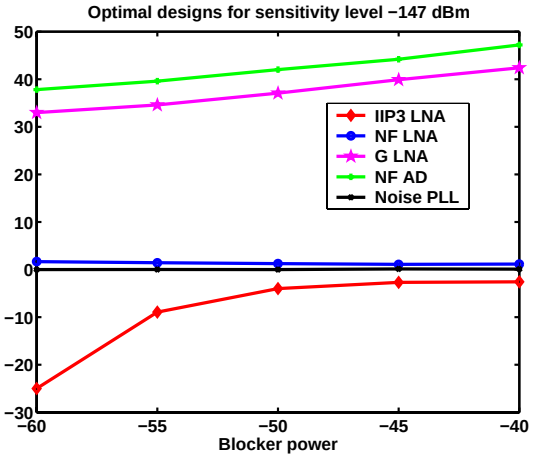


Figure 7. Trade-off of design parameters for different blocker levels

Using these models, it is possible to investigate the high level trade-offs for parameter sets in the valid region of these models. One interesting trade-off study is the variation of the power consumption as function of the required dynamic range of the receiver. This dynamic range is determined by the receiver sensitivity level and the maximum tolerable input blocker level. Fig. 6 shows the variation of the total receiver power consumption as function of the receiver sensitivity level and the maximum input blocker power. It can clearly be seen that the power increases for increasing blocker level and decreasing sensitivity level. The point which was used in the implementation of the receiver is indicated by the dot.

The full set of parameters for which the chip was optimized is shown in table I.

The design was processed in a 0.25μ CMOS technology. A photograph of the 4mm*4mm chip is shown in fig.8. The full chip has been measured and conforms to the GPS standard [4].

7 Conclusions

This paper describes an optimization technique which is able to speed up the optimization of a full wireless receiver architecture to a reasonable amount of time while still attaining a high level of simulation accuracy. The optimizer alternates between the spice level optimization of simple building blocks, while modeling the performance parameters and a full receiver optimization based on the extracted accurate models of the building blocks. The optimizer has been applied to the optimization of an architecture for a GPS receiver. The designed circuit fully qualifies the requirements for a GPS receiver architecture.

Specification	optimization parameter	
Frequency	1.57	GHz
Input Sensitivity	-147	dBm
Maximum Blocker Level	-50	dBm
NF LNA	1.5	dB
LNA Gain	35	dB
NF AD	35	dB
LNA Power	8	mW
ADC Power	14.2	mW
PLL/VCO Power	17	mW
LO-buffer Power	2	mW

Table I. Final optimized parameters of the GPS receiver

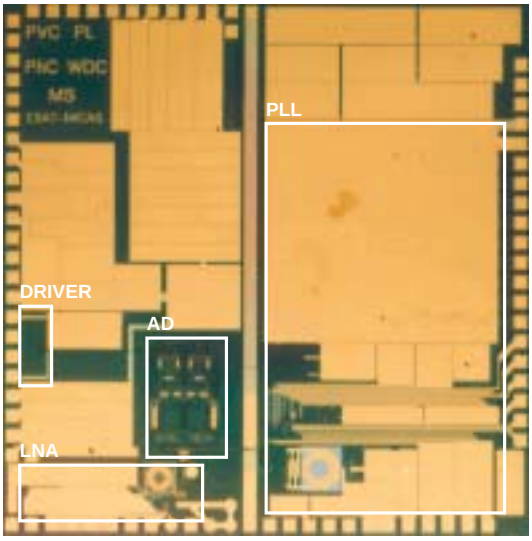


Figure 8. GPS receiver micrograph

8 Acknowledgments

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References

[1] P. Vancorenland, C. Deranter, G. Gielen, and M. Steyaert, "Optimal RF design using smart evolutionary algorithms," in *Proc. of the 37th Design Automation Conference*, June 2000.

[2] S. S. Mohan, M. del Mar Hershenson, S. P. Boyd, and T. H. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE Journal of Solid State Circuits*, vol. 34, no. 10, pp. 1419–1424, October 1999.

[3] P. Leroux, J. Janssens, and M. Steyaert, "A 0.8dB NF ESD protected 9mW CMOS LNA," in *Proceedings of the International Solid-State Circuits Conference*, February 2001.

[4] M. Steyaert, P. Coppejans, W. De Cock, P. Leroux, and P. Vancorenland, "A fully integrated gps receiver front-end with 40mw power consumption," in *Proc. of the 2002 IEEE International Solid-State Circuits Conference*, Feb. 2002.

[5] C. De Ranter, B. De Muer, G. Van der Plas, P. Vancorenland, M. Steyaert, G. Gielen, and W. Sansen, "CYCLONE: Automated design and layout of RF LC-oscillators," in *dac*, LA, jun 2000, pp. 11–14.

[6] P. Vancorenland, Ph. Coppejans, W. De Cock, and M. Steyaert, "A quadrature direct digital downconverter," in *Proc. of the 2002 Custom Integrated Circuits Conference*, May 2002.

[7] J. Silva-Martinez, M. Steyaert, and W. Sansen, *High-Performance CMOS Continuous-Time Filters*, Kluwer Academic Publishers, 1993.

[8] W. Sansen, "Distortion in Elementary Transistor Circuits," *IEEE Transactions CAS-II*, vol. 46, no. 3, pp. 315–324, March 1999.

[9] E.J. van der Zwan and E.C. Dijkmans, "A 0.2-mW CMOS ΣΔ Modulator for Speech Coding with 80 dB Dynamic Range," *IEEE Journal of Solid State Circuits*, vol. 31, no. 12, pp. 1873–1880, December 1996.