Shaping Interconnect for Uniform Current Density *

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ABSTRACT

As the VLSI technology scaling down, the electromigration problem becomes one of the major concerns in high-performance IC design for both power network and signal interconnects. For a uniform width metal interconnect, the current flows through the driving point is much larger than that flows through the fan-out point since much of current bypasses to the ground through the parasitic capacitance. This causes the lifetime of driving point to be quite shorter than that of fan-out point due to electromigration. In order to avoid breakdown at the driving point, wire sizing is an effective solution. Thus we present a wire shape, of which the current density as well as the lifetime is uniform along the wire. SPICE simulation results show the uniformity of current density of this wire shape. Under the same current density bound, we demonstrate that chip area and power consumption are significantly reduced for this wire shape compared to the uniform width wire. The wire shape functions we derived are continuous. However, it is not necessary to ultra-accurately reproduce the continuous shape on the silicon, since we can round the continuous shape to the nearest available litho width and this will not degrade the uniformity of current density.

1. INTRODUCTION

As VLSI circuits are shrunk into nanometer feature size and operate in giga-hertz frequency, interconnects have become dominant in determining system reliability [1,2,7]. One of the critical reliability problems in metal interconnect is electromigration and it is one of the main mechanisms that cause the failure of IC at any time during its lifetime [3,4]. Electromigration problem not only exists in the power network but also in signal nets. Though the current of some signal nets are bi-directional, and even the current waveforms of two directions are identical, their damage healing factors are not equal to 1. Moreover, the Joule-heating that causes the temperature-gradient-induced flux divergences can also attenuate the reliability of interconnects. Thus, the electromigration problem in signal nets is becoming one of the major concerns in IC design process [10, 12, 17]. Furthermore, the topology of IC signal nets becomes so complicated that the efforts of saving chip area and power consumption of interconnects push the signal interconnect design to the limits of the fabrication technology. This certainly aggravates the electromigration problem in signal interconnects.

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Electromigration is caused by high current density in the metal interconnect, which results in the transport of mass in metal [9,13]. The Mean-Time-To-Failure (MTTF) of metal interconnect is related to current density, moreover, in some cases, small current density difference in metal wires can incur huge difference in MTTF. Li *et al.* [8] reported, in some instances, 38% difference in current density could lead to more than 26 times difference in MTTF. For a uniform width metal interconnect, the current density of the wire at driving point is much larger than that of fan-out point since much of current bypasses to the ground along the wire through the parasitic capacitance, as shown in Figure 1. With the increasing of operating frequency and parasitic capacitance, the difference of current density between the driving point and fan-out point becomes more significant. This causes the MTTF of the uniform width wire at driving point to be much shorter than that at fan-out point. Moreover, in VLSI design, if we determine the minimum wire width according to the current flowing through fan-out point to meet the current density requirement, the wire segments near driving point will exceed the current density bound since the current density at driving point can be several times larger than that at fan-out point (refer to Figure 6). On the other hand, if we determine the minimum wire width according to the current at driving point, the wire width of the segments near fan-out point will over-satisfy the current density bound. Thus it will result in waste on chip area and power consumption due to those unnecessary wide segments.

Hence, in this paper, we present a wire shape function, of which the current density is uniform along the whole wire, so that the MTTF is uniform as well. To derive the wire shape function, we first use an interconnect model without taking the wire resistance into consideration. However, we demonstrate that this shape function, which is without wire resistance consideration, can give satisfied uniform current density in most of practical cases. Moreover, we compare this shape wire with the uniform width wire and the comparison results show that, under the same current density bound, this shape wire saves much chip area and power consumption. Finally, we demonstrate that, only if the wire is unusually long, we need to take the wire resistance into consideration. A wire shape function is derived for such unusually long wires.

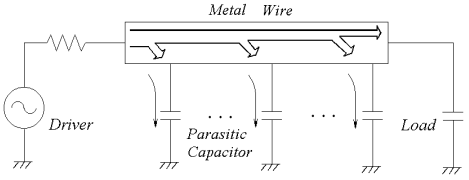

Figure 1. Current bypasses to the ground through the parasitic capacitance of the wire.

2. WIRE SHAPE FUNCTION

In this section, we will derive a wire shape function with uniform current density. The parasitic capacitance of the interconnect at location *x* with length *dx* is given by the following function [5]

$$c(x) \cdot dx = \left(c_0 \cdot w(x) + c_f\right) \cdot dx \tag{1}$$

where $c_0 = \frac{1}{T_{ox}} 1.15\epsilon_{ox}$ and $c_f = \epsilon_{ox} 2.80\left(\frac{T}{T_{ox}}\right)^{0.222}$. They are unit length area capacitance and fringing capacitance, respectively, and both are manufactory process related parameters [11]. $w(x)$ is the width of wire segment at *x*, as shown in Figure 2.

Let $I(x,t)$ denote the current flowing though the wire segment at *x* and time *t*, and it can be expressed as

$$I(x,t) = I_l(t) + \int_0^x \frac{\partial V(x,t)}{\partial t} \cdot c(x) \cdot dx \tag{2}$$

where $I_l(t)$ is the current flowing to the load capacitance at time *t*, $V(x,t)$ is the voltage of wire segment at *x* and time *t*. We take an assumption that the wire resistance is negligible, and consequently, there is no difference in the amplitude and phase of $V(x,t)$ along the wire. Thus the voltage is not related to *x* and we denote $V'(t)$ as the voltage derivative with respect to *t*. It will be shown later that this assumption does not degrade the uniformity of wire current density. Substituting (2) into (1), we get

$$I(x,t) = I_l(t) + \int_0^x V'(t) \cdot \left(c_0 \cdot w(x) + c_f\right) \cdot dx \tag{3}$$

We assume that the height of metal wire is a constant as given in most of manufactory processes. Besides, we will use the term linear current density instead of area current density and when we mention current density we refer to linear current density in the rest of this paper since uniform linear current density along the wire is equivalent to uniform area current density if the wire height is a constant. The linear current density at *x* is defined as: the current flows through the wire at *x* divided by the width of the wire at *x*. From (3), we get the current density at *x*

$$\frac{I(x,t)}{w(x)} = \frac{I_l(t) + V'(t) \cdot \int_0^x \left(c_0 \cdot w(x) + c_f\right)\, dx}{w(x)} \tag{4}$$

Assume c_l is the load capacitance and w_0 is the width of the segment at x=0. Thus the current density at fan-out point is

$$\frac{I_l(t)}{w_0} = \frac{V'(t) \cdot c_l}{w_0} \tag{5}$$

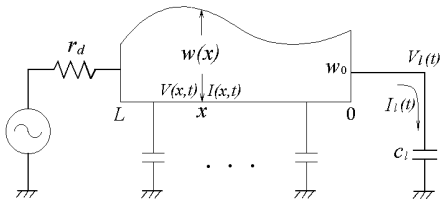

Figure 2. The wire width at *x* is *w*(*x*), the voltage and current at location *x*, time *t* is *V*(*x*,*t*) and *I*(*x*,*t*), respectively.

Our goal is to get uniform current density along the wire, thus the current density at *x* should be equal to that at fan-out point.

$$\frac{I_l(t)}{w_0} = \frac{I(x,t)}{w(x)} \tag{6}$$

Substituting (4) and (5) into (6), we get

$$\frac{w(x)}{w_0} \cdot V'(t) \cdot c_l = I_l(t) + V'(t) \cdot \int_0^x \left(c_0 \cdot w(x) + c_f\right) dx \tag{7}$$

Differentiating (7) with respect to *x*, we get

$$\frac{dw(x)}{dx} = \frac{w_0 c_0}{c_l}\left(w(x) + \frac{c_f}{c_l}\right) \tag{8}$$

Move $w(x) + \frac{c_f}{c_l}$ to the left hand side and *dx* to the right hand side,

$$\frac{dw(x)}{w(x) + \frac{c_f}{c_l}} = \frac{w_0 c_0}{c_l} dx \tag{9}$$

Integrating both sides of (9) from 0 to *x*, we get the wire shape function:

$$w(x) = \left(w_0 + \frac{c_f}{c_0}\right) e^{\frac{w_0 c_0}{c_l} x} - \frac{c_f}{c_0} \tag{10}$$

We notice that the wire shape is exponential for the uniform current density.

3. EXPERIMENTAL RESULTS

3.1 The Uniformity of Current Density

Based on the wire shape function (10), we generate 1000 VLSI wires with different wire parameters to verify the uniformity of current density. The wire parameters are selected in the following ranges [14,15], $r_d \sim 10\Omega$–$10K\Omega$, $c_l \sim 5$–$1000f$F, $r_0 \sim 0.05\Omega$–$0.5\Omega/\square$, $c_0 \sim 0.02$–$0.10f$F/μm^2, $c_f \sim 0.08$-$0.2f$F/μm, $L \sim 10$–2000μm. We use SPICE to calculate the current density for these wires and the results show that the maximum deviation error for the current density along the wire among all the experiments is 5.2%. We present two experimental results in Figure 3 and Figure 4. Figure 3 shows the RMS current density of the wire from fan-out point to driving point. RMS current value is always used in conservative electromigration model and is the most common criteria in electromigration analysis. However, for the high frequency current, the average effective current [6,16] is preferred to be used in this electromigration analysis model. The average effective current density J_{avg} is calculated by the following equation:

$$J_{avg} = J_+ + \gamma J_- \tag{11}$$

where J_+ and J- are the average current densities during the positive and negative pulse and γ is the damage healing factor. The experiment result of the average effective current density along the wire is shown in Figure 4. The parameters used in these two experiments are as follows: r_d=60Ω, c_l=25fF, r_0=0.08$\Omega/\square$, c_0=0.035fF/μm^2, c_f=0.1fF/μm, w_0=0.18μm, L=2000μm, γ=0.9. The waveform of the driver is 1GHz periodical ramp signal and its rising and falling time of the ramp is 50*p*s, respectively.

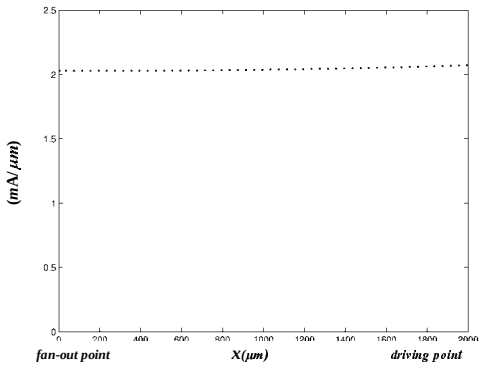

Figure 3. RMS current density along the wire from fan-out point to driving point.

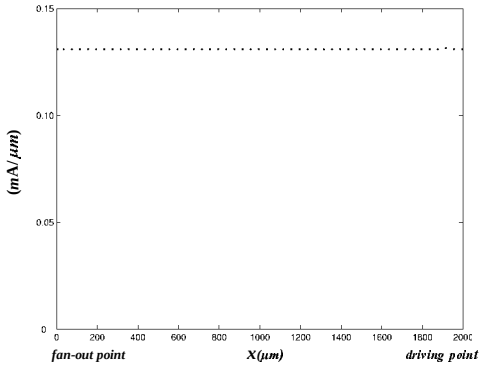

Figure 4. Average current density along the wire from fan-out point to driving point.

From these experiments, we notice that, though the wire resistance is not considered in the derivation, the current density is shown uniform along the wire. The reason is that the voltage amplitude and phase difference caused by the wire resistance is not a significant factor in determining the wire shape function. However, if the wire becomes unusually long, we need to take wire resistance into consideration. We will discuss this point in section 4.

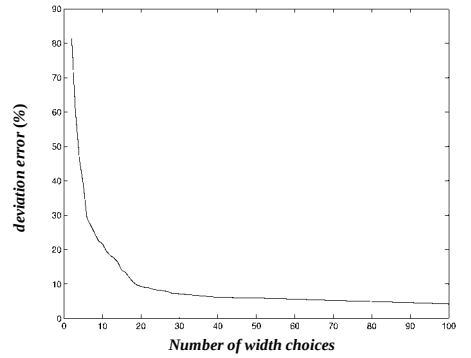

Figure 5. The deviation error of current density versus the number of width choice of the staircase shape wire.

Remark 1:

The wire shape function we derived is continuous. However, it is not necessary to ultra-accurately reproduce the continuous shape on the silicon, since we can round the continuous shape to the nearest available litho width and this does not degrade the uniformity of the current density too much. To demonstrate that, we show a relationship between the maximum deviation error of current density and the number of wire width choices in Figure 5. The interconnect parameters we used to get this curve is the same as those of the above experiments.

3.2 Compare With Uniform Width Wire

We will compare the exponential shape wire of (10) with the uniform width wire in term of chip area, power consumption and signal delay. We assume that the two shape wires are under the same current density bound and have the same load capacitance.

For a uniform wire, the segment at the driving point is the one through which the maximum current flows. Its current density is

$$\frac{I_u(t)}{w_u} = \frac{I_l(t) + \int_0^L V'(t) \cdot c(x) \cdot dx}{w_u} \tag{12}$$

where $I_u(t)$ is the current flows through the driving point of the uniform width wire, w_u is the width of uniform wire and L is the length of the wire.

Equation (5) gives the current density of the exponential shape wire. If we set this to be a current density bound, the minimum width of the uniform wire can be obtained by setting (12) be equal to (5). All the parameters of the two shape wires are assumed the same, thus, the minimum width of the uniform wire, which satisfies this current density bound, is expressed as

$$w_{um} = w_0 \frac{1+\beta}{1-\alpha} \tag{13}$$

where $\alpha = \frac{w_0 c_0 L}{c_l}$, $\beta = \frac{c_f L}{c_l}$.

α should be less than 1, otherwise the current density bound could not be satisfied. Based on the above derivation, we present an experimental result in Figure 6 to illustrate the current density of a uniform width wire and the exponential shape wire. The parameters used in this experiment are the same as those used in the experiments of above subsection.

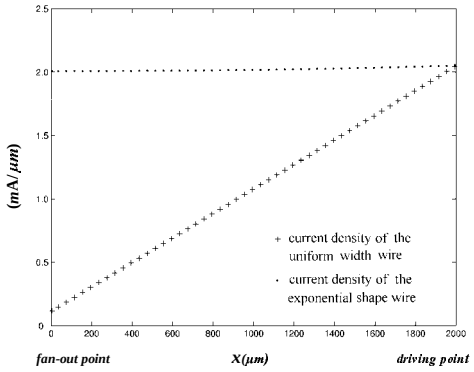

Figure 6. Comparison of current density between the exponential shape wire given by function (10) and a uniform width wire.

3.2.1 Area Comparison

We will compare the area of the uniform width wire with that of the exponential shape wire, considering the two shape wires are under the

same current density bound and all of their other parameters are the same. Let *Au* and *Ae* denote the area of the uniform width wire of (13) and the exponential wire of (10), respectively.

$$\frac{A_u}{A_e}=\frac{\int_0^L w_{um}\cdot dx}{\int_0^L w(x)\cdot dx}=\frac{\frac{1+\beta}{1-\alpha}}{\frac{1}{\alpha}(1+\gamma)(e^{\alpha}-1)-\gamma} \tag{14}$$

where $\alpha=\frac{w_0c_0L}{c_l}$, $\beta=\frac{c_fL}{c_l}$, $\gamma=\frac{c_f}{w_0c_0}$.

Since α<1, we substitute the approximation $e^{\alpha}\approx 1+\alpha+\frac{\alpha^2}{2}$ into (14)

$$\frac{A_u}{A_e}\approx\frac{\frac{1+\beta}{1-\alpha}}{\frac{1}{\alpha}(1+\gamma)(1+\alpha+\frac{\alpha^2}{2}-1)-\gamma}=\frac{1+\beta}{1+\frac{\beta}{2}-\frac{1}{2}\alpha(1+\alpha+\beta)}>1$$

Thus, under the same current density bound, the area of uniform width wire is always larger than that of the exponential shape wire of (10). Substituting the wire parameters used in the above experiments into (14), we get the area ratio is $\frac{A_u}{A_e}=2.99$.

In addition, the ratio of the width of the uniform wire to the maximum width of the exponential wire is

$$\frac{w_{um}}{w(L)}=\frac{w_0\frac{1+\beta}{1-\alpha}}{(w_0+\frac{c_f}{c_0})e^{\alpha}-\frac{c_f}{c_0}} \tag{15}$$

where $w(L)$ is the width of the exponential wire at $x=L$. It is the widest location along the exponential wire.

Taking the same approximation of e^{α} as above, we get

$$\frac{w_{um}}{w(L)}=\frac{1+\beta}{1+\beta-\frac{1}{2}(\alpha^2+\alpha\beta)(1+\alpha)}>1 \tag{16}$$

With the wire parameters used in the above experiments, we get the width ratio $\frac{w_{um}}{w(L)}=1.50$ by using equation (15).

3.2.2 Power Consumption Comparison

Let P_u and P_e denote the power consumption of uniform width wire and the exponential shape wire, respectively. We take the same assumption as in section 2 that the difference of the voltage along the wire is negligible, thus the power consumption is proportional to the total downstream capacitance seeing from the driving point.

$$\frac{P_u}{P_e}=\frac{c_l+\int_0^L(c_0\cdot w_{um}+c_f)dx}{c_l+\int_0^L(c_0\cdot w(x)+c_f)dx}=\frac{\frac{1+\beta}{1-\alpha}}{(1+\gamma)e^{\alpha}-\gamma} \tag{17}$$

where α, β, γ are the same as those in (14).

Taking the same approximation of e^{α} as above subsection, we get

$$\frac{P_u}{P_e}=\frac{\frac{1+\beta}{1-\alpha}}{(1+\gamma)(1+\alpha+\frac{\alpha^2}{2})-\gamma}=\frac{1+\beta}{1+\beta-\frac{1}{2}(\alpha^2+\alpha\beta)(1+\alpha)}>1 \tag{18}$$

With the parameters used in the experiment of this section, we get that the power consumption ratio of P_u to P_e is 1.50. Besides, SPICE simulation shows that the power ratio is 1.44, which is very close to our result.

3.2.3 Delay Comparison

In this subsection, we will first derive the analytical Elmore delay expressions of the uniform width wire and the exponential shape wire, and then give the SPICE simulation results of the two shape wires.

Based on the Elmore delay model, the delay of uniform width wire is

$$\begin{aligned}D_u&=r_d\cdot\left(\int_0^L(c_0\cdot w_{um}+c_f)\,dx+c_l\right)\\&\quad+\int_0^L\frac{r_0}{w_{um}}\cdot\left(\int_0^x(c_0w_{um}+c_f)dt+c_l\right)\cdot dx\\&=r_d\cdot c_l\cdot\frac{w_{um}}{w_0}+\frac{r_0c_lL}{w_0}\cdot\frac{1+\frac{1+\alpha}{2}\beta}{1+\beta}\end{aligned} \tag{19}$$

where α, β are the same as those in (14).

The delay of the exponential shape wire is:

$$\begin{aligned}D_e&=r_d\cdot\left(\int_0^L(c_0\cdot w(x)+c_f)\,dx+c_l\right)\\&\quad+\int_0^L\frac{r_0}{w(x)}\cdot\left(\int_0^x(c_0w(t)+c_f)\,dt+c_l\right)\cdot dx\\&=r_d\cdot c_l\cdot\frac{w(L)}{w_0}+\frac{r_0c_lL}{w_0}\end{aligned} \tag{20}$$

We notice that the first term of D_u is larger than the first one of D_e since we have proved that w_{um} is larger than $w(L)$; and the second term of D_u is smaller than that of D_e since α<1. Therefore, under the same current density, in some cases, the exponential shape wire improves the delay compared to the uniform width wire; in the other cases, the delay of the exponential shape wire is larger than that of the uniform width wire, however, this deterioration is not very distinct since the difference of the second term of D_u and D_e is slight. The SPICE simulations on the 1000 VLSI wires, which we generated in the above subsection, also demonstrate that. With the same parameters used in the experiments of above subsections, the SPICE simulation shows that the delay of the uniform width wire is 56.5*ps* and the delay of the exponential shape wire is 59.1*ps*.

4. CONSIDER WIRE RESISTANCE

When the interconnect becomes unusually long, the wire resistance is needed to take into consideration, and then the voltage of the wire at x is

$$V(x,t)=V_l(t)+\int_0^x I(x,t)\cdot r(x)\cdot dx \tag{21}$$

where $V_l(t)$ is the voltage of the load capacitance. $r(x)$ is the unit length resistance at x and it is given by

$$r(x)=\frac{r_0}{w(x)} \tag{22}$$

where r_0 is the unit square wire resistance.

Substituting (22) into (21), we get

$$V(x,t) = V_l(t) + \int_0^x \frac{I(x,t)\cdot r_0}{w(x)} \cdot dx \tag{23}$$

There exists phase difference between $I(x,t)\big|_{x\neq 0}$ and $I_l(t)$ due to taking wire resistance into consideration. However, we can take the approximation that the phase difference is negligible in most of practical instances. We will demonstrate that this assumption is reasonable later. Thus we can substitute (6) into (23) and get

$$V(x,t) = V_l(t) + \int_0^x \frac{I_l(t)}{w_0} \cdot r_0 dx = V_l(t) + \frac{I_l(t)\cdot r_0}{w_0} x \tag{24}$$

Equation (2) shows that the current $I(x,t)$ is related to the driver waveform since there is a derivative term of voltage with respect to time in its expression. We assume that the waveform of the driver source is sinusoidal to simplify the derivation, and also because any signal can be expanded by Fourier series, in the form of sum of sinusoidal waveforms of different frequencies.

Let $V(x, j\omega)$, $I(x, j\omega)$ represent $V(x,t)$, $I(x,t)$ and $V_l(j\omega)$, $I_l(j\omega)$ represent $V_l(t)$, $I_l(t)$ in the frequency domain, respectively. Based on (24) and (2), $V(x,j\omega)$ and $I(x,j\omega)$ can be expressed as follows

$$V(x, j\omega) = V_l(j\omega) + \frac{V_l(j\omega)\cdot j\omega c_l \cdot r_0}{w_0} x \tag{25}$$

$$I(x, j\omega) = I_l(j\omega) + \int_0^x V(x, j\omega)\cdot j\omega\, c(x) dx \tag{26}$$

Substitute (25) and (11) into (26),

$$I(x, j\omega) = I_l(j\omega) + V_l(j\omega) \cdot \int_0^x \left(1 + \frac{j\omega c_l \cdot r_0}{w_0} x\right) j\omega\left(c_0 w(x) + c_f\right) dx \tag{27}$$

In frequency domain, (6) is expressed as

$$\frac{I(x, j\omega)}{w(x)} = \frac{I_l(j\omega)}{w_0} \tag{28}$$

Substitute (27) into (28), we get

$$c_l + \int_0^x \left(1 + \frac{j\omega c_l \cdot r_0}{w_0} x\right) \cdot \left(c_0 w(x) + c_f\right) dx = \frac{w(x)}{w_0} c_l \tag{29}$$

Differentiate both sides of (29) with respect to x,

$$\left(1 + \frac{j\omega c_l r_0 x}{w_0}\right) \cdot \frac{w_0}{c_l}\left(c_0 w(x) + c_f\right) = \frac{dw(x)}{dx} \tag{30}$$

The left hand side of the equation is a complex function. In most of practical cases, the modulus of the imaginary part is much less than the real part. For example, if ω=6G, c_l=25fF, r_0=0.1Ω/□, w_0=0.25μm, x=1000μm, $\left|\frac{j\omega c_l r_0 x}{w_0}\right|$ is 0.06. Thus, by applying the following approximation to getting modulus of the complex,

$$\sqrt{1+x^2} \approx 1 + \frac{1}{2}x^2 \tag{31}$$

(30) can be rewritten as

$$\left[1 + \frac{1}{2}\left(\frac{\omega c_l r_0 x}{w_0}\right)^2\right] \cdot \frac{w_0}{c_l}\left(c_0 w(x) + c_f\right) = \frac{dw(x)}{dx} \tag{32}$$

Solving this differential equation is straightforward and, with the boundary condition $w(x)|_{x=0} = w_0$, we get the shape function as

$$w(x) = \left(w_0 + \frac{c_f}{c_0}\right) e^{\frac{w_0 c_0}{c_l} x + \frac{\omega^2 r_0^2 c_0 c_l}{6 w_0} x^3} - \frac{c_f}{c_0} \tag{33}$$

Comparing the above shape function with (10), we notice that there is an extra term $\frac{\omega^2 r_0^2 c_0 c_l}{6 w_0} \chi^3$ in the exponent of the shape function. This term is introduced by the wire resistance.

In practice, the term introduced by the wire resistance is negligibly smaller than the first term in the exponent of shape function (33). To show that, we present a comparison in Table 1 by using the typical technology parameters for the Metal 4 interconnects of the manufactory process in different years. The parameters used for the comparison are listed in Table 2. Table 1 shows that the second term in the exponent of the shape function (33) is much smaller than the first term. Thus this term can be ignored and does not degrade the uniform current density result. This infers that the voltage amplitude and phase difference along the wire can be neglected in the usual cases. That is the reason why the shape function (10) derived in section 2 can give very good result of uniform current density without consideration of wire resistance.

Table 1. Results of comparison between the first and second term in the exponent of wire shape function (33)

Technology	$\frac{\omega^2 r_0^2 c_0 c_l}{6 w_0} x^3 \Big/ \frac{w_0 c_0}{c_l} x$
2002	0.017
2005	0.027
2008	0.069
2011	0.086

Table 2. The parameters used in the comparison between the first term and second term in the exponent of (33)

Year	ω (G)	c_l (fF)	r_0 (Ω/□)	w_0 (μm)	x (μm)
2002	12	40	0.1	0.3	2000
2005	20	25	0.2	0.25	1000
2008	36	15	0.36	0.18	600
2011	60	8	0.6	0.12	300

However, when the wire is unusually long, the second term in the exponent can not be ignored since, in this case, it will become comparable with the first term or even become a dominant part in the shape function. We present an experiment to show this case. Taking the same parameters as those used in the experiment of section 3, except that r_0 and the length of the wire are set to be 0.4Ω/□ and 5000μm, respectively, and taking the approximation that the ω of the driver source is the dominant angle frequency in the shape function of (33), we present two experimental results in Figure 7. One curve is the current density of the shape function (10) without taking the wire resistance into consideration and the other one is the current density of the shape function (33) with the wire resistance consideration. We notice that as the length of the wire becomes longer, the equation (33) gives better uniform current density result.

Remark 2:

When we derive the shape function, we take the assumption that the waveform of the driver source is sinusoidal, thus the shape function of (33) works for driver input which is a single frequency sinusoidal

waveform. If the waveform of the driver is not a sinusoid, it can be decomposed into a series of sinusoids of different frequencies, which sum up to the original waveform. As a result, the shape function should be the sum of these shape functions on different frequencies multiplying their normalized Fourier expansion coefficients respectively. If there exist some dominant frequencies in the waveform of the driver source, we may approximately take only the sum of these shape functions associated with the dominant frequencies. We notice that, in figure 7, the curve of the current density under the shape function (33) is not very even. One of the reasons is that we take the approximation that there is one dominant frequency in the signal waveform of the driver source and other frequencies are neglected. Nevertheless, the wire shape function (10) we derived in section 2 does not depend on the waveform of the driver. Thus, this shape function can apply to any input waveform.

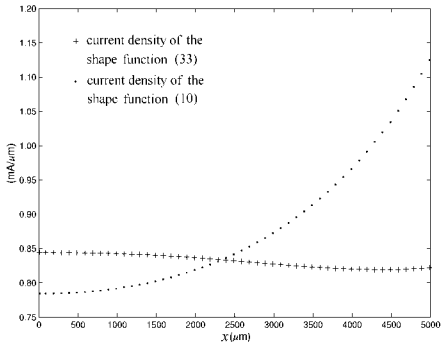

Figure 7. Comparison between the current density of the shape function (10) and that of the shape function (33). All the parameters used in the two shape wires are same.

5. CONCLUSION

To solve the reliability problem due to electromigration, wire sizing is one solution, whose objective is to have the uniform current density and thus uniform lifetime along the wire. In recent years, the driving point of a uniform width interconnect becomes a bottleneck in the reliability problem since the current flowing through this point is the maximum in the wire. Hence, in this paper, we present an analytical wire shape function such that the RMS current density as well as the average effective current density is uniform along the wire. Thus the lifetime is uniform under different electromigration analysis model. In most of practical applications, the wire resistance is not a significant factor in determining the wire shape. If it is not considered in the wire shape function, the uniformity of the current density is not degraded. Moreover, we also derive another analytical wire shape function by taking the wire resistance into account, which is useful when the wire is unusually long. With wide range technology parameters, the uniformity of current density is verified by SPICE simulations.

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