Macromodeling of Digital I/O Ports for System EMC Assessment

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Abstract

This paper addresses the development of accurate and efficient behavioral models of digital integrated circuit input and output ports for EMC and signal integrity simulations. A practical modeling process is proposed and applied to some example devices. The modeling process is simple and efficient, and it yields models performing at a very high accuracy level.

1. Introduction

The development of behavioral models of digital Integrated Circuits (IC) ports is a key resource for the assessment of EMC and Signal Integrity (SI) effects on fast digital circuits. Such an assessment is mainly achieved by simulating the evolution of signals on interconnects and requires accurate and efficient models of IC ports. Behavioral models, that are simplified models obtained from waveforms computed or measured at devices ports, match this requirement.

In this paper we address the development of behavioral models via parametric representations, that have useful advantages. The estimation of such models includes the selection of their structures and automatically takes into account all the effects significantly influencing the relations between the port variables. Besides, the estimation data can be obtained from actual measurement and the accuracy of the estimated model are weakly sensitive to their load conditions. Such a modeling approach is alternative to the widely used approach based on simplified equivalent circuits (*e.g.,* see the Input/output Buffer Information Specification (IBIS) [1]), and can be usefully exploited to achieve high accuracy levels. In addition, such models can be estimated directly from transient measurement on real devices.

Modeling processes are proposed for both input and output ports and are applied to some example commercial devices.

2 Drivers models

The modeling of a digital IC output port (*driver* hereafter) via a parametric model amounts to relate its port voltage and current by a suitable parametric equation. The equation (or model representation) must be nonstationary, in order to take into account the port logic state and state transitions. Different model representations are possible, yet we obtain the best results by using the following discrete-time piecewise representation:

$$i_{\rm out}(k) = w_1(k) f_1(k) + w_2(k) f_2(k) \qquad (1)$$

where $i_{\rm out}$ is the output port current expressed as a combination of two submodels f_1 and f_2 with weight coefficients w_1 and w_2. Submodels f_1 and f_2 describe the behavior of the driver when its output is in the High and Low logic states, respectively, whereas w_1 and w_2 describe state switchings. Submodels f_1 and f_2 are nonlinear dynamic parametric models based on the theory of Radial Basis Functions (RBF) [2]. They are linear combinations of gaussian functions whose arguments are the past r samples of the port current $i_{\rm out}$ (r is named the dynamic order of the model), and the present and past r samples of the port voltage $v_{\rm out}$. Each basis function is properly centered in the vectors space of the voltage and current sequences and depends on the distance of the actual sequences from the center.

The above Piece-Wise RBF (PW-RBF) model (1) arises systematically as an approximation of the actual behavior of digital drivers and stems from the properties of such devices and of the RBF representations [3]. Piecewise model structure is also typical of other behavioral modeling approaches (*e.g.,* see IBIS), which however are based on simplified equivalent circuits justified by empirical considerations.

The estimation of model (1) is carried out by a simple procedure [3] and is done by matching the output of the model to the output of actual drivers for suitable input signals. Port voltage and current waveforms involved in the estimation of parametric models are named *identification signals*. Submodels f_1 and f_2 are obtained via effective estimation algorithms [4, 5] whereas the weight coefficients w_1 and w_2 are estimated by linear inversion of (1) when v and i are replaced by sampled waveforms recorded on two different loads (*identification loads*) during the Up (Low-to-High) and the Down (High-to-Low) state switchings. The

last part of the modeling process is the implementation of the estimated PW-RBF models (1) in a circuit simulation environment, like SPICE, by means of an equivalent circuit. This is achieved by converting equation (1) into a continuous time state-space model and by synthesizing it via RC circuits with controlled sources.

This modeling process has been developed and validated by applying it to several virtual and actual devices [6, 3]. Besides, it has been successfully applied to the modeling of commercial IBM drivers and receivers [7, 8].

3 Receivers models

The development of behavioral models for input ports ($receivers$ in the following) is rather straightforward because, in contrast with output ports, their operation is hardly influenced by the IC internal states.

For input port voltages in the range of power supply, receivers exhibit a mainly linear capacitive behavior, whereas outside such a range their behavior is dominated by the nonlinear protection circuits. This property and the physical structure of receivers suggest the following model representation

$$i_{\rm in}(k) = i_l(k) + i_{nl}(k) \qquad (2)$$

where $i_{\rm in}$ is the current flowing into the input pin, and i_l and i_{nl} are a linear and a nonlinear submodel, respectively.

As a linear submodel we use an AutoRegression with eXtra input (ARX) parametric model [9] defined by the linear combination of the present sample of the port voltage $v_{\rm in}$, and the past r samples of $v_{\rm in}$ and $i_{\rm in}$ (again r is the order of the model). Submodel i_l is estimated by standard routines [10, 5] from suitable identification signals, that are obtained by driving the receiver with a voltage waveform composed of few steps and spanning the range of the power supply, in a region where the port behavior is nearly linear.

The nonlinear submodel i_{nl} is split into two contributions

$$i_{nl}(k) = i^u_{nl}(k) + i^d_{nl}(k)$$

where i^u_{nl} and i^d_{nl} are RBF parametric models [2] that account for both the nonlinear static and dynamic behavior of receivers. Submodel i^u_{nl} [i^d_{nl}] is estimated by standard routines [4, 5] from identification signals obtained by driving the receiver with a multilevel voltage waveform whithin the port voltage range where the effects of the up [down] protection circuit cannon be neglected.

It is ought to remark that a simple receiver model (the $i - v$ model hereafter) composed of a shunt capacitor $C_{\rm eq}$ and a shunt nonlinear resistor belongs to the class defined by (2), as well. In fact, a capacitor and a nonlinear resistor are the simplest i_l and i_{nl} submodels taking into account both the static and dynamic behavior of receivers. However, it can be verified that a $i - v$ model gives only a rough approximation of the receiver behavior. A better accuracy can be achieved by using for (2) the parametric model discussed above and defined by a linear ARX submodel and nonlinear RBF submodels.

As a last step of the modeling process, the estimated parametric models (2) are turned into equivalent circuits and implemented as SPICE-like subcircuits by following the same procedure described in Section 2.

4 Validation examples

In this section, we show some validation examples highlighting the accuracy of the proposed drivers and receivers models. The example models are estimated from the responses of the detailed transistor-level models (*reference* models hereafter) of the modeled devices and involve a commercial driver and some high speed IBM devices.

Example 1: The first modeled device (MD1) is a commercial low-voltage CMOS driver, namely the `74LVC244`. For this device, a transistor-level model (typical values of components) is available from the vendor, as well as an IBIS data set (version 2.1) including slow, typical and fast cases, that take into account the spreading of parameters due to the manufacturing process.

From the transistor-level model of MD1, we built a PW-RBF model (1), that turns out to have a dynamic order $r = 1$ and submodels f_1 and f_2 composed of 10 and 15 basis functions, respectively. From the IBIS data set, we also built a typical, a slow and a fast IBIS model. All the above models are then implemented as SPICE-like subcircuits in order to compute their responses by using the same simulation environment.

In order to compare the accuracy of the PW-RBF model and of the IBIS models in predicting the actual behavior of MD1, we use a validation setup composed of an ideal transmission line ($Z_0 = 100\,\Omega$, $T_d = 0.5$ ns) driven by MD1 and loaded by a 1 pF capacitor. Figure 1 shows the MD1 port voltage response $v_{\rm out}(t)$ predicted by the PW-RBF model and by the three IBIS models when the driver performs a Low-to-High transition (bit pattern `"01"`). From this Figure, it is clear that the PW-RBF model turns out to be very accurate and could be safely used to replace the transitor-level model. However, IBIS models may lead to poor predictions, even if the parameter spreading is considered.

Example 2: The second modeled device (MD2) is a CMOS driver (power supply: $V_{ss} = 0$ V, $V_{dd} = 1.65$ V) used in IBM mainframe products. The PW-RBF model estimated for MD2 has dynamic order $r = 1$ and its submodels f_1 and f_2 are composed of nine basis functions.

As a validation test, Figure 2 compares the responses of MD2 when it applies a 4 ns pulse (bit pattern `"010"`) to three ideal transmission lines, with different characteristic

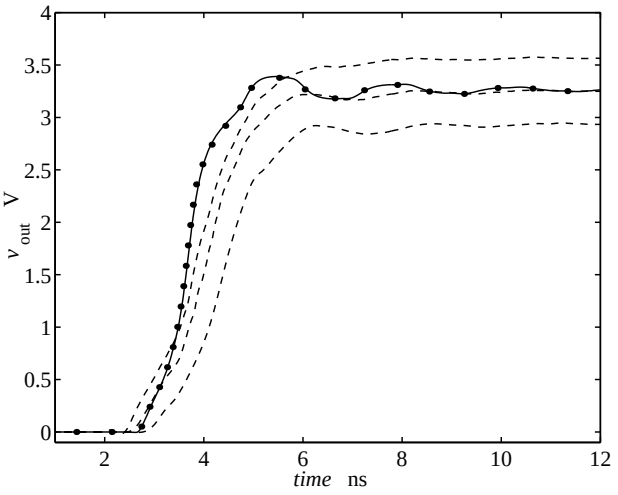

Figure 1. Near end voltage waveform $v_{\rm out}(t)$ on an ideal transmission line ($Z_0 = 100\,\Omega$, $T_d = 0.5$ ns) driven by MD1 and loaded by a 1 pF capacitor. Solid line: reference; dotted line: PW-RBF model; dashed lines: fast, typical and slow IBIS models.

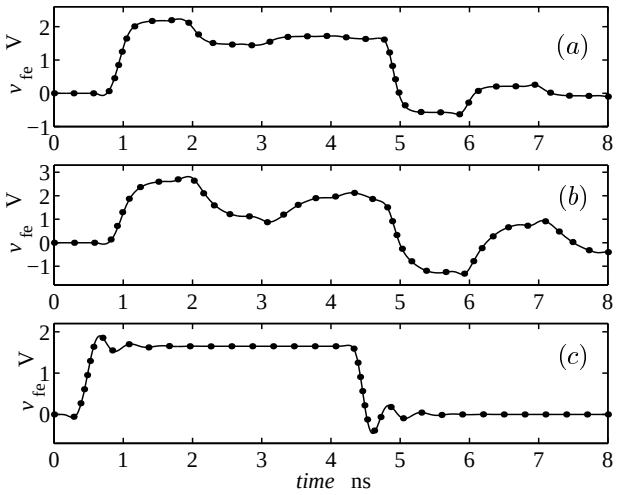

Figure 2. Far-end voltage waveform $v_{\rm fe}(t)$ on three ideal transmission lines driven by MD2. Solid lines: reference; dotted lines: PW-RBF model. Panel (a) refers to a line with $Z_c = 50\,\Omega$, $T_d = 0.5$ ns; (b) $Z_c = 100\,\Omega$, $T_d = 0.5$ ns; (c) $Z_c = 100\,\Omega$, $T_d = 40$ ps.

impedance and time delay values, terminated by a 1 pF capacitor. The accuracy of the PW-RBF model in reproducing the reference behavior of MD2 for generic dynamic loads can be clearly appreciated.

Example 3: The third modeled device (MD3) is another IBM CMOS driver ($V_{ss} = 0$ V, $V_{dd} = 1.5$ V). The PW-RBF model estimated for MD3 has dynamic order $r = 1$, and nine and six basis functions in submodels f_1 and f_2, respectively.

Figure 3 shows the validation setup devised for this example. It is based on a three-conductor lossy on-MCM interconnect (2 lands + reference plane) driven by two MD3 devices and terminated by 1 pF capacitors. The device on land `#1` is active and sends a train pulse (bit pattern `"011011101010000"`), whereas the device on land `#2` remains quiet in the Low logic state (bit pattern `"000000000000000"`).

Figure 4 shows the far-end voltage waveforms $v_{21}(t)$ and $v_{22}(t)$ on both the active and the quiet land of the setup. This third comparison highlights that also the far-end crosstalk signal, which is a sensitive quantity, can be carefully predicted by using PW-RBF models.

Example 4: The fourth modeled device (MD4) is a receiver ($V_{ss} = 0$ V, $V_{dd} = 1.8$ V) used in the same series of IBM products as those of the previous two examples. For MD4, we estimate the two different models outlined in section 3: the simple $i - v$ model ($r = 1$, $C_{\rm eq} = 3$ pF) and the parametric model (ARX submodel i_l with dynamic order $r = 3$ and RBF submodels i^u_{nl} and i^d_{nl} with dynamic orders $r = 3$ and $r = 2$, respectively).

As a first validation, devised to stimuate the nearly linear behavior of the receiver, we drive a MD4 by the series connection of a $5\,\Omega$ resistor and an ideal voltage source with a trapezoidal waveform (amplitude=1 V, transition time=100 ps). Figure 5 shows the $i_{\rm in}(t)$ waveform computed with the reference model and the two estimated models for this validation. The gain of accuracy of the parametric model can be clearly appreciated.

As a second and more realistic validation test, we use a 10 cm long lossy transmission line loaded by the MD4 and driven by the series connection of a $30\,\Omega$ resistor and an ideal voltage source with trapezoidal waveform. The pulse duration is 2 ns, the transition times are 100 ps long, and the amplitude of the pulse is set to $A = 1.8$ V $A = 2.2$ V and $A = 2.8$ V, in order to explore the nonlinear region of input voltages. Figure 6 shows the $v_{\rm in}(t)$ waveform computed by the reference model and by the $i - v$ and the parametric models. The accuracy of the proposed parametric model in both the linear and nonlinear region is clearly appreciable.

5 Accuracy and efficiency

From the validation curves of the previous section, the reader can appreciate the good accuracy of the proposed

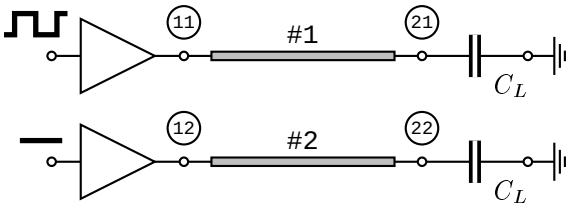

Figure 3. Coupled-line structure for the realistic test case of Example 3 (length 0.1 m, $l_{11} = l_{22} = 0.441\,\mu$H/m, $l_{12} = l_{21} = 14.4$ nH/m, $c_{11} = c_{22} = 144$ pF/m, $c_{12} = c_{21} = -1.38$ pF/m, dc resistance $24.4\,\Omega$/m, skin effect coefficient $11.7\,10^{-6}\,\Omega\,\mathrm{s}^{-1/2}$/m, dielectric loss factor $2.5\,10^{-3}$, $C_L = 1\,pF$)

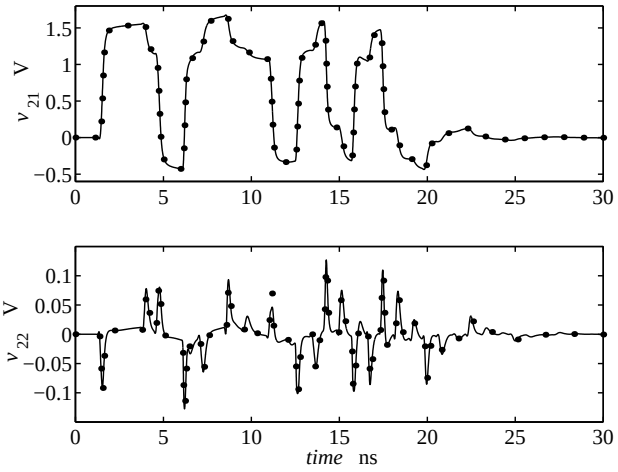

Figure 4. Far-end voltage waveforms $v_{21}(t)$ and $v_{22}(t)$ on the active and quiet line of the structure of Fig. 3. Solid lines: reference; dotted lines: PW-RBF model.

drivers and receivers models. In all experiments we ran so far, we found timing errors between our model and the reference always less than 20 ps (in most cases, the timing error is 5 ps), being $T_s = 10 \div 50$ ps the sampling time used in the estimation process. Such timing errors are obtained by computing the maximum delay between the reference and the model responses measured at the crossing of a suitable voltage threshold.

Besides, the proposed parametric models can be generated at low cost and their numerical efficiency is fairly good. The CPU time required by the estimation of the models of the previous section is some ten seconds on a Pentium-II PC @ 350 MHz. Simulation times for the generation of the curves of Fig. 4 are compared in Tab. 1 (same CPU). As a rule of thumb, the obtained models for both drivers and receivers are more than 20 times faster than the original transistor-level models.

Driver Model	CPU time
Transistor level	34.7 sec
PW-RBF	1.4 sec

Table 1. CPU time comparisons for the simulation of the coupled structure shown in Fig. 3.

6 Conclusion

This paper addresses the development of accurate and efficient behavioral models of both input and output ports of digital ICs. The proposed approach is based on the estimation of nonlinear parametric models from port current and voltage waveforms. The obtained models perform well on high speed actual devices. Their cost of generation is low and they can replace transistor-level models for the simulation of realistic EMC problems without appreciable loss of accuracy.

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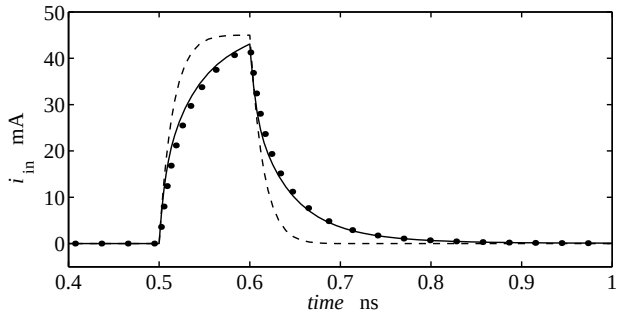

Figure 5. Model responses for a receiver driven directly by an equivalent source (see text). Solid line: reference response; dotted line: parametric model; dashed line: $i - v$ model.

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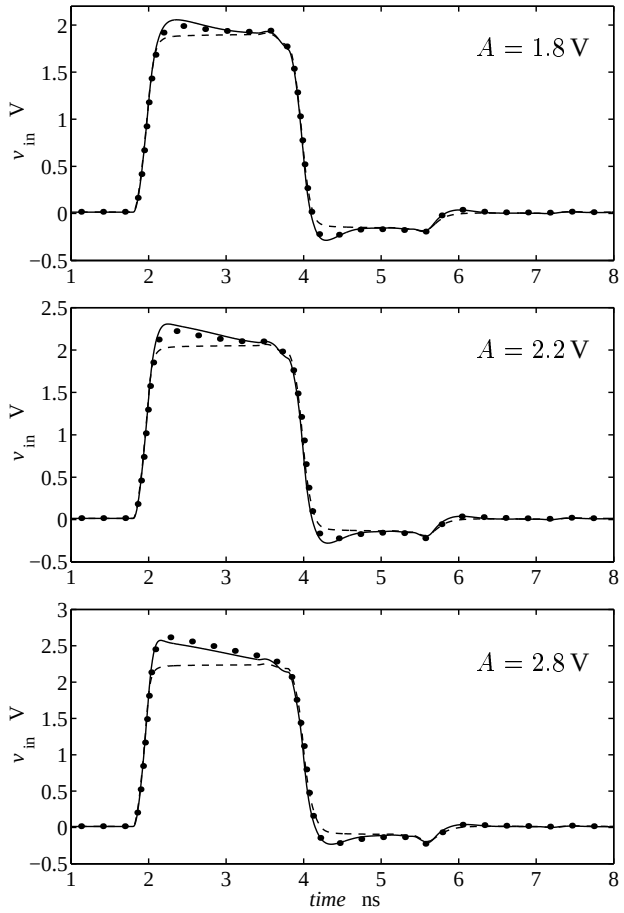

Figure 6. Far-end voltage waveforms on a 10 cm long lossy transmission line loaded by MD4 and driven by the series connection of a $30\,\Omega$ resistor and an ideal voltage source producing a pulse whose amplitude is A. Solid lines: reference; dotted lines: parametric model; dashed lines: $i - v$ model.