Built-in Dynamic Current Sensor for Hard-to-Detect Faults in Mixed-Signal ICs

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Abstract

There are some types of faults in analogue and mixed signal circuits which are very difficult to detect using either voltage or current based test methods. However, it is possible to detect these faults if we add to the conventional dynamic power supply current test methods I_{DDT}, the analysis of the changes in the slope of this dynamic power supply current. In this work, we present a Built-In Current Sensor (BICS) which is able to process the highest frequency components in the dynamic power supply current of the circuit under test (CUT). The BICS add to the resistive sensor an inductance made from a gyrator and a capacitor to carry out the current to voltage conversion. Moreover, the proposed test method improves the fault coverage in continuous circuits and switched current circuits as well.

1. Introduction

More than a decade ago supply current test was introduced as a very promising technique to test CMOS circuits. The Iddq testing has been proved to be effective in digital CMOS circuits, nevertheless, most of the test methods valid for digital circuits cannot be easily applicable to analogue and mixed signal circuits.

The high cost associated with production and the field test of complex mixed signal VLSI circuits make attractive the alternative to simplify the test equipment moving some or all the tester functions onto the chip. This highlights the advantages of the fault detection method based on built-in current sensors.

There have been many proposals of current sensors for digital, analogue and mixed signal circuits that may be classified by the type of sensing devices: resistive sensors [1],[2],[3] or capacitive sensors [6],[7], by the type of measurement: direct, such as sensors based on current mirrors [4], or indirect, such as sensors based on current to voltage converters[5], current to frequency converters or current to delay time converters.

As the power supply current Idd can be defined by its two elements, Iddq-quiescent current and Iddt-transient or dynamic current, many published papers in the last years have dealt with the design of sensors specialised in both types of current detection. Nevertheless, there are hard-to-detect faults in continuous time circuits and also in switched analogue circuits that need an improvement in the detection methods to enhance their fault coverage.

Catastrophic models include short and opens as most of the defects that exist in CMOS IC mixed signals circuits, however, open defect, the open source/drain or the floating gate, can generate complicated fault effects and sometimes are difficult to detect with the direct measurement of the power supply current.

A method to detect most of the hard-detection faults (opens and shorts) in analogue circuits will be presented in this paper as well as a new sensor that can improve the fault coverage including these faults among the detected ones. The methods will be applied not only to continuous time, but also to switched analogue circuits.

A sensor that not only detect the transient Iddt-current but also different slopes of this transient current supply in the presence of hard faults may improve the fault coverage when these types of faults exist in the analogue circuits.

In the paper we present the design of a sensor relying on the voltage drop across a resistance, induced by the dynamic power supply current, in order to generate the fault signal. This current is captured in the sensor through a current mirror. However, when there are hard faults in continuous time and switched current analogue circuits (SI), whose effects may be detected through the slope of the dynamic power supply current [8], the design of the sensor has been modified to be capable of detecting these changes in current supply due to the circuit faults as an additional method to enhance the fault coverage of the test process.

This last operation of the sensor gives greater specific weight to the higher frequency components of the current. Thus, an inductive rather than a resistive load is used to carry out the conversion of the current sampled in the CUT to a voltage. To design the inductive load a simplified structure of a gyrator and a capacitor is used, made up of four transistors.

To evaluate the efficiency of the proposed method in switched and continuous time circuits, a fault analysis is performed by simulation using as benchmark circuits an integrator based on a S^2I memory cell and a continuous time filter [9] based on operational amplifiers.

The paper is organised as follows. Section 2 describes some of the most difficult to detect faults in continuous time and switched current circuits obtained by simulation in the benchmark circuits. Section 3 describes the resistive dynamic current sensor and explains how the BICS is coupled to the benchmark circuits. Section 4 describes circuit emulating the behaviour of the inductance to build the enhanced sensor. Section 5 describes the fault

evaluation process and some simulation results are shown in order to verify the efficiency of the test approach. Finally, some conclusions are presented.

2. Hard faults in analogue and mixed circuits

The catastrophic fault model considered includes shorts between the gate and the source/drain of the transistors, together with opens in the source/drain contacts[11]. However it has been reported that the floating gates are important faults within transistor opens[12]. In this work it has been considered that all the faults have the same probability of occurrence. The catastrophic transistor level fault model has been used for the fault simulation. The shorts are modelled by a 100Ω resistor.

The open faults are modelled by a 10MΩ resistor in parallel with a 1fF capacitor. Although in [13] it has been demonstrated that the open gate defect strongly depends on the technology and physical topology of the circuit, this widely-used model helps the convergence of the electrical simulator and the repetitive results obtained can be used to evaluate the efficiency of the proposed test methodology.

Nine different faults of gate oxide short (GOS) between gate and bulk for each NMOS transistor, and three GOS faults for each PMOS transistor have been considered [14], which cover the range from the hardest to the softest situation of GOS, corresponding to three values of R_s (1Ω, 1KΩ, 1MΩ) and K (0.1, 0.5, 0.9). In addition, we have included four fault conditions for the passive components of the operational amplifier.

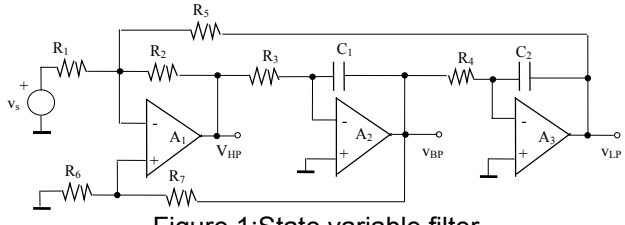

Figure 1:State variable filter

In continuous time analogue circuits testing the state variable active filter is suggested in [9] as a benchmark circuit. This circuit includes three interconnected operational amplifiers. The stimuli necessary to detect the faults through a dynamic current test must be pulses in the input of the filter, so that current transitions appear in the supply current produced by the changes in the input signal. A purpose-built sensor must detect these changes and convert them into the go/no go output of the test.

If we apply the catastrophic fault model to the Operational Amplifiers, figure 2, appearing in the filter, it is possible to analyse by simulation the difficulty of detecting the short and open faults in the circuit by dynamic supply current analysis. In this way, in the transistors of the input differential amplifier M_1 and M_2 of the operational amplifier, the short and open faults are detected by Iddt analysis with a resistive sensor. However, the open faults of the other two transistors appear as hard-to-detect faults since this sensor does not detect them.

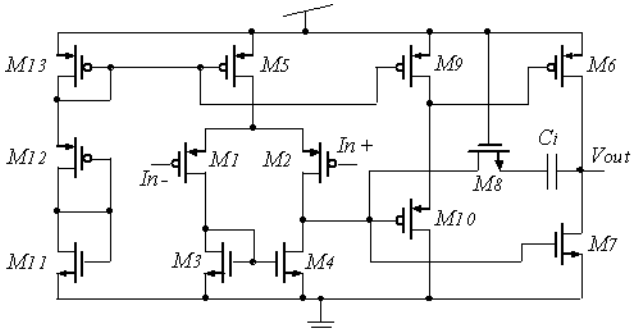

Figure 2: Operational Amplifier

It will be necessary to redesign the sensor so that all the faults of the input differential amplifier are covered by this test method of dynamic supply current analysis.

In figure 3 we show a cascode S^2I current memory cell consisting of two pMOS transistors and another two nMOS transistors which make up the fine and coarse current memories respectively. This type of memory cells significantly reduces the most frequent errors in the SI cells [7], and so it has been chosen for the development of this work

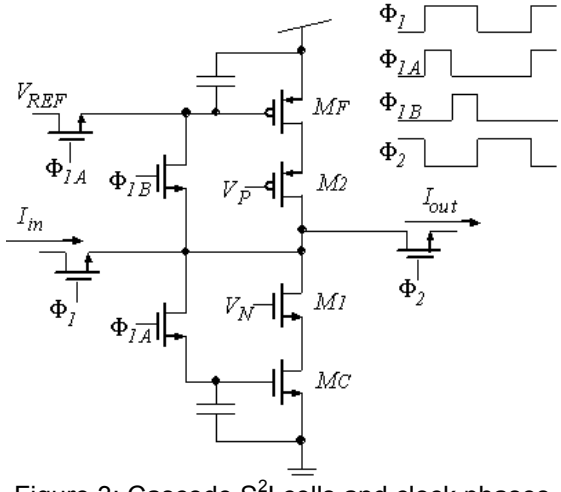

Figure 3: Cascode S^2I cells and clock phases

The experimental evidence shows that shorts faults are generally detected with a resistive dynamic sensor, with some exceptions such as the drain-source short in the cascode transistors, which will be considered as hard-to-detect faults.

This cascode S^2I cell can be applied to the design of any of the most common basic building-blocks, such as amplifiers, integrators, etc.

It is possible to carry out the switched-current circuit test based on this method of capturing dynamic current signals if we take into account the different clock phases in the working of these circuits and the different currents which circulate in the storage transistors of the memory cells of the SI circuit.

It is also necessary to fix the type of stimulus to be applied at the input in order to detect the presence of a fault. As in the case of continuous circuits, it is necessary

to apply a pulse at the input to provoke a transient at the output, in this type of circuit, the changes in clock phase are taken advantage of, and so, it is sufficient to apply a constant signal at the input to be able to detect the presence of a fault.

Given that our chosen method of fault detection is the analysis of current transients that are produced after the change of the different clock phases, ϕ_{1a}, ϕ_{1b}, ϕ_{2a} and ϕ_{2b}, there are four critical time intervals where fault-free and faulty circuits can be distinguished by transient current analysis.

The advantage of switched-current circuits, compared to continuous-time circuits, is that they are discrete systems in time and it is precisely in the instants when the voltage changes that we measure the dynamic current. These voltage changes can be due to changes in input current or, as in our case, due to the phase changes in the clocks of the circuits. In this way we introduce a constant current signal at the input and analyse the instants after the clock phase changes.

3. Resistive dynamic current sensor

In analogue continuous-time circuits a dynamic supply current coupling method has been proposed based on a current mirror and taking advantage of the parasitic capacitance associated with these structures[1].

In figure 4 a resistive sensor has been implemented in an operational amplifier. This sensor reproduces the dynamic current through the analogue circuit, by means of an additional branch of the current mirror placed in parallel to a biasing branch of the CUT. The test circuitry converts this current into a binary voltage.

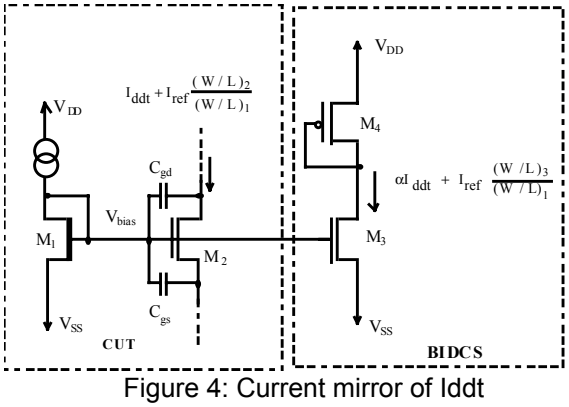

Figure 4: Current mirror of Iddt

The relationship between the Iddt in the CUT and the Iddt captured by the additional branch is shown in figure 4 and it depends not only on the MOS parameter design, but also on the biasing-dependent parameters of the capture transistor M_2 (g_m, r_0). However, the dynamic characteristics also depend on the parasitic capacitances of the transistor M_2 (C_{gs},C_{gd}).

If we consider the cascode S^2I cell in figure 3 there are two currents, which can be measured by use of the dynamic current sensor. These are the currents in the fine and coarse memory respectively. So, it is not possible to predict if the presence of a fault in the circuit we are considering is going to be detected in the fine or in the coarse memory. According to this there are two possible configurations for the sensor, which include an analysis of the transient current.

In any case, these two configurations can be converted in a single one by the use of switches, in such a way that during one clock phase the current in the fine memory is measured, and in the other phase the current is measured in the coarse memory. Consequently, it will be necessary to carry out the test during a time interval of two clock periods to detect the presence of a fault in the circuit.

If we only measure the absolute value of the current, in the second of the cases mentioned above the fault could not be detected [7]; however, thanks to the incorporated dynamic sensor it is possible to detect the presence of the fault.

As the current captured may increase or decrease in the faulty circuits, with reference to the fault-free one, we have designed a sensor that detects the current's upper and lower limits. This has been designed, as shown in figure 5, to detect the presence of a fault when there is an increase or a decrease of the current consumption, and so, there are some faults that cannot be detected. Therefore, if there is no fault in the circuit, at the output there should be 5V, while if there is a fault, the output should be 0V either during one clock phase or during the two periods when the test is carried out.

The upper and lower limits of the captured current are detected by the sensor as abnormal currents in the presence of a fault

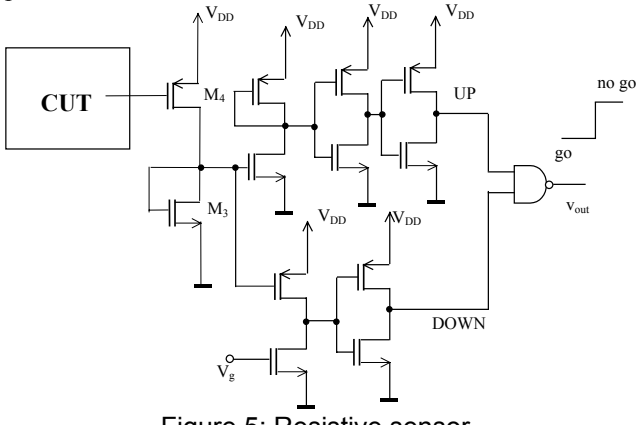

Figure 5: Resistive sensor.

Most of the faults are detected in the sensor that captures the drain current in the coarse memory MOS transistor. Nevertheless some faults are not detected, especially the short drain-source in cascode transistors M_1 and M_2.It is possible to detect this type of faults if we consider the dynamic current in the coarse memory MOS transistor. In this case the slope of the dynamic current is different in the fault free circuits and in the faulty circuit.

It could be possible to redesign the sensor to detect this type of faults if we consider the response of the sensor to dynamic currents.

4. Slope sensitive dynamic current sensor

The built in current sensor (BICS) proposed for the detection of the hard faults in the CUT is based on the analysis of the slope of the dynamic power supply current. Therefore, it is necessary to design a circuit which presents a frequency dependency, in such way that the circuit amplifies the highest frequency components most. This is the behaviour of a series circuit composed of a resistor and an inductance connected to ground.

The method used to implement inductances inside an integrated circuit, emulates the inductance with a gyrator circuit built from CMOS active devices.

The gyrator can also be implemented with an active circuit based on OVAS or OTAS. However, this approach is expensive in terms of silicon area and power consumption. Moreover, the limited bandwidth of the components reduces the circuit frequency range.

Our approach is based on the inverted back-to-back connection of the active devices to implement the basic gyrator behaviour. The transconductance sources are done with two transistors, a NMOS (M_0) and a PMOS (M_1), connected as it is shown in figure 6. Transistor M_2 biases M_0 and M_1 in the saturation region. The capacitor is achieved by means of the gate-source and gate-drain capacitance of a NMOS transistor, $C = C_{gs3} + C_{gd3}$.

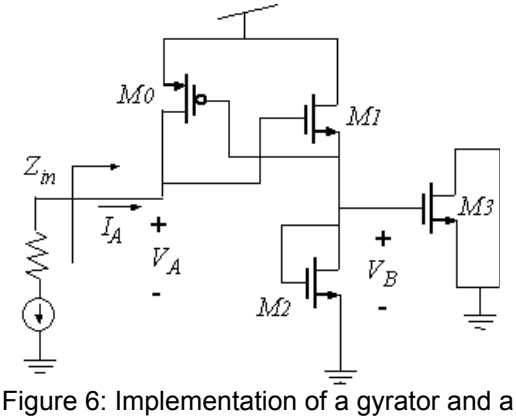

Figure 6: Implementation of a gyrator and a capacitor using active devices.

The model of this circuit can be approximated by an ideal gyrator that consists of two transconductance stages, (g_1 and g_2). It transforms a capacitor C inserted at the output port into an inductor L at the input one:

$$L = \frac{C}{g_1 \cdot g_2} \qquad (1)$$

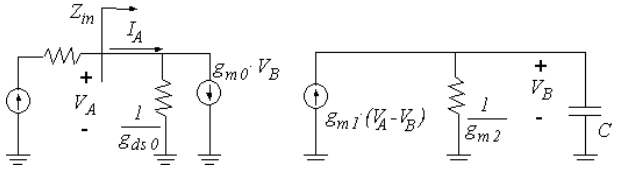

Figure 7 Small signal model of the circuit in figure 6 without stray capacitances.

The admittance seen from port A is given by;

$$Y_{in} = g_{ds0} + \frac{g_{m0} \cdot g_{m1}}{g_{m1} + g_{m2} + sC} \approx \frac{g_{m0} \cdot g_{m1}/(g_{m1} + g_{m2})}{1 + sC/(g_{m1} + g_{m2})} \qquad (2)$$

This function, unlike the ideal inductance, presents some characteristics that affect the circuit performance.

a) Inductance value. The admittance at high frequencies comes reasonably close to an inductance.

$$Y_{in}(s \to \infty) \approx \frac{g_{m0} \cdot g_{m1}}{s \cdot C} \qquad (3)$$

b) Series resistance. The admittance does not have an infinite value for frequencies close to zero. It is necessary to add a series resistance to the ideal inductance model. The resistor value is

$$Y_{in}(s \to 0) \approx \frac{g_{m0} \cdot g_{m1}}{g_{m1} + g_{m2}} \qquad (4)$$

This means that the sensor not only detects the high frequency components of the dynamic current, but also maintains the information given by the quiescent current.

c) Parallel resistance. The minimum value of the admittance function is limited by the output admittance of the M_0 transistor above a few (1/MΩ).

d) Bandwidth. At low frequencies, the circuit emulates a degenerate inductance, so the denominator has a pole at

$$Pole = -\frac{g_{m1} + g_{m2}}{C} \qquad (5)$$

On the other hand the parasitic capacitances of the transistors, of the circuit in figure 1, must be included to analyse the circuit at high frequency. In this case the circuit model deviates from the ideal inductance and new poles and zeros appear. This determines the upper frequency limit of the sensor operation.

e) Maximum value of L. The capacitor value is limited to a few picofarads due to the physical size of the transistor. A W=15µm and L=25µm transistor has a gate-drain capacitance plus a gate-source capacitance of about 1 pF, in Alcatel MIETEC 0.7 micron technology.

In order to sample the power supply current of the CUT, the BICS adds an additional branch to a current mirror of the proposed benchmark circuits to replicate the current. The sampled current is converted to voltage using the gyrator of figure 6 as a load.

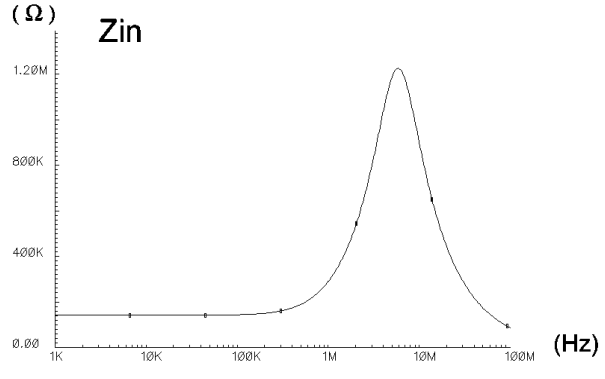

Figure 8. Circuit impedance versus frequency

Figure 8 shows the transfer function of the impedance, seen from the point where the current to voltage conversion is done. This circuit has a great sensitivity to the high frequency components of the current waveform.

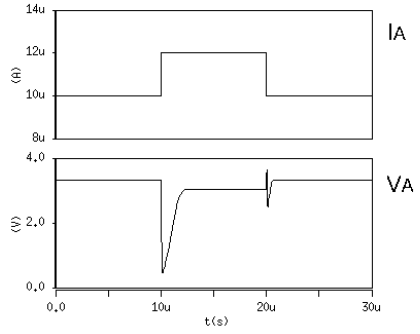

Figure 9. Relation between current and voltage at the gyrator input

Figure 9 shows a simulation of the gyrator, where a two microampere change in the input current over a ten microampere DC current (upper graph) produces an abrupt voltage change at the input of the gyrator (lower graph). The change in the quiescent voltage, after the current stabilisation, is smaller and it is given by low frequency impedance.

The greater sensitivity of the current to voltage conversion, when the BICS uses an inductive instead of a resistive load, can be appreciated in figure 10.

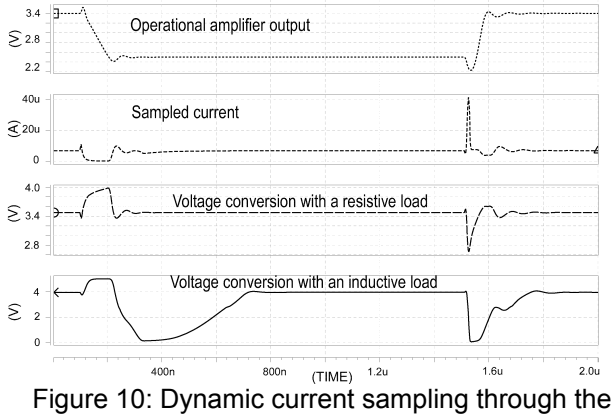

Figure 10: Dynamic current sampling through the differential stage of an operational amplifier

The figure 10 waveforms correspond to a simulated operational amplifier configured as a voltage amplifier. This circuit will be used later as a part of a benchmark circuit in order to evaluate the goodness of our proposal of test approach. The upper waveform is the output voltage of the operational amplifier. The second signal is the sampled current, a copy of the dynamic current through the differential stage. The third waveform is the voltage after the current conversion is done by a resistive load. The last one is the same voltage but with an inductive load, built from the circuit in figure 6, instead of a resistive load. In the last case the bigger voltage variations help in the processing of the current information.

5. Fault evaluation of the test approach

The simulations have been carried out, both on the operational amplifier and on the S^2I cell. The parameters measured were: the voltage /V_a, obtained from the conversion of the current with an inductive load using the gyrator described, and the voltage obtained from the conversion of this current with a resistive load.

In this way, the value of the two parameters will determine the presence of a fault in the dynamic stage and/or in the static stage of our sensor, respectively.

In the operational amplifier case, the conversion was done on the current flowing in the differential stage, while in the S^2I cell it was done on the current flowing in the fine memory during one clock phase and that flowing in the coarse memory during the next phase.

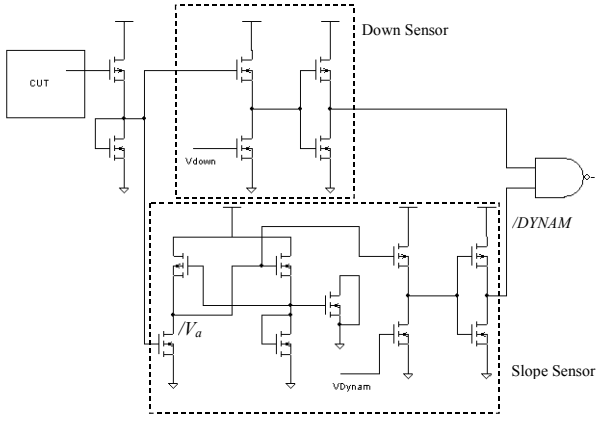

Figure 11. Dynamic sensor in the S^2I cell.

On the other hand, it was established that, in the case of those faults provoking an increase of the static state current, the dynamic stage of the sensor is equally effective for their detection. For this reason, the stage determining the upper limit of the current in the original resistive sensor can be eliminated, as shown in figure 11, both for the case of continuous and S^2I circuits.

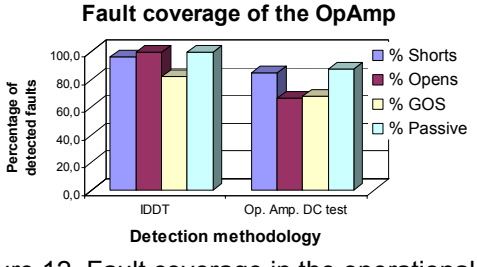

Figure 12. Fault coverage in the operational amplifier

Figure 12 shows the fault coverage obtained in the operational amplifier simulation. The detected faults are classified according to their type (shorts, opens, GOS and passive components) and the detection methodology applied. Our transient current test approach *IDDT* is shown in the left-hand columns and the operational amplifier DC test voltage *Op. Amp. DC Test* in the right ones.

The sensor detects 95% of the simulated shorts, 100% of the simulated opens and 82% of the simulated GOS in the operational amplifier. The IDDT test approach has a greater fault coverage than the DC voltage test, since some faults, especially opens and GOS, do not produce appreciable changes in the DC biasing voltages of the transistor gates, but modify the higher frequency components of these voltages as they introduce delays in the propagation paths of the signals.

Focusing, for example, on the Drain or Source Open faults, the following table was obtained. It shows, for each type of fault of the simulated transistors, the stage of the dynamic sensor, which carries out the detection, and whether it is produced during the up-slope of the input pulse, or during the down-slope.

TRANSISTORS	FAULTS	Slope Sensor		Down Sensor	Both Sensors
		Input up-slope	Input down-slope		
M1	Drain open	¬	¬	v	v
	Source open	¬	¬	v	v
M2	Drain open	¬	¬	v	v
	Source open	v	¬	v	v
M3	Drain open	v	v	¬	v
	Source open	v	v	¬	v
M4	Drain open	¬	v	¬	v
	Source open	¬	v	¬	v
M5	Drain open	¬	¬	v	v
	Source open	¬	¬	v	v
M6	Drain open	v	¬	¬	v
	Source open	v	¬	¬	v
M7	Drain open	¬	¬	v	v
	Source open	¬	¬	v	v
M9	Drain open	v	¬	¬	v
	Source open	v	¬	¬	v
M10	Drain open	v	¬	¬	v
	Source open	v	¬	¬	v
M13	Drain open	v	v	¬	v
	Source open	v	v	¬	v

√ Detected
¬ Non-detected

Table 1.Open Faults in the operational amplifier.

The numbering of the transistors in Table 1 corresponds to Figure 2, which describes the operational amplifier used in the simulations.

As can be seen in Table 1, some of these faults are only detectable using a sensor based on the current slope and not only in the current consumption, given that, in these cases, this consumption is only 1µA greater than the fault-free circuit, and is even identical in some occasions. Nevertheless, the different slope appearing in the faulty circuit with respect to the fault-free case allows us to detect the fault with a dynamic sensor.

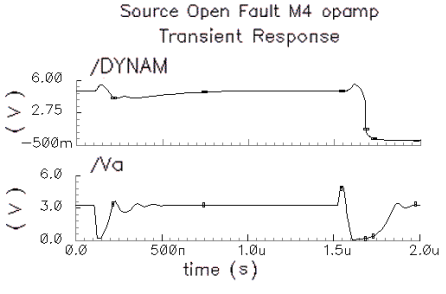

Figure. 13. Output of the dynamic stage and voltage V_a.

This is the case, for example, of the transistor M_4, figure 13, belonging to the current mirror of the differential stage. This example is different from the rest as the detection is produced during the down-slope of the input pulse, given that, during the up-slope, the value of V_a is very similar to the fault-free circuit, both in the Drain Open and Source Open cases.

It should also be mentioned that in the last transistor in the table M_{13}, the dynamic current consumption increases with respect to the fault-free case, both in the Drain Open and in the Source Open, so that these could be detected using a resistive type sensor which fixes an upper limit for this current, although, as mentioned previously, the stage of our sensor which analyses the supply current slope is also capable of detecting these effects. However, it should be highlighted that these faults cannot be considered as only detectable using the slope analysis.

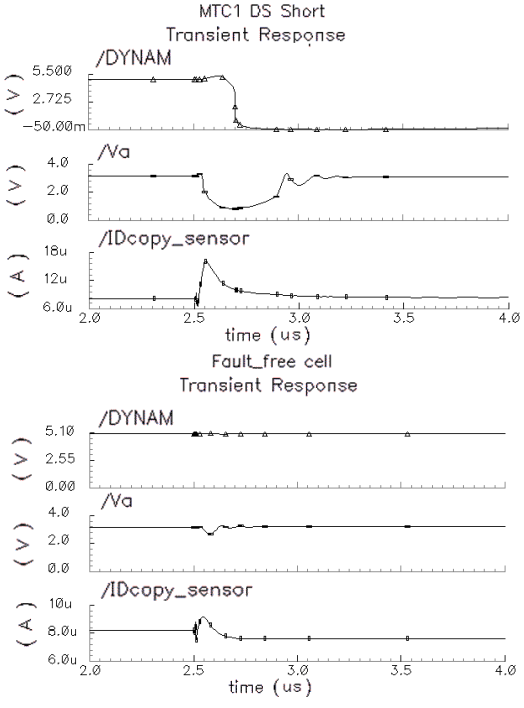

Figure 14. Output of the dynamic sensor in the faulty and fault-free circuits.

In the simulations carried out on basic S^2I cells, the use of a resistive sensor, which detects when the current consumption in the memory is greater or less than some determined limits, permits a coverage of 90% of the faults, considering Short and Drain and Source Open faults in the transistors of the fine and coarse memories of the cell, without taking into account the faults in the switches. Two faults still have to be detected: the Drain-Source Shorts in the cascode transistors of both memories. These faults do not produce variation in the current consumption, but can be detected due to a modification of the slope of the dynamic current with respect to the fault-free case figure 14.

The slope stage added to the original static sensor permits, not only the detection of the remaining faults, achieving a 100% coverage in the previously mentioned faults, but moreover, it gives rise to the elimination of the part of that sensor which detected the upper limit of the current consumption, thus simplifying the design and reducing the sensor area.

MEMORIES	TRANSISTORS	FAULTS	Sensor fine	Sensor coarse
		DG short	¬	v
		GS short	v	v
	MC	DS short	v	v
		Drain Open	v	v
COARSE		Source Open	v	v
MEMORY		DG short	v	v
		GS short	v	v
	M1	DS short	¬	v
		Drain Open	v	v
		Source Open	v	v
		DG short	v	v
		GS short	v	v
	MF	DS short	v	v
		Drain Open	v	v
FINE		Source Open	¬	v
MEMORY		DG short	v	v
		GS short	¬	v
	M2	DS short	¬	v
		Drain Open	¬	v
		Source Open	v	v

√ Detected
¬ Non-detected

Table 2. Detection of faults in the S^2I cell.

If we extend the fault detection procedure, valid for operational amplifiers and S^2I memory cells, to the proposed benchmark circuits, the S^2I integrator and the state variable filter, the results obtained by simulation are different in the two cases.

In the integrator case, any fault in the first S^2I cell is reflected in the transistors of the second cell, and viceversa. Moreover, the faults detected in the S^2I integrator are the same as those appearing in an isolated cell. It can be concluded, therefore, that the behaviour observed for a single cell is repeated for combinations of this cell. In this way, the presence of a fault produced in one of the cells of the benchmark circuit can be detected by dynamic current analysis in any of the other cells. By applying the test to the S^2I integrator, the same fault coverage is obtained as in the case of the isolated cell.

Nevertheless, in the case of the continuous-type benchmark cell, it is observed that a single open-type fault does not produce the same response in all the operational amplifiers of the circuit. In fact, the faults are not reflected in the same way in the transitory currents of the rest of the operational amplifiers.

However, it has been proved by simulation that the test methodology based on the analysis of the dynamic current is still valid for fault detection. The configuration of the sensor described for the isolated operational amplifier detects the open-type faults of the first of the operational amplifiers of the filter. For each one of the remaining operational amplifiers it is necessary to use an individual sensor for each operational amplifier, with adjustments to the configuration for each case.

This leads us to two alternatives: the use of individual sensors for each operational amplifier of the filter, all working at the same time; or else, the use of a single sensor which adjusts its settings for different clock cycles. In other words, we have to choose between an increase of the area of the sensor or an increase of the time necessary to carry out the test of the complete circuit.

6. Conclusions

This paper presents a test approach based on the analysis of the dynamic power supply current.

We propose the use of BICS in order to sample the current transients of the CUT.

The sensor has been designed with the aim of prioritising the information obtained from the higher frequency components of the current over the information provided by quiescent current. For this reason an inductance has been implemented as a loading element of the current to voltage conversion circuit. This voltage is digitised to get digital pulses at the sensor output, that indicates the existence or not of a fault in the CUT.

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