IEEE 1394a_2000 Physical Layer ASIC

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Abstract

CN4011A is IEEE 1394a_2000 standard Compliant Physical Layer ASIC. It is a 0.18um mixed-signal ASIC incorporating three analog ports, PLL, reference generator for analog along with the digital control logic. Whole ASIC from specification to GDSII including analog was designed at Controlnet (I) Pvt. Ltd

CN4011A has three 1394a_2000 fully compliant ports that support data transfers at 100/200/400 Mbps. It supports repeating of data over on all ports other then receiving port. It's Interoperable with other 1394a_2000 compliant Physical Layers and fully Compliant with 1394a_2000 Link Layer and OHCI.

The ASIC operates on a single 24.576 MHz external crystal oscillator. The Internal PLL generates 400MHz Clock. This Clock is divided to get the clocks required for the Internal logic and to transmit and receive data at 100/200/400 Mbps over the serial interface and over the Link Interface.

1.   1394a_2000 Overview

IEEE-1394a_2000 is a high performance serial bus. It has multi-master and live connect/disconnect (hot plugging) capability. Standard cabling connectors on interconnect cabling and dynamic node address allocation as nodes are added to the serial chain. Another feature is that transmission speed is scalable from approximately 100 Mbps to 400 Mbps with 1394a-2000. Each node also acts as a repeater, allowing nodes to be chained together to form a tree topology. Due to the high speed of 1394, the distance between each node or hop should not exceed 4.5m and the maximum number of hops in a chain is 16, for a total maximum end-to-end distance of 72m. Cable distance between each node is limited primarily by signal attenuation. An inexpensive cable with 28-gauge signal pairs can be up to 4.5 meters long. The most widely separated nodes must have 16 or fewer cable hops between them. This gives an end-to-end distance of 72 to 224 meters.

2.   CN4011A- The ASIC

The CN4011A is a three-port 400Mbps IEEE 1394a_2000 Compliant Physical Layer. Each Port incorporates two differential line transceivers for transmitting and receiving data over the serial bus. It also incorporates circuitry for detecting connection and disconnection of devices. Each cable port is capable of transmitting and receiving data at 100, 200 and 400 Mbps. It also incorporates a standard interface to carry out efficient data transfer with the Link Layer.

The ASIC requires an external 24.576 MHz crystal as reference. The external oscillator drives an internal Phase-Locked loop (PLL), which generates the 393.216 MHz reference clock. A 49.152 MHz clock signal is derived from the 393.216 MHz reference and provide to the Link Layer and used for the resynchronization of the received data.

3.   ASIC Architecture

The ASIC is partitioned into three major blocks.
* The Analog Block
* The Low Speed Digital Block
* The High Speed Digital Block

The Analog Block
The Analog portion constitutes of the three IEEE 1394a_2000 compliant ports (differential transceivers-LVDS), PLL and Reference generator.
The ports have differential drivers for driving the "data" and "strobe" signals over the "TPA+/-" and "TPB+/-" differential pairs as per the IEEE 1394a_2000 standards. The port also provides a "tpbias" driver, which drives the "tpbias" output appropriate voltages. The port receives "data" and "strobe" signals from the "TPA+/-" and "TPB+/-" lines and provides digital levels. The port incorporates arbitration comparators and provides digital representation of the line status. Speed comparators are implemented in the ports, which decode the current on the line to determine the speed of the packet. The port

provides a constant current source and connect detect circuit to determine the connection status.

The PLL provides the reference 393.216 MHz clock derived from an external 24.576 MHz Crystal oscillator.

The Reference Generator provides the required current and voltages required by the analog block.

The High speed Digital Block

The high-speed digital block works on 393.216 MHz clock. The major functions of the block is encoding and transmitting the data and receiving and decoding the data. This transmitter in this block serializes and performs the data-strobe encoding on the parallel data received from the Link Layer.

The clock is recovered from the received data. The received data is decoded, de-serialized, and forwarded to the Link Layer. The receiver in this block implements FIFO's for PPM compensation of 100ppm as specified by the IEEE 1394a_2000 standards.

The Low speed Digital Block

The Low speed Digital Block carries most of the control functions of the ASIC. This block incorporates Arbitration Controller, Phy-Link Interface Controller, and Port Connection Controller and implements the Phy-Register Stack.

The Arbitration Controller forms the heart of the system and controls the operation of the ASIC during bus initialization and also after that for normal data transfers. This logic performs operations like Initiating/Detecting Bus Resets, Tree Identification and Self-Identification process and Normal Arbitration process. Every time a new device is added to the system or an existing device is removed from the system, the Arbitration Controller resets and reconfigures itself automatically.

The Phy-Link Interface Controller Interfaces with the Link Layer as per the Phy-Link Interface standards. It decodes the link requests and forwards these requests to the Arbitration Controller for packet transmission or Register Stack for register read/write. This block accepts data form the Link Layer to be transmitted over the bus and forwards it to the High speed Digital Block for transmission. It receives data from the High speed Digital Block and forwards the data to the Link Layer. This Block also performs the function of status (bus reset, subaction gap and arbitration reset gap) and register transfer to the Link Layer.

The Phy-Register Stack maintains all the registers defined by the IEEE 1394a_2000 standards. This block accepts register read/write requests from the Link Layer and appropriately returns/updates the registers. The Phy-Link Interface also decodes the Phy-Packet. It maintains the
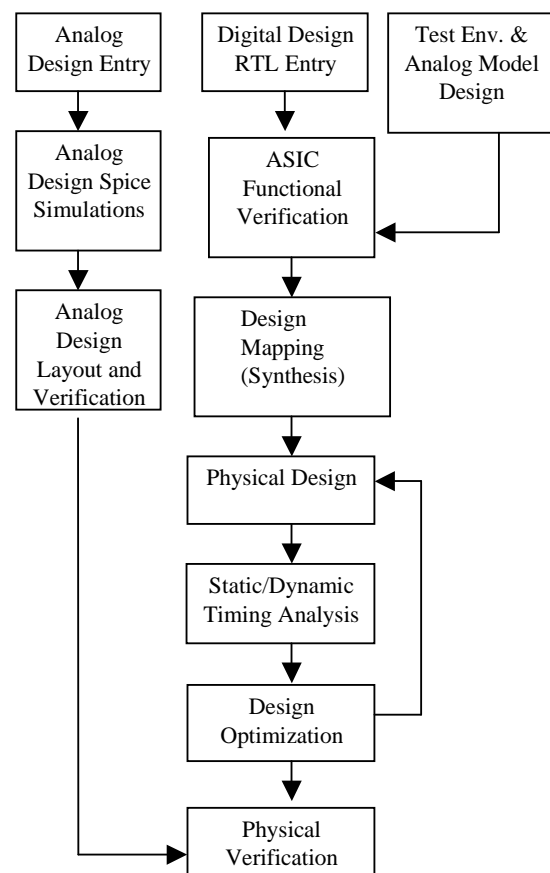
Phy-Packets and transmits Phy-Packets whenever required.

ASIC Block Diagram
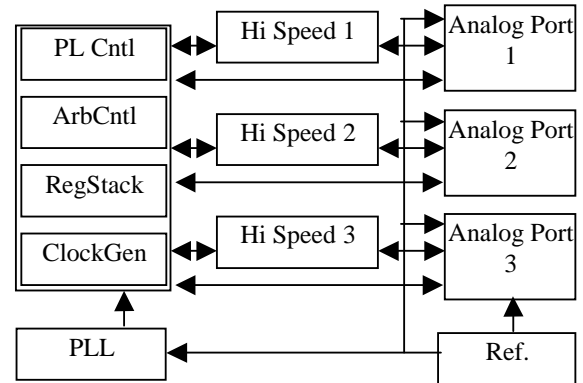
4. Design Flow

The Design Flow stages are illustrated below:

1. Digital Design Entry:

The Low speed and High speed blocks were designed in Verilog HDL. Verilog Models were developed and used for the functional verification of the ASIC. The Test Environment development involved designing a Link Layer Controller for verifying the Phy-Link interface of the ASIC. A Line controller was designed for forcing/analyzing symbols on the 1394 bus. This Line controller was used to verify the ASIC's basic functionality. For rigorous testing the ASIC were connected back-to-back and simulated for functionality and compliance with the standards. Standard Verilog simulation tools were used for Functional verification

2. Analog architecture and Design:

This Analog portion of this chip is designed to deliver 1394a signals over a STP cable. The 1394a standard defines the cable characteristics as well as the termination scheme. The standard lists down the limits for the differential and common voltages that can be transmitted over this medium. These limits had to be translated in form of specifications for various drivers and receivers that interfaces with the physical medium

While design, all the blocks were grouped into
- Those operating on line common mode voltage
- Those operating on line differential mode voltage

The specification for category '1' were defined first and then they were used like constraints to define the specifications of category '2'. This was done because the line common mode voltage influences the design of all the blocks. The same is not true in case of differential voltage.

The standard also list the line impedance conditions, these were taken into account while writing the specifications. In general all the limits imposed by the standard of the type 'min.' were overrated by 10%, while that of the type 'max.' were de-rated by 10%. Once the specifications were defined their inter-relationship was verified by writing a behavioral model in HSPICE.

The design requires several DC voltages for common mode voltage comparators. Also all the blocks need to have identical biasing conditions. For this a Band gap reference block is used. The band gap output voltage is fed to two linear transconductors. One uses a external precision resistor, while the other an internal polysilicon resistor. These currents obtained thus are distributed throughout the chip to the Analog blocks. Had the voltage been distributed instead of current then the voltage drop along the interconnect length would have caused a problem. The currents from the transconductor with an

external precision resistor are used for biasing, while the ones form the internal poly resistor are used to generate the required DC voltages. The variations in the on-chip resistors will track each other and thus the generated DC voltage won't shift, inspite of resistor value variation.

All the receiver, whether differential or common mode, are interfaced to the cable such that only their gate terminal connects to the line. This way very high impedance is presented by these receivers and they will not cause any line imbalances.

The supply for PLL, Reference Block and the Analog port are different. This helped in avoiding noise coupling from the high speed switching taking place in the Analog port.

There's a provision for turning off specific blocks in the Analog Port. This helps in reducing power consumption

The signal which the data receiver gets over from the physical medium can be noisy. To avoid spurious detection of signals a 30mV hysteresis has been built into the data receiver.

The arbitration comparator is supposed to detect a difference of around 125mV between the lines. The arbitration comparator shifts one of the line voltages by 125mV by driving current through a resistor with one of its terminals connected to the line whose voltage is to be shifted

For simulation of Analog portion The actual spice model for the 1394a cable was used to test the Analog portion of this chip. The Analog portion of this design has been checked for TT, FF, SS process, 0 to 70 deg. C and 10% supply variations. While simulating the Analog portion of the design, bond lead inductance was also taken into consideration

3. Digital Design Mapping (Synthesis)

The Digital Design was carried out using Standard cells methodology. The Verilog RTL was mapped to TSMC 0.18u CMOS technology using standard synthesis tools. For Analog blocks timing models were used. The Design was partitioned into one block (high speed) and top. The block was optimized separately.

4. Physical Design

The Physical Design was carried out using Hierarchical flow. The ASIC had the following blocks at Top: Analog Port (3.No), Reference Block, PLL, and High Speed where as the Low speed was distributed on Top. Abstracts and Timing models were developed for the Analog Blocks. The Digital Design Physical Design was carried out using the Standard cells timing driven P&R flow. The routing rules for High speed were modified so as the parasitics do not hamper the timing after P&R. The parasitic for the high speed block and for full chip were

extracted for timing analysis. The design required one optimization on the top for meeting the timings.

5. Post Layout Verification

After the parasitic extraction the ASIC was verified with the netlist and back annotated timing. The Static Timing analysis was performed with the back annotated extracted parasitics.

6. Analog Design Layout

Before layout floor planning was done to ensure critical blocks face the same environment, less noise coupling and isolation.

Layout for analog was full custom handcrafted. Different micros(pcells) were created to ease the layout process such as MOS transistors, cascode structures, resistors, MOS capacitors. proper matching techniques like common centroid method were followed so that off sets are reduces to best possible extent. Analog blocks were isolated from digital blocks using proper wide guard rings

7. Physical Verification

The high speed blocks was first checked and cleaned for DRC/LVS/Antenna. Then the Full chip was integrated merging the Analog blocks. Checking and cleaning the chip for DRC/LVS/Antenna then carried out full Chip verification.

5. Design Issues

The major design issues related to the design are as follows:

- **Design of a 0.18u Mixed Signal ASIC:**

Design a Mixed Signal ASIC is an issue to be dealt with very carefully. These issues crop up from the start of the design. A model of analog is required for modeling the behavior of analog for functional verification of the ASIC. The Integration of at the Physical level imposes extra efforts as compared to any other designs. In architecture phase itself proper partitioning was done between analog and digital blocks. All signals and their characteristics were defined between analog and digital.

- **Design of 400Mbps Differential transceivers on 0.18u Technology:**

Design of Differential drivers/receivers to work at 400MHz is a critical task. Layout of the design at such high frequencies is a challenge itself.

The type of signaling 1394 engages into requires four different types of receiving circuitry.

The single differential receiver is used when the transmission is unidirectional. The maximum data transfer rate, which this receiver can detect, is 400MBPS and at this speed the differential voltage can be as low as 100mV. The LS differential receiver is used when the transmission is bi-directional, i.e. during arbitration. The arbitration signaling is at low speeds and the signal is a three level signal. The HS common mode voltage detector is a comparator that detects the speed signal. It compares the line common mode voltage with a set of predefined voltages. This comparator stabilizes in less than 40ns after the input has changed. The LS comparator uses the common mode voltage to sense the connection status of the peer device.

Signal Type	Module	Functionality
Differential HS	Differential Receiver	Data Receiver
Differential LS	Differential Receiver	Arbitration Detector
Common Mode HS	Common Mode Voltage detector	Speed-Signal Detector
Common Mode LS	Common Mode Voltage detector	Connect Detector.

Four types of drivers are needed to support 1394 signaling standard.

Signal Type	Module	Functionality
Differential HS	LVDS Driver	Data Transmitter
Common mode LS	Common Mode Voltage Driver	TPBIAS Generator
Current	Current Sinks	Speed Signal
Current	Current Source	Connection Status

The differential driver drives a STP with matched terminations. This is a current driver and generates LVDS level differential voltages. These voltages are centered around a common voltage. The differential voltage has to meet the tight rise/fall time specifications bound by the EMI standards lower side and signal speed on the higher side. This driver pumps 4mA current into the terminations. The differential voltage generated has a

nominal value of about 220mV with a 0.6ns rise/fall time. The highest speed is of course 400 Mbps.

Common mode voltage driver generates a PVT stabilized common mode voltage. The stability of this voltage is necessary for proper functioning of all the other modules. The current sinks of the peer PHY draw the current mainly from this module. This voltage source needs to stabilize within 2% of its nominal value in less than 0.1ms. The Current sinks are used to sink the current from the peer. The amount of current sunk in determines the speed of signal termination. These current sinks sink in a current of 12 mA in 100ns.

- **Design of 400MHz PLL on 0.18u Technology:**

Main challenge in designing PLL was to get low jitter and noise influence on clock. PLL generates 400Mhz clock for High Speed logic with the Input reference clocks is of 24.576 MHz. Most complex block in PLL was VCO, Its ring oscillator type with 5 stages. Others issue was coupling of noise from supply to output clock. To avoid this noise filter logic was put between VCO supply and standard supply

- **Analog Block Layout:**

The layout of the Analog portion posed following challenges:
- 1> Matching of Data & Strobe Portions.
- 2> Digital To Analog Isolation
- 3> Minimizing Substrate coupling from high-speed Analog blocks to Low speed Analog blocks.
    - a) Latch Up.
    - b) Noise coupling through substrate.
- 4> Specialized I/O and ESD protection.

The Analog block is floorplanned in such a way that the high speed/high current drivers are in proximity of the I/O region. This ensures that the substrate noise elements are grouped together. The high speed current drivers are heavily guard ringed to avoid latch-up. Each Analog module in the design has a guard ring around to isolate the substrate of that module. This guard ring is in the form of a "p" ring connect to GND and an "n" ring connected to the supply. The differential lines are laid out in a separate Metal layer to minimize the cross talk.

The Data & Strobe modules were laid out in mirrored fashion. The length and shape of TPA/TPB pairs are identical.

Common centroid matching technique has been used wherever possible. A substrate/well contact per 5 microns has been added as rule; this was done to prevent the body effect. Dummy elements were added to minimize the boundary effects/loading.

The whole Analog portion has a guard ring around it. The width of this guard ring is more than 3 contacts wide.

Around this guard ring there's a floating NWELL ring. This floating NWELL ring along with the guard ring forms a face-to-face connected diode combination. This gives maximum isolation from the noise getting coupled from the digital side.

The I/O cells have an ESD protection, which can withstand HBM level of ESD, zaps. Each of the signals is VCC and VSS clamped to dirty VDD and VSS respectively. The size of the ESD devices are chosen such that they do not toss the load condition on the differential lines at the same time give adequate ESD protection.

The digital and Analog supply/ground are different. The supply/ground of the reference block as well as that of the PLL is different from the Functional Analog block.

- **Timing Convergence for the Digital Logic at 400MHz and its P&R:**

As the feature size is reducing the parasitics effect the timing conversion of ASIC. The RTL is designed to have a very low logic on 400MHz. For a 400MHz on 0.18u, special care had to be taken for P&R so that the parasitics do not hamper the timings drastically.

- **Implementation of Complex 1394a_2000 Physical layer arbitration protocol and timing parameters involved State Machines:**

The IEEE 1394a_2000 Physical Layer employs an intelligent arbitration functions. Implementation of Specification to RTL so that the ASIC Complies with the standard demands for a higher level of abstraction than usually followed in RTL. Also mapping the various timings specified by the standard require extra consideration while designing.

- **RTL Implementation for a generic code so that the same design can be upgraded to more ports (*n*PORT-Phy) i.e. a design with configurable no of ports:**

Implementing RTL in a generic way so that the RTL can be configured for the no of ports poses another challenge. Generalizing parameters impose extra efforts in designing as well as functionally verifying the ASIC.

- **Development for a complete test suite for verifying the ASIC functionality:**

For Functional verification of the ASIC a Link Model has be designed. The ASIC's major verification was carried out with connection the designs interfaced with the Link Layer Models. Configuring the test bench manually seemed laborious and scripts were developed to automatically configure the test benches. Large number of

test cases had to written for thoroughly verifying the design functionality. The Port Connection timing parameters are in the order of milliseconds. Simulation of these requires large time especially on netlist simulations. To solve this extra signal were define which will reduce this timing while doing simulation, this reduced simulation time considerably . For functional verification code coverage was used to get areas which required to verified also it give measure of verification activity done.

6. Features

Following are the major features of the ASIC
- Fully Compliant with IEEE 1394 and IEEE 1394a_2000 standard.
- Operates on a single 24.576 MHz clock to transmit and receive data at 100/200/400 Mbps over the serial interface and over the Link Interface.
- Supports 1394a_2000 arbitration enhancements like Multi-speed Concatenation, Fly-By Concatenation, Acknowledge Accelerated Arbitration, and Arbitrated Short Bus Reset. Includes Connection Debounce, Port Suspend/Disable/Resume.
- Incorporates Data Strobe Encoding/Decoding for data transmission and Reception over the serial bus.
- Received Data resynchronized on local clock.
- 80 Pin QFP Package.

Die Plot

7. ASIC Information

CN4011A is a Mixed Signal ASIC. The ASIC is in the foundry and expected in the third quarter of 2001. Following are the details:

Technology:	TSMC 0.18u
Operating Voltages:	3.3/1.8V
Operating Frequency:	400/50 MHz
Die Size:	126.5 X 119 mils
Package:	80 Pins QFP
Part No.:	CN4011A