Low Power Solution for Wireless Applications

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***Abstract*—Low standby power dissipation is the primary need for most of the wireless applications for prolonged battery life. Traditionally ASIC solutions currently address either high density or high performance requirements and to some extent power to cater to the needs of a variety of customers. The solution needs to be improved further for the power considerations specifically. This paper describes how the ASIC solution for high density can be tuned to get a low power library. The strategy involves changing the length of all the mosfets in all the core cells in the library. This solution decreases the leakage power by atleast 3X. This paper also describes about the performance and area impact of the low power library compared to the high density library. Unlike the other approaches such as multi Vt, this approach is very cost effective since it neither involves any changes in the fabrication process nor does it require extra masks and hence this is the most suitable and quick solution for the wireless applications..**

***Index terms*—CMOS, 2.5G, 3G, Multi-Vt**

I. INTRODUCTION

Wireless applications demand low voltage, low power and high speed of operation. The core designs have scaled to low voltage process technologies over time which inherently addresses the need for wireless to some extent in terms of power. The threshold voltages have been scaled in the past [9], [10] to obtain a high circuit operation speed. But the price to be paid is in terms of leakage current. This is the reason why portable battery-driven systems, where large portions of circuits remain in standby mode for long duration, have been reluctant to use this solution. With 2.5G and 3G wireless market picking up, they cannot afford to compromise on speed and they are very concerned about the power consumption from the point of view of battery-life than chip heating and hence the need for mixing solutions for power and density without compromising speed, in the same chip.

There are numerous ways to address low power solutions – a) supply voltage scaling. Reducing the power supply voltage gives the largest factor of power reduction, but has a disadvantage of degradation of operating speed due to reduced average transistor on-drive currents b)Multi-Vt [3] [4], which uses low Vt [2] for fast circuit operation and high Vt for reducing leakage power. Though this is a very good solution, it calls for changes in the fabrication process and flows to support these transistors in the same die. One more issue with this solution is, the inability of the synthesis tools to take advantage of these cells and simultaneously optimize for timing and leakage power static probabilities c) Self adjusting threshold CMOS [1]. Controlling the threshold voltage by exploiting the body effect of MOS devices reduces the leakage current significantly. But this solution does not work in deep-submicron process, due to the Vt variations with the process scaling d)Clock gating idle units provides needed reduction in power, but this has a limitation because it calls for changes in the flow and tools which are existing currently. We have discussed only a few solutions here, but there are many more ways[6] [7] which we compared this solution with.

We want a solution which addresses the low power requirements, which does not call for any changes in the masks or fabrication process since the cost incurred due to this cannot be absorbed in this cost sensitive market for just addressing the power issues. Thus we looked at this solution of changing the channel lengths which will be a rapid and cost effective product development solution to address the power requirements.

In this paper we describe the strategy followed to reduce static power, the implications and results. In Section II we describe the approach followed, while section III presents the impact. In Section IV we present the conclusions and results.

II. ‘ DELTA *L*’ METHODOLOGY

Static power is a product of supply voltage and leakage current(1)

$$P_{static} = I_{leak} * VDD \quad \ldots\ldots(1)$$

Leakage current [5] is a complex equation(2) which is a function of threshold voltage, W and L of MOSFET [12]

$$I_{leak} = Iso' * W/L(1-exp(-Vds/Vt) * Exp(Vgs-Vt\_Voff/n.Vt) \quad \ldots\ldots\ldots\ldots(2)$$

Where *Iso'* is a function of various process parameters like mobility of electrons, surface

potential, oxide thickness etc., From equation (2) it is apparent that by increasing the channel length L, the leakage current can be reduced and hence the static power of a circuit. The sub-threshold current [11] decreases as the channel length is increased due to the exponential relationship between the current and the potential barrier in the sub threshold region. If the channel length is increased, the static power decreases(Fig.1), the average power increases(Fig.2) due to the capacitances increase and the operating speed degrades slightly(Fig.3) because the drive current reduces.

Hence we decided to change the channel length of the MOSFETS. We have discussed how we went about to study the impact of channel length increase on power, both static and dynamic and performance in terms of average delay.

We took a sample set of 20 cells from a standard cell high density library and changed the channel length from *L* to (*L* + *min grid),* where '*min grid'* is the manufacturing grid. We did the layout for these cells after changing the channel lengths to quantify the area impact. We used the layout migration tool to migrate the existing layouts done using a channel length of *l* to get the new layouts. Since this migration does not involve any topological changes to the layout, we could get the migrated layouts in a very short time. The layout generated through this method is correct by construction and of production quality. Thus the comparison of cell area was accurate.

The two circuits were simulated using SPICE (circuit with channel length *L* and circuit with channel lengths as *L* + *min grid)*. We took various critical paths from production designs and simulated those paths with both set of cells, with unchanged channel length and changed channel length and then compared the rise time, fall time and average delay. For measuring the effect on the leakage and dynamic power, we took the same critical paths as testcases. We also looked at the trend on various parameters like delay power with channel lengths varying from L to L+2*min grid

III. IMPACT

A. Area Impact

Area impact on a cell by cell basis is shown in the Table.1

Area of the cell is directly proportional to 'W/L' of a transistor. But the chip level area is not a direct linear function of either 'L' or cell level area.

From the table(Table.1) it is apparent that we are not affecting the die size of the chip significantly. Only 2 out of the 20 cells shows an increase in the width and the increase is by just one routing grid. These 20 cells we took as testcases are a representative set of cells for a high density library. The increase in die area due to only few cells is acceptable if we consider the cost, effort and cycle time involved in implementing this strategy. More over if we have to apply any other design techniques instead of this strategy, we have to compromise on the area by a significant amount. Considering all this, the area impact this strategy gives is very less. To understand the area effects at the chip level, we collected data on the usage of the cells in terms of number of instances and area occupied by each cell in the chip, across various designs and process nodes. We found that the cells which will increase in area if the channel lengths are increased, constitutes only 5% of the die. If the average increase in number of grids is from 5 to (5+1), then this results in only ~1.5% increase in die area assuming a worst case utilization of 100%.

Cells	*Impact*
Inverter, 1x	No Impact
2 i/p NAND	No impact
Buffer, 1x	No impact
4:1 mux	No impact
EXOR, 1x	1 grid increase
Inverter, 2X	No Impact
2 i/p AND, 1x	No Impact
4:1 mux, inv o/p	No Impact
Boolean	No Impact
Buffer, 7x	1 grid increase
Boolean	No Impact
2 i/p OR, 1x	No Impact
Latch	No Impact
D Flipflop	No Impact

Table.1 Area Impact

B. Power Impact

The leakage power impact for paths using cells with 'l' Vs 'Delta l' is shown in the plot below(Fig.1) and the values in the table(Table.2)

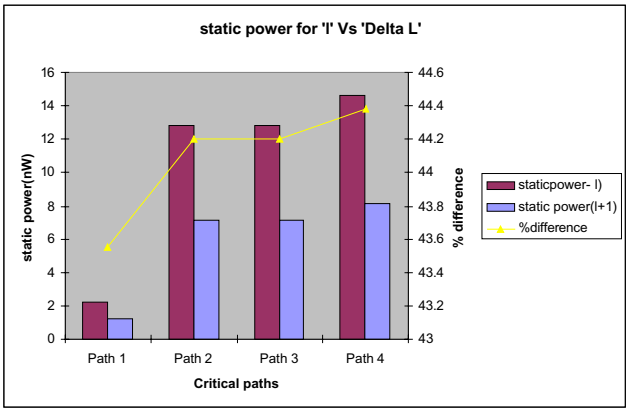

Fig.1 Static power comparison

	Staticpower (l)	static power(l+1)	%difference
Path 1	2.25	1.27	43.55556
Path 2	12.83	7.159	44.20109
Path 3	12.83	7.159	44.20109
Path 4	14.66	8.154	44.37926

Table.2 Static power comparison

There is a ~45% reduction in leakage power on an average by changing the channel length from l to l+1 grid. The paths we took has only combinational cells and the levels of logic varies from 4 to 10.

We measured the average dynamic power at the VDD node for the same paths. The average power has not significantly increased for channel lengths l+1. Refer to table(Table.3)

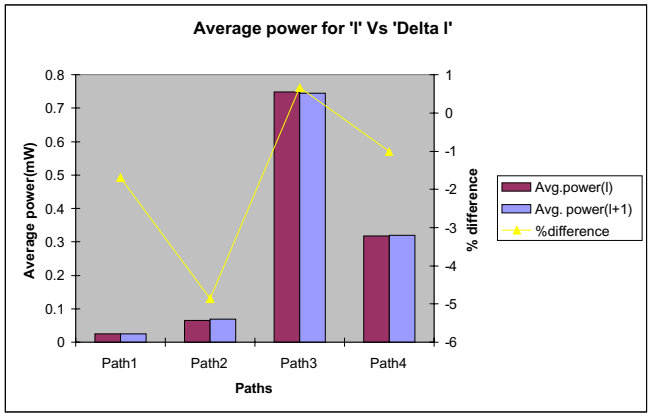

Fig.2 Average Dynamic Power comparison

	Avg. power(l)	Avg. power(l+1)	%difference
Path1	0.02458	0.024996	-1.69243
Path2	0.065187	0.068357	-4.86293
Path3	0.749375	0.744412	0.662285
Path4	0.316862	0.320073	-1.01337

Table.3 Average dynamic power comparison for *l* and *l+1*

The average power for delta L paths are at the most 5% greater than the minimum L paths(Refer Fig.2)

C. Performance Impact

Similarly there is a small increase in delay for delta L paths as expected.

The theoretical relationship between performance and channel length can be explained by the equation (3)

$$tphl = C/(\mu_n C_{ox}.\ W/L) * (VDD/(VDD-Vt)$$

$$\ldots\ldots\ldots\ldots(3)$$

From the plot(Fig.3) , it can be seen that the performance degradation is not more than 12%. In absolute values, the difference in delay is not more than 2ns for a path whose delay is 16ns(Table.4)

	Delay-(l)	Delay-(l+1)	%difference
Path1	2.7257	3.00403	-10.2113
Path2	1.02375	1.16348	-13.6488
Path3	16.932	18.1385	-7.12556
Path4	4.9546	5.39752	-8.93957

Table.4 Performance comparison for *l Vs l+1*

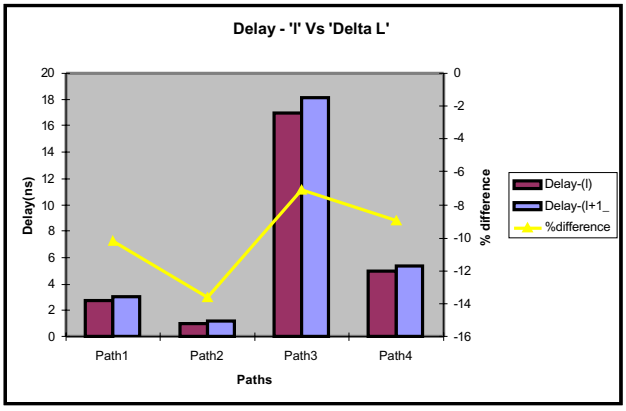

Fig.3 Performance comparison

If we look at the trends for delay, static and average power across different channel lengths(Fig.4) varying

from l to l+2 *min grid*, it is clear that the amount of leakage power reduction we get is huge and degradation in terms of average power and delay is not large enough to offset the reduction in leakage we get.

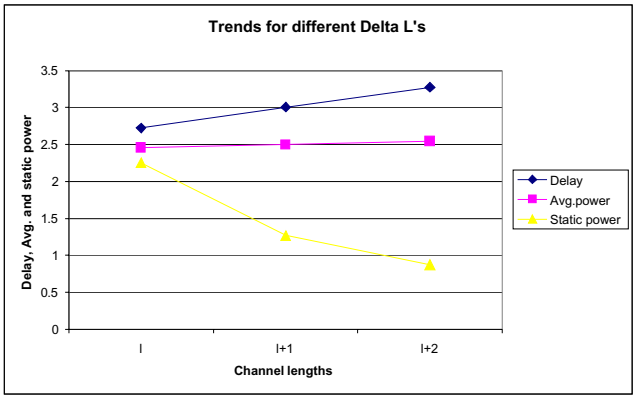

Fig.4 Delay, Static and dynamic power comparison for *l, l+1* and *l+2*

From the plot(Fig.4) it is apparent that this approach is a good strategy to follow for mobile applications.

IV. CONCLUSION

In summary if the channel length is increased by a min grid, the leakage power is reduced by 50%, with an area increase of ~1.5% in the chip level and a performance degradation of not more than 12%.

The degradation in delay and dynamic power is not significant and hence can be absorbed in the library for getting the leakage reduction desired.

A design which demands high density, good performance and very low leakage power can be obtained by mixing the two libraries – a library with minimum 'l' and library with 'delta l' to get the advantages of both the libraries. Also mixing these two libraries do not need any enhancements in the flow neither does it need any fabrication process changes and hence this is the most cost effective way to get the best of both libraries.

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