PREDICTMOS MOSFET Model and its Application to Submicron CMOS Inverter Delay Analysis

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Abstract

Predictive delay analysis is presented for a representative CMOS inverter with submicron device size using PREDICTMOS MOSFET model. As against SPICE, which adopts a time consuming numerical approach and relies more on empirical fitting of parameters for short channel devices, the predictive MOSFET model used is relatively simple and can be related to process and layout data with potential of estimation of the performance of a scaled design. The submicron CMOS inverter delay estimation under various loading and operative conditions have been compared against two benchmarks (a) Computer aided simulation with SPICE level 3 and (b) The analytical results of the Alpha Power Law based model. It is concluded that the PREDICTMOS model is potentially promising as a predictive analytic tool for submicron level design with transparency of device or circuit physics and an acceptable level of accuracy.

1. Introduction:

As the minimum feature size continues to decrease and the device count increases, it is increasingly realized by VLSI designers that simulators such as SPICE which are developed around numerical techniques are too slow for large scale designs. The problem gets further aggravated as the device model parameters for MOS transistors get more and more complex and empirical.

Though the CMOS gate / inverter transient characteristics, which are of primary interest to the VLSI designers, have been known through the analytical approach from the very early stage [1], the results are based on the early understanding of the device model. The lack of an accurate and manageable physical models for short channel devices and the domination of simulation based design methodology have resulted in the loss of physical insight into the dynamics of the CMOS switch based subcircuits and systems.

The basic difficulty of analytic handling of the CMOS devices with small geometry features has been the choice of an acceptable physical model. Shoji [2] was perhaps the first to address the design issues of primitive short channel CMOS cells analytically. The present day scaling of the MOS device at the submicron level, however, demands much higher degree of authenticity of modeling than that used by Shoji. Alpha (α or n) power law by Sakurai and Newton introduced an empirical approach to account for velocity saturation characteristics of scaled MOSTs of submicron feature size [3]. Though in the last few years alpha power model has been used with some degree of success in the analytical characterization of short channel submicron CMOS inverters and circuits with varying degrees of complexity and operating conditions such as step and ramp response with capacitive load neglecting PMOS current contribution [4], ramp response with gate – drain coupling capacitance [5], transient response including PMOS load current [6] switching delay with RC [7], and CRC interconnect [8] model, series connected gates [9], generalised delay estimation [10] etc, the approach survives with the limitation of being totally empirical denying the possibility of exploring the potential of scaled design. Further, the alpha power model does not meet the demanding requirement of analog design. There has been some effort to find a correspondence between

the alpha power model parameters and physical / technological entities of the device but it is at best an afterthought and does not have a natural physical basis.[11]

Briefly, there is a strong case for exploring a compact physical model which should be as cute and simple as the original quadratic model of MOS transistors, even in the presence of short channel effects such as velocity saturation, gate voltage dependent mobility degradation, channel length modulation, drain induced barrier lowering, etc. which characterize modern submicron and deep submicron devices so that an analytical design approach of basic analog and digital cells can be adopted keeping intact the transparency of the intrinsic device and circuit physics. Apart from the benefits of scalability such a model would be useful for developing physically meaningful delay and timing simulators with submicron devices.

The present work reports some initial exploratory results related to delay studies of short channel CMOS inverters with submicron feature size using a physics based predictive compact model – PREDICTMOS[15].The investigation demonstrates that the model could provide an analytical base for large signal analysis of digital design with a strong link to process and layout parameters, keeping intact the physical insight during circuit simulation. The results indicate an acceptable level of accuracy over a wide range of loading and tranisent conditions.

The scope of the present work is confined to the demonstration of the predictive potential of PREDICTMOS model in digital design through a few representative delay studies of primitive CMOS cells with typical interconnect and loading conditions. The analysis presented is without considering the role of PMOS load current and gate - drain coupling. It may however be mentioned that the above simplifications do not reflect a limitation of the PREDICTMOS analytical capability and have been adopted solely for a simplified presentation of the results.

The results with the PREDICTMOS model have been compared with two benchmarks selected: Alpha Power law analytical approach and the SPICE 3 circuit simulations.

Section 2 presents the essential features of PREDICTMOS and Alpha Power models. Section 3 gives the outline of the formulation for the delay analysis with final expressions of delay parameters. Section 4 gives the graphs and tables demonstrating the capability of PREDICTMOS based analysis. Section 5 summarizes the conclusion of the study.

2. MOSFET Model:

2.1 The PREDICTMOS Model :[15]

The current – voltage equation of small geometry CMOS transistor in PRDEICTMOS is given by the following relationship taking into account the velocity saturation, variation of the depletion channel width along the channel, channel length modulation , gate voltage dependent surface mobility, etc.:

$I_d=0$ for $V_{gs}<V_T$

$$Id_{lin}=\left[\frac{\mu_s WCox}{L+\frac{\mu_s}{\upsilon_s}V_{ds}}\right]\left[\left(V_{gs}-V_T-\frac{\alpha_i}{2}V_{ds}\right)V_{ds}\right] \quad \text{for } V_{ds}<V_{dsat} \qquad (1)$$

$$Id_{sat}=\left[\frac{\mu_s WCox}{L+\frac{\mu_s}{\upsilon_s}V_{ds}}\right]\left[\left(V_{gs}-V_T-\frac{\alpha_i}{2}V_{dsat}\right)V_{dsat}+\left(V_{gs}-V_T-\alpha_i V_{dsat}\right)\left(V_{ds}-V_{dsat}\right)\right]$$

$$\text{for } V_{ds}>=V_{dsat} \qquad (2)$$

$$V_{dsat}=\left[\left(\frac{V_{ge}+LE_p}{\frac{E_p}{E_c}-1}\right)\right]\left[\sqrt{\frac{1+2V_{ge}LE_p\left(\frac{E_p}{E_c}-1\right)}{\left(V_{ge}+LE_p\right)^2}}-1\right] \qquad (2a)$$

$$\alpha_i=1+\frac{0.5k_{eff}}{\sqrt{\phi_i+V_{sb}}}\left[1-\frac{1}{a_1+a_2\left(\phi_i+V_{sb}\right)}\right] \qquad (2b)$$

$$\mu_s=\frac{\mu_o}{1+\theta\left(V_{gs}-V_T\right)+2k_{eff}\theta\sqrt{\phi_i+V_{sb}}} \qquad (2c)$$

where $a_1=1.744$ and $a_2=0.8364$. for short channel devices, Equations (2a), (2b) and (2c) get into the PREDICTMOS model expression due to the considerations of the (a) velocity saturation effect due to the high electric field along the channel, (b) the bulk charge variation along the channel, and (c) gate voltage dependent mobility degradation. Cox is gate oxide capacitance per unit area, μ_s is the surface mobility, ν_s is the saturation velocity of the carrier mobility , W is the effective channel width, L is the effective channel length, V_{ge} is the effective gate voltage, V_{ds} is applied voltage between the drain and source and V_{gs} is the applied voltage between the gate and the source, k_{eff} is the effective substrate factor, E_c is the critical electric field, E_p is the geometry independent electric field at the saturation point, φ_i is the surface potential for the onset of strong inversion, V_{dsat} is the

drain saturation voltage, Id_{sat} and Id_{lin} are the currents in the saturation and linear regions respectively and V_{sb} is the applied bias between the source and the bulk.

2.2 Alpha Power Model:

As the results of PREDICTMOS have been compared with those obtained from the use of the alpha power law model. The Alpha Power law model is also mentioned for the sake of completeness and ready comparison. The I-V relationship is empirically assumed as [4]:

$$Id=0 , \quad V_{gs} < V_T \qquad (3)$$

$$Id=K_1(V_{gs}-V_T)^{\alpha/2}V_{ds}, \quad V_{ds} < V_{dsat} \qquad (4)$$

$$Id=K_s(V_{gs}-V_T)^{\alpha} , \quad V_{ds} > =V_{dsat} \qquad (5)$$

where α is the velocity saturation index and K_1 and K_s are technology parameters. It is to be noted that α is dependent on the degree of velocity saturation to be derived empirically and the conductance parameters K_1 and K_s are technology and device size dependent. They have however no direct physical basis.

PREDICTMOS uses the conventional approach of calculating the inversion charge in the region where the gradual channel approximation (GCA) is valid. In the high field region where the GCA fails and the gate progressively loses control over the channel a box approximation is assumed for the channel charge. .The continuity of charge between the GCA and non-GCA region preserved at the boundary. The current is computed by standard drift current formulation. As can be seen from the equation (2) the approach does not require the calculation of the modulation of electric channel length ΔL but elegantly accounts for the finite conductance of the device output through the drop of excess voltage ($V_{ds} - V_{dsat}$) on the high field region. The gate voltage dependence on mobility, geometry and bias dependence of the threshold voltage V_T can be easily incorporated. All the parameters involved are physical and scalability potential is built-in.

Alpha Power model on the other hand requires an empirical fitting of parameters such as α, K_1 and K_s to match the device characteristics. In short, where the Alpha Power lays emphasis on "fitting" with an analytically amenable simple form of the characterizing equation, the PREDICTMOS model is concerned with "predictability" without compromising on the parameters related to short channel MOS physics and the simplicity of the form.

3. Propagation Delay with Ramp Input Waveform:

3.1 Delay Estimation with Capacitive Load:

For transient analysis of the CMOS inverter as shown in the Fig. 1, we have considered the case of a ramp input which is a realistic description of the driving signal. For fast input ramps the effect of the PMOS on the delay can be neglected. This approximation is considered valid if the input slope exceeds one third the output slope, which normally happens in VLSI circuits, [4]. We shall make use of standard expression for the delay given by :

$$T_d = t_{0.5} - \frac{T}{2} \qquad (6)$$

where T_d is the propagation delay, $t_{0.5}$ is the time at which the output voltage drops to $V_{dd}/2$ and T is the input rise time as depicted in Fig. 2.

The transeint behavior of the circuit in Figure 1 is obtained using the following differential equation:

$$\frac{dV_{out}}{dt} = \frac{-I_{ds}}{C_L} \qquad (7)$$

where I_{ds} is the drain to source current and depending on the state of operation of the transistor, Id_{lin} or Id_{sat} may be obtained from equation (1) and equation (2) respectively.Equation (7) is not solvable with the form of equations that describe the current and therefore some of the expressions have to be recast in an appropriate form to make the equation (7) amenable to analytical solution. We only outline below the steps involved as the details are outside the scope of the present paper.

PREDICTMOS Delay :The calculation of the propagation delay involves the following steps :

- Step 1: Linearization of the function V_{dsat} which has nonlinear dependence on ($V_{gs} - V_T$).
- Step 2: Estimation of V_{out1} which is the value of output voltage when the input voltage reaches $V_{dd.}$
- Step 3: Calculation of $t_{do,}$ the time for which the NMOST is in saturation after the input has reached V_{dd} as shown in Fig. 2.
- Step 4: The calculation of $t_{1,}$ the time for which the NMOST operates in the linear region.
- Step 5: The limits of integration are between V_{out1} and $0.5V_{dd.}$

With the implementation of the above steps and some straightforward manipulation an analytical expression for the delay, as defined in equation (6), is obtained which is given below:

$$T_d = \frac{T}{2} + \left(\frac{C_L}{a}\right)\left[\left(\frac{V_{out1}}{g} + \frac{-b + gV_{out1} + gL\ln\left|f - gV_{out1} + g^2V_{out1}\right|}{g^2}\right)\right] - \left(\frac{C_L}{a}\right)\left[\left(\frac{\frac{V_{dd}}{2}}{g} + \frac{-b + gV_{dd} + gL\ln\left|f - gV_{dd} + g\frac{V_{dd}}{2}\right|}{g^2}\right)\right] \qquad (8)$$

where, a = μ_s W Cox ; f = (V_{gs}-V_T-α_i/2 V_{dsat}) V_{dsat} ; g = (V_{gs}-V_T -α_i/2 V_{dsat}) ; h = V_{dsat} ; i = α_i/2 ;
ν_t= V_T/ V_{DD} , and C_L is the capacitive load.
It may be noted that the terms involved in the prediction of delay are related to physically meaningful parameters of device, process and layout.
Alpha Power Delay : The expression for delay using the Alpha Power law is given by [4] :

$$T_d = \left(\frac{1}{2} - \frac{(1-\upsilon_t)}{(1+\alpha)}\right)T + \frac{C_L V_{dd}}{2I_{do}} \qquad (9)$$

where, I_{do} is the saturation current and the other symbols retain their meanings. It may be noted, that the expression for delay by Alpha Power model does not relate it with either the layout or process parameters. It may be further observed that both Alpha Power and PREDICTMOS based expressions for delay with capacitive load and ramp input maintain however, the same general form.

3.2 Delay Expression with RC Interconnect Load:

The delay expression for a CMOS inverter driving RC interconnect load using PREDICTMOS model is obtained by following the same steps as outlined above except that the limits of integration are between V_{out2} and (0.5 V_{dd}) which duly takes into account the shielding effect imposed by the interconnect resistance on the capacitive load to be seen by the inverter output [7]. Skipping the intermediate mathematical steps the final delay expression with PREDICTMOS model, is given by :

$$T_d = \frac{T}{2} + \left(\frac{C_L}{a}\right)\left[\left(\frac{V_{out1}}{g} + \frac{-fi + ghi + gL\ln\left|f - gh + gV_{out2}\right|}{g^2}\right)\right] - \left(\frac{C_L}{a}\right)\left[\left(\frac{\left(\frac{V_{dd}}{2}\right)}{g} + \frac{-fi + ghi + gL\ln\left|f - gh + g\left(\frac{V_{dd}}{2}\right)\right|}{g^2}\right)\right] \qquad (10)$$

where R is the interconnect resistance between CMOS output node and the output capacitive load C_L and V_{out2} is the value of the output voltage when the input voltage reaches V_{dd}. The delay expression of an inverter driving a RC interconnect load is given by equation (8) of [7].

4. **Discussion:**

4.1 Propagation Delay with Varying Capacitive Load and Rise Time:

The delay was obtained using the PREDICTMOS, Alpha Power law and SPICE 3 for comparison and the results are shown through graphs and tables. All the analysis and simulations are done for 0.6µ CMOS inverter with W=0.9µ, L=0.6µ and V_{dd}=5 volts. The figure 3 shows the change in propagation delay for varying capacitive loads. It is found that PREDICTMOS accuracy is superior to Alpha Power for low capacitive loads.
The table 1 shows the propagation delay for varying input rise times and a fixed capacitive load.

Table 1. Propagation Delay of a CMOS inverter Driving a Capacitive Load

T (nS)	C_L (f F)	T_d spice (nS)	T_d PREDICT MOS (nS)	T_d (Alpha Power) (nS)	Error PREDICT MOS (%)	Error (Alpha Power) (%)
0.1	150	0.43	0.39	0.39	9.3	9.3
0.25	150	0.44	0.42	0.4	4.5	9
0.5	150	0.48	0.46	0.41	4.1	14.5
0.75	150	0.51	0.49	0.43	3.9	15.6
1	150	0.55	0.51	0.44	7.2	20

It is observed that PREDICTMOS also leads to the conclusion that the propagation delay is less sensitive to input rise time compared to the capacitive load as given by SPICE and Alpha Power. An analysis of the results of Fig. 3 shows that PREDICTMOS model gives less error compared to the Alpha Power model on an average.

4.2 Propagation Delay with RC Interconnect:

Table 2 shows the propagation delay estimated by the PREDICTMOS model and Alpha Power model and their accuracy with respect to SPICE for a RC interconnect load for a few representative values of interconnect resistance for a fixed capacitive load.

Table 2. Propagation Delay of a 0.6µ CMOS Inverter Driving an R-C Interconnect

R Ω	T nS	C_L fF	SPICE T_d ns	PREDICTMOS T_d (ns)	Alpha Power T_d (ns)	Error PREDICT MOS (%)	Error (Alpha Power) (%)
100	0.5	150	0.47	0.45	0.4	4.2	14
500	0.5	150	0.41	0.41	0.34	0	17
1K	0.5	150	0.35	0.36	0.26	2.8	25

It is seen that PREDICTMOS gives accuracy in delay prediction much superior to that of Alpha Power for RC interconnect load, with Spice 3 as reference.

5. **Conclusions:**

- PREDICTMOS – a compact MOS model valid for submicron devices – has been used for characterizing the delay parameters of a CMOS inverter with submicron feature size providing physically meaningful analytical expressions
- Though relatively simple cases have been illustrated with PREDICTMOS for delay

modeling of the CMOS inverter neglecting the contribution form the PMOS load and gate – drain coupling, a more generalized analysis, can be also implemented with the model. It can be shown that with generalization of the analysis without the above approximations the PREDICTMOS results match even closer with SPICE.

- The sample results given show that the PREDICTMOS model gives comparable accuracy relative to the Alpha Power model and has been found to require significantly less computational time compared to SPICE in circuit simulation.
- PREDICTMOS circuit modeling is scalable as the expressions involve parameters related to layout and process which is not possible with Alpha Power approach. PREDICTMOS uses significantly less number of model parameters than BSIM and provides acceptable accuracy for digital CMOS design. Though not a substitute for BSIM, the predictive feature and analytical capability of PREDICTMOS have their own merits, advantages and applications.
- PREDICTMOS, in principle, has all the features for accurate analog circuit analysis making it suitable for mixed signal ASIC design.
- Results of more generalized considerations and specific applications are quite promising and under consideration for journal publication.

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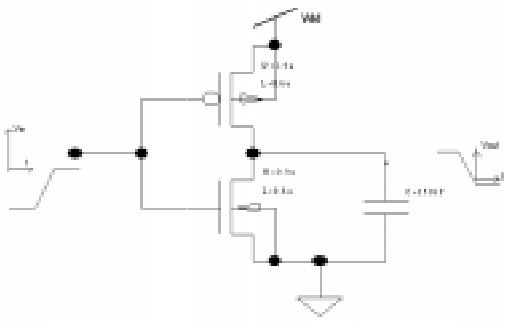

Figure 1. CMOS Inverter

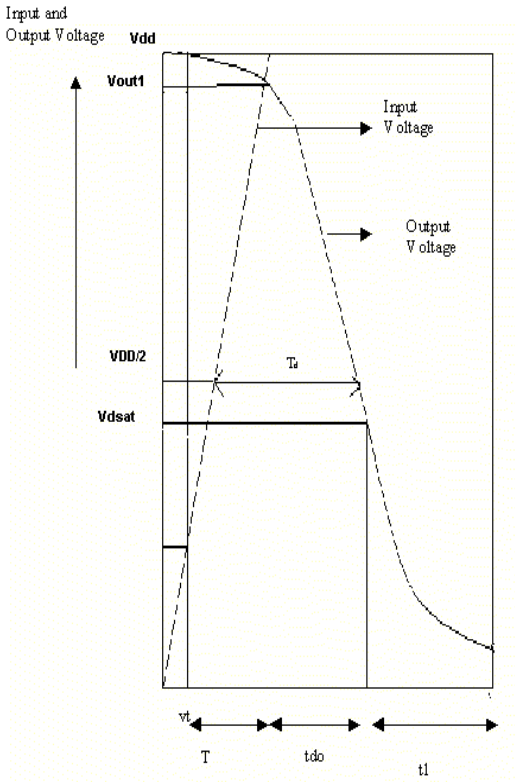

Figure 2. Inverter Operation Regions

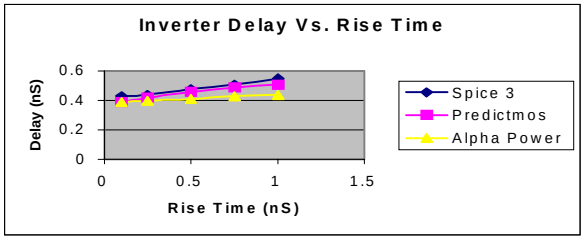

Figure 4. Inverter Delay Vs. Rise Time

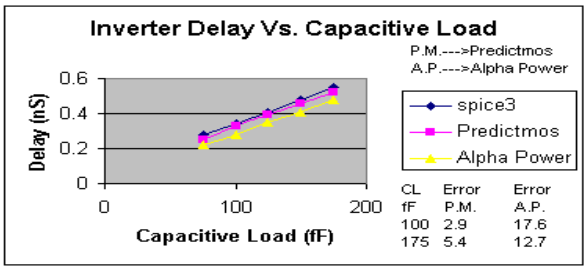

Figure 3. Inverter Delay Vs. Capacitive Load