Transistor Sizing for Reliable Domino Logic Design in Dual Threshold Voltage Technologies

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ABSTRACT

Dynamic logic is much susceptible to noise, specially in ultra deep submicron technology. The keeper transistor has to be carefully sized to maintain noise margin without much speed penalty. In this paper, we analyze the keeper transistor sizing with respect to the size of NMOS transistors in the evaluation tree. Based on the analytical results, we propose a keeper transistor sizing method. HSPICE simulation results show that the proposed keeper transistor sizing method can be broadly applied to all domino logic gates.

1. INTRODUCTION

Tight cycle time in giga-hertz range can not be met with static logic and thus designers use more dynamic logic [1, 8]. Unfortunately, dynamic logic is more susceptible to noise than static logic [5, 9]. Furthermore, in Ultra Deep SubMicron (UDSM) technology, the signal integrity is one of the most crucial circuit design issues [6]. For UDSM technology, the supply voltage has to be scaled down for reliability [3] and reduction of power consumption. Since lowering supply voltage causes performance degradation, it is desirable to scale down threshold voltage in proportion. V_t scaling increases subthreshold current (I_{sub}) exponentially, which makes dynamic circuit design much more difficult.

Recently, applying dual V_t to domino logic has been discussed. [9] recommends not to use low V_t in domino logic due to noise sensitivity. To reduce leakage currents in standby mode, Kao in [4] proposes to make all domino logic gates evaluated in standby mode. But noise immunity is not addressed in [4]. In dual V_t domino logic design techniques, the noise immunity has become one of the most important design issues due to significant crosstalk of UDSM technology and significant I_{sub} of low V_t transistor.

Several domino logic sizing algorithms have been proposed. [2] mainly focuses on timing constraint and does not pay attention to noise due to I_{sub}. Although [10] uses noise margin constraints with lower and upper bounds, it does not present any method how to find lower and upper bounds.

Domino logic can not recover after dynamic node loses its data due to noise. Thus, noise immunity must be considered while designing domino logic. The noise immunity of domino logic can be maintained by proper keeper transistor sizing. In this work, an analytical model for keeper sizing of domino logic gate is introduced. Based on the model, we propose a keeper sizing method.

2. NOISE SUSCEPTIBILITY OF DOMINO LOGIC

2.1 Noise Sources of Domino Logic

The dynamic node of domino logic should be held by a small keeper transistor during the evaluation phase. And the operation of domino logic is synchronized with clock, which can inject the noise to power supply. Furthermore, a domino logic gate, especially wide OR logic gate, has a very low trip point. Therefore, domino logic is intrinsically susceptible to noise.

In addition to the inherent noise sensitivity, UDSM technology and low V_t make it even worse. In UDSM technology, the crosstalk between two signal wires gets worse because the interconnection layers are packed closer together. Furthermore, V_t scaling increases I_{sub} exponentially. As a result, significant amount of I_{sub} of low V_t transistor acts a major noise source combined with increased crosstalk in UDSM technology. Thus, noise immunity must be taken into account when applying dual V_t to domino logic.

We adopt the following static noise constraint introduced in [9], which is widely used in industry. Base on the noise constraint, the keeper transistor will be sized to hold a dynamic node against noise during evaluation phase.

< Noise Constraint >

For a complex domino logic, we define a noise constraint as follows. V_{DD} is applied to the inputs of all the NMOS transistors in the evaluation tree except for topmost NMOS

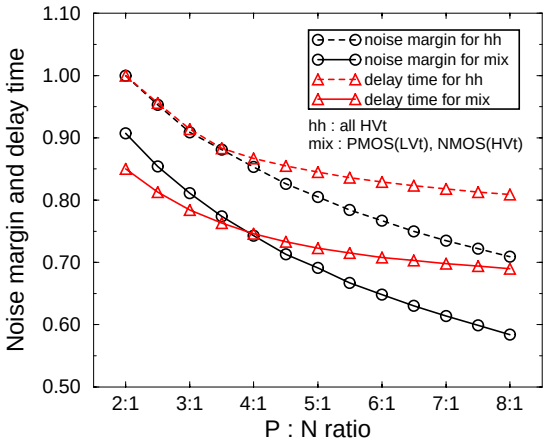

Figure 1: Noise margin and delay time of output inverter

transistors connected to the dynamic node. The input voltage of topmost NMOS transistors is $0.2 * V_{DD}$. The domino logic will be considered error free if the voltage of inverter output is less than $0.1 * V_{DD}$.

2.2 Keeper Transistor Sizing

Some tradeoff should be made between evaluation time and noise margin. Noise margin and delay time of the output inverter are shown in Figure 1. The symbol *hh* denotes inverter which has high V_t NMOS and PMOS transistors and *mix* denotes inverter which has high V_t NMOS and low V_t PMOS transistor. Noise margin and delay time are normalized by those of *hh* when P:N ratio is 2:1. Noise margin of output inverter is defined as follows.

$$NM_{H\ output\ inverter} = V_{DD} - V_{IH10\%} \quad (1)$$

where $NM_{H\ output\ inverter}$ is high noise margin of output inverter, V_{DD} is power supply voltage, and $V_{IH10\%}$ is input voltage of output inverter which corresponds to output voltage $0.1 * V_{DD}$.

As shown in Figure 1, the delay time of output inverter gets smaller but the noise margin of output inverter gets worse when output inverter is highly skewed (high P:N ratio) or low V_t is applied to the PMOS transistor of the output inverter.

We can also replace high V_t NMOS transistors in the evaluation tree with low V_t NMOS transistors to improve the performance. However, with low V_t, significant subthreshold leakage currents make the dynamic node unreliable, thus lowering noise immunity of domino logic. Unless we resize the keeper transistor appropriately, the domino logic may fail due to reduced noise margin. As the keeper size increases, the contention between the keeper and the NMOS transistors in the evaluation tree increases. The increased contention leads to more switching power consumption and may lead to more delay time.

In summary, noise margin depends on the P:N ratio of the output inverter and threshold voltage assignments. The keeper transistor has to be properly sized to maintain noise immunity while minimizing delay and power.

3. KEEPER TRANSISTOR SIZING ANALYSIS

3.1 Drain Current in Linear and Subthreshold Regions

Equations (2) and (3) describe the drain current (I_{DS}) in linear and subthreshold regions. BSIM2 MOS transistor model [7] is used for the subthreshold region.

1. *Linear Region* $[V_{GS} > V_t \ and \ 0 < V_{DS} < V_{DSAT}]$

$$I_{DS} = \mu_0 C_{ox} \left(\frac{W}{L}\right) [(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2] \quad (2)$$

2. *Subthreshold Region* $[0 < V_{GS} < V_t]$

$$I_{DS} = \mu_0 C_{ox} \left(\frac{W}{L}\right) A e^{q/n'KT(V_{GS}-V_t)} \cdot [1 - e^{-V_{DS}(q/KT)}] \quad (3)$$

where W and L are effective channel width and length, respectively. $A = (\frac{KT}{q})^2 e^{1.8}$. $V_{DSAT} = V_{GS} - V_t$ and $V_t = V_{T_0} + \gamma' V_S - \eta V_{DS}$. μ_0 is the zero bias mobility. C_{ox} is the gate oxide capacitance per unit area. n' is the subthreshold swing coefficient of the transistor. V_{T_0} is the zero bias threshold voltage. The body effect for small values of V_S is nearly linear. It is represented by the term $\gamma' V_S$, where γ' is the linearized body effect coefficient. η is the drain induced barrier lowering coefficient.

3.2 Domino Inverter Gate

Figure 2 shows domino inverter gate and node voltages to meet the noise constraint as mentioned in section 2.1.

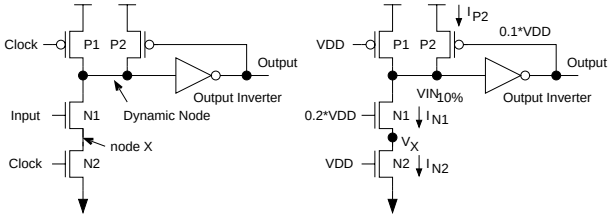

Figure 2: Domino inverter and node voltages to meet the noise constraint

Our concern is the noises injected into domino logic during evaluation mode. Therefore, clock is connected to V_{DD} and $0.2 * V_{DD}$ is applied to the input of domino logic as a noise. We set the dynamic node $V_{IN10\%}$ since the minimum allowable voltage of dynamic node is $V_{IN10\%}$ to meet the noise constraint where $V_{IN10\%}$ corresponds to the inverter output of $0.1 * V_{DD}$. $V_{IN10\%}$ depends on the P:N ratio and the threshold voltage of the output inverter. Transistor N1 is in subthreshold region because V_{GS} of N1 is less than V_t, while transistors N2 and P2 are in linear region because the absolute values of V_{DSAT} of N2 and P2 are greater than V_{DS}. In this analysis, the subthreshold current of transistor P1 and the gate leakage currents are ignored because they are far

smaller than the currents through N1, N2 and P2. Therefore, based on Equations (2) and (3), I_{N1} and I_{N2} through N1 and N2 are described by

$$I_{N1} = \mu_0 C_{ox}\left(\frac{W_{N1}}{L_{N1}}\right) A e^{q/n' KT(0.2*V_{DD}-V_X-V_{tN1})} \cdot\left[1-e^{-(V_{IN10\%}-V_X)(q/KT)}\right] \quad (4)$$

$$I_{N2} = \mu_0 C_{ox}\left(\frac{W_{N2}}{L_{N2}}\right)\left[(V_{DD}-V_{tN2})V_X - \frac{1}{2}V_X^2\right] \quad (5)$$

where $V_{tN1} = V_{Tn_0} - \eta V_{IN10\%} + (\gamma' + \eta)V_X$, $V_{tN1} = V_{Tn_0} - \eta V_{IN10\%} + (\gamma' + \eta)V_X$, and V_X is the voltage of internal node X between N1 and N2 as shown in Figure 2.

Under this condition, V_x and q/KT is far less than $(V_{DD} - V_{tN2})$ and $(V_{IN10\%} - V_X)$, respectively. Therefore, Equations (4) and (5) can be simplified as

$$I_{N1} = \mu_0 C_{ox}\left(\frac{W_{N1}}{L_{N1}}\right) A e^{q/n' KT(0.2*V_{DD}-V_X-V_{tN1})} \quad (6)$$

$$I_{N2} = \mu_0 C_{ox}\left(\frac{W_{N2}}{L_{N2}}\right)(V_{DD}-V_{tN2})V_X \quad (7)$$

where $V_{tN1} = V_{Tn_0} - \eta V_{IN10\%}$ and $V_{tN2} = V_{Tn_0} - \eta V_X$.

Because $I_{N1} = I_{N2}$, with $L_{N1} = L_{N2}$, Equations (6) and (7) lead

$$(V_{DD} - V_{tN2})V_X = \left(\frac{W_{N1}}{W_{N2}}\right) A e^{q/n' KT(0.2*V_{DD}-V_X-V_{tN1})} \quad (8)$$

$V_{IN10\%}$ is predetermined according to P:N ratio and V_t of the output inverter. The internal node voltage V_X is uniquely defined for a given (W_{N1}/W_{N2}). Therefore, I_{N1} and I_{N2} can be related to W_{N1} and W_{N2} as follows.

$$I_{N1} = f_1\{V_X(W_{N1}/W_{N2})\} \cdot W_{N1} \quad (9)$$

$$I_{N2} = f_2\{V_X(W_{N1}/W_{N2})\} \cdot W_{N2} \quad (10)$$

For a given value of (W_{N1}/W_{N2}), the only variable to set I_{N1} (or I_{N2}) is W_{N1} (or W_{N2}). In other words, with a fixed size ratio of NMOS transistors in the evaluation tree, the current through NMOS tree I_N is linearly proportional to W_{N1} or W_{N2}, i.e,

$$\textit{For a given } (W_{N1}/W_{N2}) \textit{ ratio}$$
$$I_N = \alpha_1 \cdot W_{N1} = \alpha_2 \cdot W_{N2} \quad (11)$$

where α_1 and α_2 are constants.

Now, let us consider the keeper transistor P2 in its linear region. According to Equation (2), the current I_{P2} is given by

$$I_{P2} = \mu_0 C_{ox}\left(\frac{W_{P2}}{L_{P2}}\right)[(0.1*V_{DD} - V_{DD} - V_{tP2}) \cdot (V_{IN10\%} - V_{DD}) - \frac{1}{2}(V_{IN10\%} - V_{DD})^2] \quad (12)$$

where $V_{tP2} = V_{Tp_0} + \eta V_{IN10\%}$.

Since all variables in Equation (12) are fixed except for W_{P2}, we have a simplified following expression.

$$I_{P2} = \beta \cdot W_{P2} \quad (13)$$

where β is a constant.

Because $I_N = I_{P2}$, we can conclude from Equations (11) and (13) that

$$\textit{For a given } (W_{N1}/W_{N2}) \textit{ ratio}$$
$$\left(\frac{W_{P2}}{W_{N1}}\right) = \frac{\alpha_2}{\beta} \cdot \left(\frac{W_{N2}}{W_{N1}}\right) = C \ (\textit{constant}) \quad (14)$$

The size ratio for evaluation NMOS transistors determines an optimal (W_{P2}°/W_{N1}) ratio, where W_{P2}° is optimal keeper transistor size. If the keeper transistor size is greater than W_{P2}°, then it results in unnecessary data contention between PMOS keeper transistor and NMOS transistors in the evaluation tree. Thus, the performance is degraded and the power consumption is increased. If the keeper transistor size is less than W_{P2}°, then the domino circuit cannot meet the noise constraint. It results in functional failures.

The value of V_X varies with the (W_{N1}/W_{N2}) ratio, so do the values of α_1 and α_2. Therefore, we can not expect the effect of (W_{N1}/W_{N2}) ratio change from Equation (14). Next, we evaluate the effect of (W_{N1}/W_{N2}) ratio.

Let $(W'_{N1}/W'_{N2})/(W_{N1}/W_{N2}) = K$ and $K > 1$. From Equation (8), the following equation is obtained.

$$\left(\frac{V_X}{V'_X}\right) = \left(\frac{V_{Tn_0} - nV'_X}{V_{Tn_0} - nV_X}\right)\frac{1}{K} e^{q/n' KT(1+\gamma'+\eta)(V'_X - V_X)} \quad (15)$$

where V_X and V'_X are the voltage of node X corresponding to (W_{N1}/W_{N2}) and (W'_{N1}/W'_{N2}), respectively.

We can observe from Equation (15) the following inequality for all values of γ' and η.

$$V'_X < KV_X \quad (16)$$

From (7), (13) and $I_{N2} = I_{P2}$

$$I_{N2} = \alpha_3 \cdot W_{N2} \cdot V_X, \quad I'_{N2} = \alpha_3 \cdot W'_{N2} \cdot V'_X$$
$$I_{P2} = \beta \cdot W_{P2}, \quad I'_{P2} = \beta \cdot W'_{P2}$$
$$W_{P2} = \left(\frac{\alpha_3}{\beta}\right) W_{N2} V_X, \quad W'_{P2} = \left(\frac{\alpha_3}{\beta}\right) W'_{N2} V'_X \quad (17)$$

where, α_3 and β are constants.

By combining (16) and (17),

$$W'_{P2} = \left(\frac{\alpha_3}{\beta}\right) W'_{N2} V'_X < \left(\frac{\alpha_3}{\beta}\right) W'_{N2} K V_X < K W'_{N2}\left(\frac{W_{P2}}{W_{N2}}\right) \quad (18)$$

By inserting $K = (W_{N1}^{'}/W_{N2}^{'})/(W_{N1}/W_{N2})$ into (18),

$$\left(\frac{W_{P2}^{'}}{W_{N1}^{'}}\right) < \left(\frac{W_{P2}}{W_{N1}}\right) \quad for \quad \left(\frac{W_{N1}^{'}}{W_{N2}^{'}}\right) > \left(\frac{W_{N1}}{W_{N2}}\right) \qquad (19)$$

We can see the (W_{P2}/W_{N1}) ratio decreases as (W_{N1}/W_{N2}) ratio increases.

3.3 Complex Logic Gate

Figure 3 shows k-input OR gate and k-input AND gate. To simplify the analysis, we assume a uniform (W/L) ratio for all NMOS transistors in the evaluation tree. However, our analysis can be readily extended to arbitrary (W/L) ratios. For k-input OR gate as shown in Figure 3(a), all

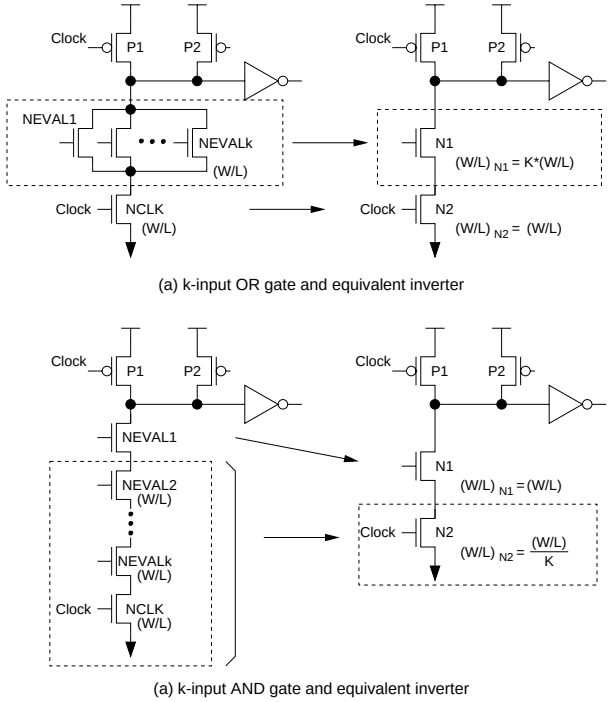

Figure 3: K-input OR and k-input AND gate and equivalent circuit

the evaluation NMOS transistors ($\text{NEVAL}_1, \cdots, \text{NEVAL}_k$) are in subthreshold region and have the same V_{GS}, V_{DS} and V_t. Thus, the (W/L) ratio of an equivalent transistor N1 for the evaluation NMOS transistors and the (W/L) ratio of the equivalent transistor N2 are

$$\left(\frac{W}{L}\right)_{N1} = \sum_{i=1}^{k}\left(\frac{W}{L}\right)_{NEVAL_i} = k\left(\frac{W}{L}\right) \qquad (20)$$

$$\left(\frac{W}{L}\right)_{N2} = \left(\frac{W}{L}\right)_{NCLK} = \left(\frac{W}{L}\right) \qquad (21)$$

For k-input AND gate, we assume that NCLK, NEVAL_2 through NEVAL_k in the linear region have the same threshold voltages. And the values of $\frac{1}{2}V_{DS}^2$ in Equation (2) for those transistors are negligible. Then the (W/L) ratio of the equivalent transistor N2 for NCLK, NEVAL_2 through NEVAL_k, and the (W/L) ratio of the equivalent transistor N1 are given by

$$\left(\frac{W}{L}\right)_{N1} = \left(\frac{W}{L}\right)_{NEVAL_1} = \left(\frac{W}{L}\right) \qquad (22)$$

$$\left(\frac{W}{L}\right)_{N2} = \left[\sum_{i=2}^{k}\left(\frac{L}{W}\right)_{NEVAL_i} + \left(\frac{L}{W}\right)_{NCLK}\right]^{-1} = \frac{1}{k}\cdot\left(\frac{W}{L}\right) \qquad (23)$$

Now, we know the (W_{N1}/W_{N2}) ratios of the equivalent transistors N1 and N2 for k-input OR and k-input AND gates. And (W_{P2}/W_{N1}) ratio is determined for a given (W_{N1}/W_{N2}) ratio. Therefore, we can find the (W_{P2}/W_{N1}) ratio from pre-simulated value.

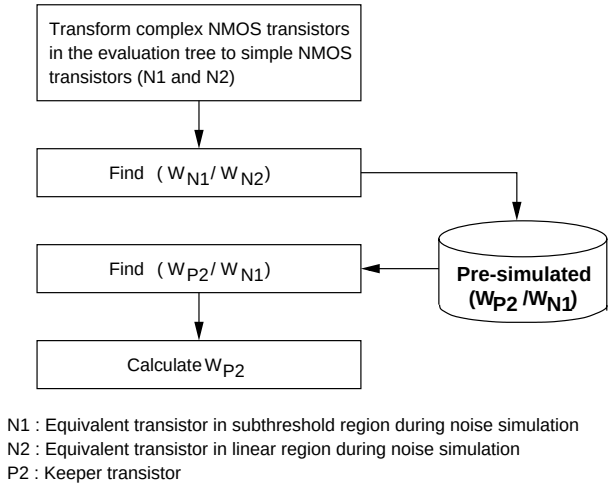

Figure 4: Keeper sizing flow

Figure 4 shows the generic flow of keeper sizing. First, complex NMOS transistors in the evaluation tree are transformed to equivalent NMOS transistors, namely N1 and N2 transistors. N1 transistor is the equivalent transistor which corresponds to the transistors in subthreshold region. N2 transistor is the equivalent transistor which corresponds to the transistors in linear region. Then, the (W_{N1}/W_{N2}) ratio is computed from equivalent NMOS transistors ($N1$ and $N2$). Next, (W_{P2}/W_{N1}) ratio can be determined by pre-simulated (W_{P2}/W_{N1}) ratio based on the value of (W_{N1}/W_{N2}). From Equation (14), (W_{P2}/W_{N1}) remains constant as long as (W_{N1}/W_{N2}) fixed. Therefore it is unnecessary to simulate all the design corners corresponding to feasible ranges of W_{N1} and W_{N2} to achieve an optimal keeper transistor size. In other words, the pre-simulated value of (W_{P2}/W_{N1}) ratio for a (W_{N1}/W_{N2}) ratio can be used to compute (W_{P2}/W_{N1}) ratio of all domino logics which have the same (W_{N1}/W_{N2}) ratio. Finally, the keeper size is obtained by computing $W_{P2} = W_{N1} \cdot (W_{P2}/W_{N1})$.

4. SIMULATION RESULTS

Table 1 shows the delay time and sub-threshold leakage current (I_{sub}) characteristics for low and high V_t transistors which were used in our work. The values of delay time and I_{sub} are normalized with respect to high V_t transistor.

Table 1: Performance and subthreshold leakage current of low and high threshold voltage transistors

Transistor Type	Delay Time	Sub-Threshold Leakage Current
High V_t	1.0	1.0
Low V_t	0.85	4.1

Table 2: Simulation cases

Type	evaluation NMOS	PMOS of Static CMOS gate
HH	High V_t	High V_t
LL	Low V_t	Low V_t

Table 2 shows two simulation cases according to V_t assignment. One is HH type domino logic which uses all high V_t transistors. The other one is LL type domino logic, where low V_t is applied to NMOS transistors in the evaluation tree and PMOS transistor of the output inverter.

Figure 5 and 6 show simulation results of keeper sizing for 15 domino inverters which have different W_{N1} and W_{N2} for HH type and LL type, respectively.

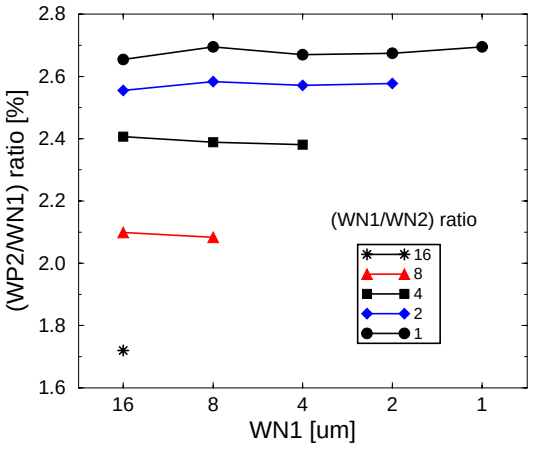

Figure 5: Simulation results of keeper sizing for 15 different domino inverters of HH type

W_{N1} varies from $1\mu m$ to $16\mu m$ and W_{N2} varies from $1\mu m$ to $16\mu m$ with $W_{N1} > W_{N2}$. If high V_t transistors are replaced by low V_t transistors to improve performance, the keeper transistor size (W_{P2}) has to be increased. Figure 5 and 6 indicate that for the same W_{N1}/W_{N2} ratio, the W_{P2}/W_{N1} ratio is almost constant within 5% tolerance irrespective of W_{N1} and W_{N2}, which supports Equation (14). Therefore, keeper transistor sizes of domino inverter gates, even for same W_{N1}, depend on the W_{N1}/W_{N2} ratio. As W_{N1}/W_{N2} ratio increases, W_{P2}/W_{N1} ratio decreases as expected from Equation (19).

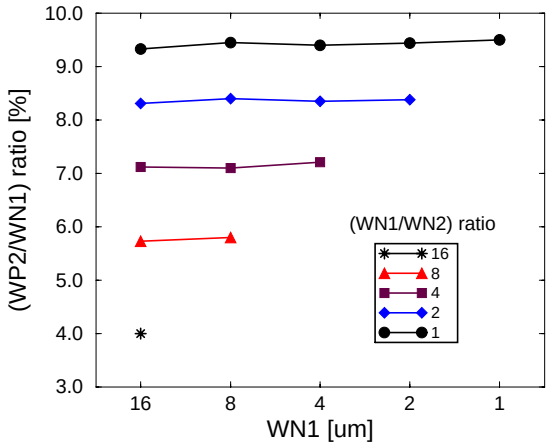

Figure 6: Simulation results of keeper sizing for 15 different domino inverters of LL type

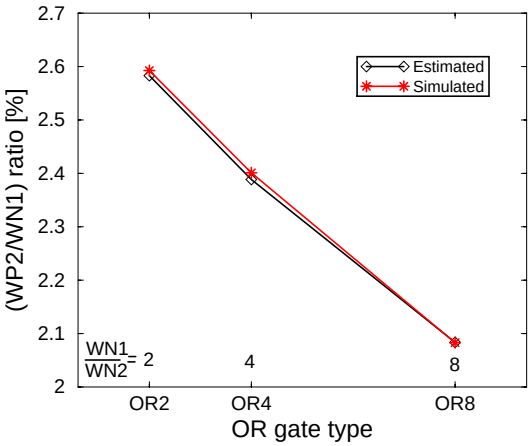

Figure 7: (W_{P2}/W_{N1}) ratio for 2,4 and 8-input OR gate

For instance, the W_{P2}/W_{N1} ratio of $W_{N1} = 8\mu m$ can be selected as the pre-simulated values. Figure 7 shows two sets of (W_{P2}/W_{N1}) ratios with respect to various OR gates. One set is for pre-simulated W_{P2}/W_{N1} ratios of $W_{N1} = 8\mu m$. Another set is obtained by HSPICE simulation for different OR gates of HH type. W_{NEVAL_i} and W_{NCLK} are $4\mu m$ for all OR gates. Figure 7 asserts that computation results based on our analytic model accurately comply with real simulation results.

Similarly, the computation results and simulation results on (W_{P2}/W_{N1}) ratios are compared for various AND gates as shown in Figure 8. W_{NEVAL_i} and W_{NCLK} are set to $6\mu m$, $9\mu m$ and $12\mu m$ for 2, 3 and 4-input AND gates, respectively.

Figure 9 shows an example of the complex domino logic gate. The equivalent W_{N1} is $21\mu m$ and W_{N2} is $20/3\mu m$. Therefore, (W_{N1}/W_{N2}) ratio is 3.15 for an equivalent con-

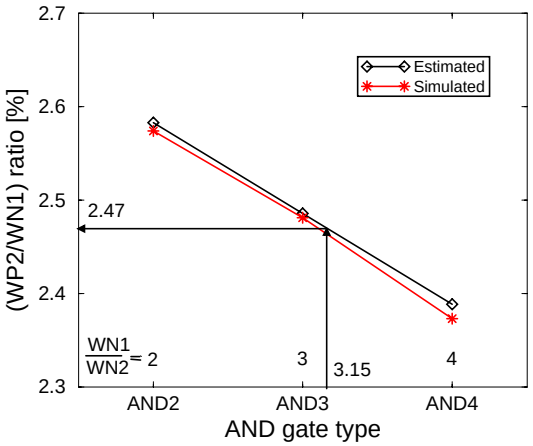

Figure 8: (W_{P2}/W_{N1}) ratio for 2,3 and 4-input AND gate

figuration. Simulated (W_{P2}/W_{N1}) ratio is 0.025. From pre-simulated value, (W_{P2}/W_{N1}) ratio is 0.0247 as shown in Figure 8, which matches into the simulated value well. Therefore, the estimated value from pre-simulated value can be used to determine the keeper size for any types of logic gates as expected in our analysis.

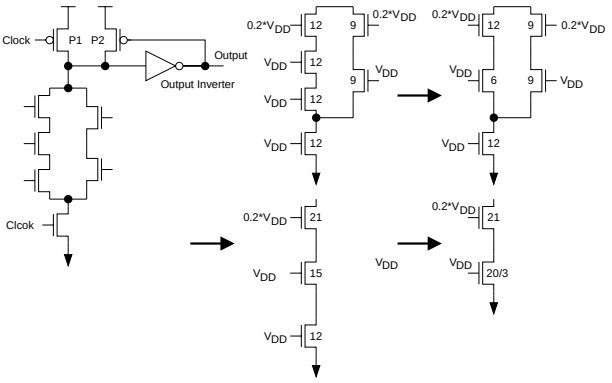

Figure 9: Complex gate and its equivalent gate

5. CONCLUSION

Domino logic has been prevalently used for high performance circuit design. However, domino logic becomes more sensitive to noise in UDSM and dual threshold voltage technology. The noise immunity of domino logic can be maintained by properly sizing the keeper transistor. When the threshold voltage is lowered to improve performance, we should reconsider the keeper transistor sizing. In this paper, we presented an analytical model for keeper transistor sizing to meet the noise constraint. Simulation results show that our analytical model can be applied effectively to domino inverter and complex logic gates.

6. ACKNOWLEDGMENTS

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