Design for Testability Strategies Using Full/Partial Scan Designs and Test Point Insertions to Reduce Test Application Times

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Abstract As an LSI is on the two-dimensional plane, the number of external pins of an LSI does not equally increase to the number of gates. Therefore, the number of flip-flops on a scan path is relatively increasing. As the results, the test application time becomes longer. In this paper, three new DFT strategies are proposed to reduce the test application time. Experimental results showed the DFT strategies reduced the test application times by 46 to 82% compared with a conventional full scan design method.

1. INTRODUCTION

According to the recent advance of semiconductor process technology, the circuit densities on LSI are growing and the automatic test design becomes more important. Because the automatic test pattern generation (ATPG) for a sequential circuit is difficult in general, a design for testability (DFT) must be applied to obtain high fault efficiency. The full scan design method [1,2] is one of popular DFT methods, so far. In the full scan design method, all flip-flops (FFs) are replaced with scan FFs. A scan FF is equivalent to a primary input and a primary output at the test mode. In the scan design method, ATPG can be performed for the portion of the circuit excluding the scan path, which is the kernel circuit. Since the kernel circuit of the full scan design LSI is a combinational one, a combinational ATPG algorithm can be applied to it and it can obtain high fault efficiency.

Test application time by the scan design method is the product of the test length of an automatic test equipment (ATE) of the formula (1) and the clock period of the ATE.

$$TL = (TP + 1) \times MSL + TP \quad \ldots(1)$$

In the formula(1), TL is test length of an ATE, TP is the number of test patterns of the kernel circuit and is called the ***ATPG patterns***, MSL is the maximum number of scan FFs on one scan paths and is called the ***maximum scan path length***.

As the increasing number of the external pins on LSI boundary is slower than the increase of the size of an LSI, the number of scan FFs on a scan path connected to the external pins increases relatively. Consequently, the full-scan-design test application time becomes longer. The formula (1) shows that the test length of a scan design method can be shortened by shortening the maximum scan path length and/or by reducing the number of ATPG patterns.

In this paper, three DFT strategies are proposed in order to reduce test application times as follows:

(1) DFT strategy1: applies the full scan design method with test point insertions to an LSI.
(2) DFT strategy2: applies the partial scan design method to an LSI.
(3) DFT strategy3: applies the partial scan design method with test point insertions to an LSI.

The next section explains the motivation of this research. In section 3, the three DFT strategies are proposed. The effectiveness of the strategies by applying them to practical LSIs are showed in section 4. The conclusion and our future works are described in section 5.

2. MOTIVATION

The road map of ITRS [3] predicts that the number of gates increases at a rate of about 40% per year, and the number of external pins increases at a rate of about 10% per year. Experimentally the number of FFs is proportional to the number of gates, and the number of scan paths is proportional to the number of external pins, i.e. the increase of the number of scan paths is slower than that of FFs. Thus, the maximum scan path length is lengthened.

On the other hand, the amount of increase of the number of ATPG patterns depends on the structure of a circuit when the number of gates increases. Fig.1 shows the relation between the numbers of gates in the IP (Intellectual Property) circuits including a decoder and the numbers of ATPG patterns of them. In Fig.1, #TP shows the numbers of ATPG patterns, #GATE shows the numbers of the gates, and #BIT shows the numbers of outputs of decoders in the IP circuits. #TP is increasing in proportion to increase of #GATE. If combinational circuits of a primary output are constituted using

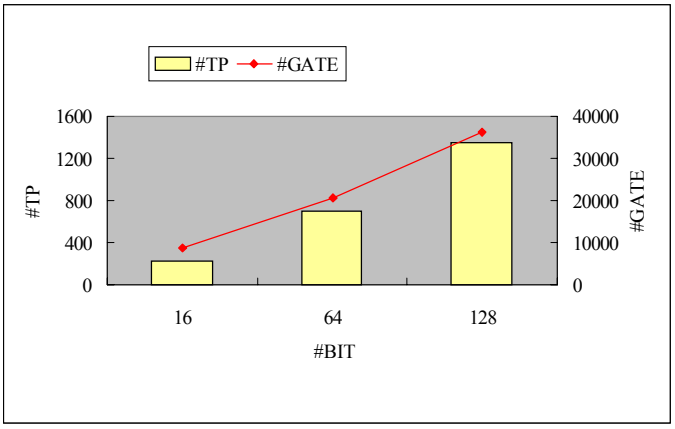

Fig.1 Relation between the number of ATPG patterns and the number of gates of IP circuits including a decoder

many primary inputs, the number of primary inputs where 0's and/or 1's are assigned to detect a certain fault at the primary output may increase. It is considered that the effect of the test pattern compaction [10,12,13] is generally low in this case. Since ALUs like multipliers do not consist of the combinational circuits of a primary output using many primary inputs, it is considered that the effect of test pattern compaction is generally high. On the other hand, since decoders consist of the combinational circuits of each primary output using all primary inputs, the effect of test pattern compaction is very low. The number of ATPG patterns will also increase by leaps and bounds for large-scale circuits where the effect of test pattern compaction is low.

3. DFT STRATEGIES FOR SHORTENING OF THE TEST LENGTH

3-1. Basic Concept of DFT Strategies

Let m be the number of blocks in a circuit, let B_i (i=1, 2, …, m) be a block, and let T_i be an ATPG patterns of B_i when it is considered that each input of B_i is a primary input and each output of B_i is a primary output. Here, an ***ideal LSI model*** is defined as an LSI which has the following features.

(Features 1) Each output of B_i is directly connected with each FF in B_i. (These FFs are called ***output FFs***.)

(Features 2) The number of fanouts of each output of B_i is one.

In this ideal LSI model, the expected values of T_i are observable at output FFs of B_i by replacing the output FFs of B_i with scan FFs and let OS_i be a set of scan FFs which observe the expected values of T_i. Moreover, T_i is controllable from output FFs of blocks whose outputs are connected with the inputs of B_i. Let CS_i be a set of scan FFs which control T_i. T_i may be also controllable from primary inputs. However, since the number of the primary inputs is a negligible amount in many cases, in this ideal LSI model, the primary inputs is not taken into account. In this ideal LSI model, because $CS_i \cap CS_j$ = empty ($i \neq j$, integer of $1 \leq i, j \leq m$) and $OS_i \cap OS_j$ = empty ($i \neq j$, integer of $1 \leq i, j \leq m$), each T_i can be simultaneously set to each element of CS_i. Thus, the number of ATPG patterns of an ideal LSI model is max(T_i). It is experimentally considered that the structures of practical LSIs is similar to that of an ideal LSI model. In this paper, it is assumed that the number of ATPG patterns of a practical LSI is nearly equal to the maximum number of ATPG patterns of blocks in the practical LSI (**Assumption 1**).

3-2. DFT Strategy 1

(1) The algorithm of DFT strategy 1

Fig. 2 illustrates the algorithm of DFT strategy 1 which uses the full scan design method with test point insertions. First, the number of ATPG patterns is calculated by applying the full scan design method to each block and by performing ATPG for each block (the 3rd line of Fig.2). The inputs and outputs of the blocks are considered as the primary inputs and outputs, respectively. Next, the block with the maximum number of ATPG patterns is selected as a target block (B_{tpi}) of test point insertions (the 4th line of Fig.2). The full scan design method is applied to B_{tpi} (the 7th line of Fig.2) and test points are inserted into B_{tpi} (the 10th line of Fig.2). The full scan design method is applied to other blocks (the 7th line of Fig.2). Since the maximum number of ATPG patterns of blocks is nearly equal to that of the LSI (**Assumption 1**), the reduction of the number of ATPG patterns of B_{tpi} reduces TL of the formula (1).

(2) The Basic Concept of Test Point Insertion

The test point insertion method to reduce the number of ATPG patterns is explained. Fig. 3 shows a target circuit of the test point insertions. ***C1*** through ***C10*** are combinational gates, and ***n1*** through ***n33*** are signal lines. ***n1*** through ***n4*** are primary inputs, and ***n31*** through ***n33*** are primary outputs. The ***fault detection probability*** and the ***value assignment probability*** are defined as cost functions to reduce the number of ATPG patterns. A target circuit of test point insertions is a combinational circuit.

(Definition 1 : *Fault Detection Probability*)

The ***fault detection probability PD (PO_i)*** at a primary output PO_i is defined as the rate of the number of signal lines which are reachable from a primary output PO_i to the total number of signal lines in a circuit, provided that when a signal line l which is reachable from PO_i is reachable to k primary outputs, signal line l is calculated with $1/k$.

```
1:  DFT Strategy 1 ( )
2:  {
3:      Calculate the full scan ATPG patterns for all blocks.
4:      Select the test point insertion block Btpi that has the maximum ATPG
          pattern.
5:      for (each block)
6:      {
7:          Apply full scan design method to Bi.
8:          if (Bi == Btpi)
9:          {
10:             Insert test points for Btpi.
11:         }
12:     }
13: }
```

Fig.2 Algorithm of DFT strategy 1

Example 1: Let us calculate the fault detection probability at ***n32***. The number of signal lines which are reachable to only the primary output ***n32*** is 3 (i.e. signal lines ***n27***, ***n29***, and ***n32***). The number of signal lines which are reachable to two primary outputs including ***n32*** is 9 (i.e. signal lines ***n6***, ***n10***, ***n12***, ***n14***, ***n17***, ***n18***, ***n19***, ***n25***, and ***n28***). The number of signal lines which are reachable to three primary outputs including ***n32*** is 6 (i.e. signal lines ***n1***, ***n2***, ***n4***, ***n11***, ***n15***, and ***n16***). Thus, ***PD(n32)*** is 28.79% from (3+9/2+6/3) / (33) .

(Definition 2 : *Value Assignment Probability*)

The ***value assignment probability PA(l)*** of a signal line ***l*** is defined as the probability that 0 or 1 is assigned to the signal line ***l*** at the time of ATPG to detect a fault. The value assignment probability ***PA(l)*** is calculated by summing up the fault detection probabilities of all the primary outputs which the signal line ***l*** is reachable to. When a fault is detected at a primary output PO_i, the value assignment probability is defined based on the concept that 0 and/or 1 may be assigned to all the signal lines that are reachable from PO_i if the worst comes to the worst.

Example 2: Let us calculate the value assignment probability of ***n25***. Since ***n25*** is reachable to the primary outputs ***n32*** and ***n33***, ***PA(n25)*** is 66.67% from ***PD(n32) + PD (n33)***.

On the other hand, test compaction technique [10,12,13] of ATPG pattern shows that compaction efficiency becomes high if an ATPG pattern includes many don't cares (*Xs*). If value assignment probabilities of primary inputs are low, the probability that the values of primary inputs are *Xs* becomes high, so that compaction efficiency may be high. The number of ATPG patterns can be reduced if compaction efficiency becomes high.

In this test point insertion method, test points are inserted into signal lines so that value assignment probabilities of primary inputs are made low. Let ***PI(l)*** be a set of primary inputs which are reachable from a signal line ***l***, let ***PO(l)*** be a set of primary outputs which a signal line ***l*** is reachable to, let lpo_i (i=1,2,…, ***m***) be each element of ***PO(l)***, and let ***m*** be the number of ***PO(l)***. The test point insertion into ***l*** may reduce the value assignment probabilities of the primary inputs which are $\bigcup_{i=1}^{m} PI(lpo_i)$. The concept of the test point insertion is that the value assignment probabilities of primary inputs as many as possible are reduced by the test point insertion. In this paper, test points are inserted into signal lines which are fan-out stems with high value assignment probabilities and whose level are multiples of n (n is a positive integer). Since we do not aim at the proposal of the refined test point insertion algorithm, in this paper, we will consider it in our future work. In Fig.3, ***l(PA (l))*** is denoted on a signal line ***l***. Each value assignment probability of the primary inputs of Fig.3 is as follows. ***PA(n1)*** =100%, ***PA(n2)*** =100%, ***PA(n3)*** =71.21%, and ***PA(n4)*** =100%. In this example, test points are inserted into signal lines which are fan-out stems (the value assignment probabilities are more than 60%) and whose level are multiples of n (n=3). Test points are inserted into ***n25*** and ***n28***. Each signal line where a test point is inserted can be considered as a primary input and a primary output, and the circuit that test points are inserted into ***n25*** and ***n28*** is shown in Fig.4. In Fig.4, ***n25*** is modified to the primary input ***n25pi*** and the primary output ***n25po***, and ***n28*** is modified to the primary input ***n28pi*** and the primary output ***n28po***. Each value assignment probability of the primary inputs of Fig.4 is as follows. ***PA(n1)*** =60.48%, ***PA(n2)*** =40%, ***PA(n3)*** =48.57%, ***PA(n4)*** =63.33%, ***PA(n25pi)*** =39.52%, and ***PA(n28pi)*** =31.91%. The maximum value of the value assignment probabilities of primary inputs can be reduced from 100% to 63.33% by inserting test points into ***n25*** and ***n28***.

3-3. DFT Strategy 2

(1) The Algorithm of DFT Strategy 2

Fig.5 illustrates the algorithm of DFT strategy 2 which uses the partial scan design method. First, the number of ATPG patterns is calculated by applying the full scan design method to each block and by performing ATPG for each block. (the 3rd line of Fig.5). The inputs and outputs of the blocks are considered as the primary inputs and outputs, respectively. Next, the block with the maximum number of ATPG patterns is selected as a target block (B_{fs}) of full scan design (the 4th line of Fig.5). The number of ATPG patterns of B_{fs} will increase further if the partial scan design method is applied to B_{fs}. In DFT strategy 2, our purpose is to keep the number of ATPG patterns of an LSI. Therefore, the full scan design method is applied to B_{fs} (the 9th line of Fig.5). The partial scan design method is applied to other blocks (the 13th line of Fig.5), ATPG is performed, and the number of ATPG patterns is calculated (the 14th line of Fig.5). Here, let ***TP(B)*** be the number of ATPG patterns of block ***B***. The numbers

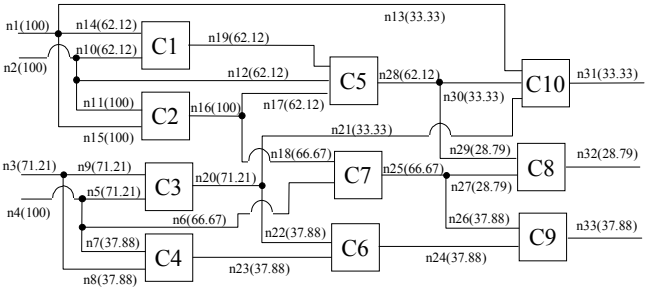

Fig.3 Combinational circuit before test point insertions

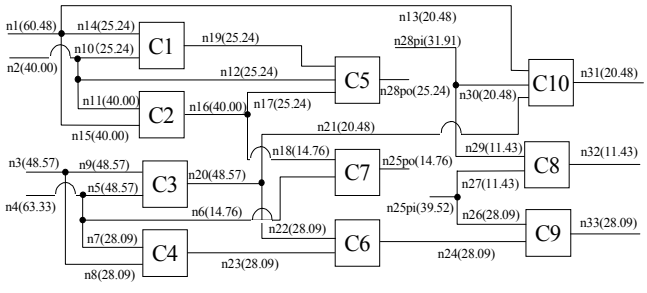

Fig.4 Combinational circuit after test point insertions

```
1:  DFT Strategy 2 ( )
2:  {
3:      Calculate the full scan ATPG patterns for all blocks.
4:      Select the full scan design block B_fs that has the maximum ATPG
          pattern.
5:      for (each block)
6:      {
7:          if (B_i == B_fs)
8:          {
9:              Apply full scan design method to B_fs.
10:         }
11:         else
12:         {
13:             Apply partial scan design method to B_i.
14:             Calculate the partial scan ATPG pattern for B_i.
15:             while (TP(B_i) > TP(B_fs) )
16:             {
17:                 Add scan FFs to B_i in order to make the sequential
                    depth of B_i shallow.
18:             }
19:         }
20:     }
21: }
```

Fig.5 Algorithm of DFT Strategy 2

```
1:  DFT Strategy 3 ( )
2:  {
3:      Calculate the full scan ATPG patterns for all blocks.
4:      Select the test point insertion block B_tpi that has the maximum ATPG
          pattern.
5:      Apply full scan design method B_tpi
6:      Insert test points into B_tpi.
7:      Calculate the full scan ATPG pattern for B_tpi.
8:      Set the number of ATPG patterns of a block that has the maximum ATPG
          pattern into T_max.
9:      for (each block except B_tpi)
10:     {
11:         Apply partial scan design method to B_i.
12:         Calculate the partial scan ATPG pattern for B_i.
13:         while (TP(B_i) > T_max )
14:         {
15:             Add scan FFs to B_i in order to make the sequential depth of B_i
                shallow.
16:         }
17:     }
18: }
```

Fig.6 Algorithm of DFT Strategy 3

of ATPG patterns of blocks except B_{fs} must not exceed $TP(B_{fs})$ so that $TP(B_{fs})$ is nearly equal to the number of ATPG patterns of an LSI from **Assumption 1**. Thus, this algorithm takes notice that the numbers of ATPG patterns of partial scan design blocks must not exceed $TP(B_{fs})$ (from 15th line to the 18th line of Fig.5). By applying the partial scan design method to blocks except B_{fs}, the number of scan FFs on an LSI is reduced. Thus, the shorting of the maximum scan path length reduces TL of the formula (1).

(2) The Basic Concept of the Partial Scan Design method

This partial scan design method selects FFs to replace with scan FFs so that circuit structure has acyclic structure [8-11] in order to guarantee high fault efficiency. Moreover, the fault in an acyclic sequential circuit has the feature[2] that it is detectable with the number of ATPG patterns which is not more than sequential depth [2, 6]+1 of the circuit. Therefore, the number of ATPG patterns for one fault can be reduced by making a sequential depth of a circuit shallow. Moreover, in the partial scan design method, ***output FFs*** of a block have to be replaced with scan FFs as described in section 3-1. When the number of ATPG patterns of a partial scan design block exceeds $TP(B_{fs})$, scan FFs are added to the block in order to make the sequential depth of a circuit shallow.

3-4. DFT Strategy 3

Fig.6 illustrates the algorithm of DFT strategy 3 which uses the partial scan design method with test point insertions. First, the number of ATPG patterns is calculated by applying the full scan design method to each block and by performing ATPG for each block. (the 3rd line of Fig.6). The inputs and outputs of the blocks are considered as the primary inputs and outputs, respectively. Next, the block with the maximum number of ATPG patterns is selected as a target block (B_{tpi}) of test point insertions (the 4th line of Fig.6). Next, the full scan design is applied to B_{tpi} (the 5th line of Fig.6), test point insertion is performed for B_{tpi} (the 6th line of Fig.6), ATPG is performed for B_{tpi}, and the number of ATPG patterns is calculated (the 7th line of Fig.6). The maximum number of ATPG pattern is set into T_{max} (8th line of Fig.6). Next, the partial scan design method is applied to other blocks (the 11th line of Fig.6), ATPG is performed, and the number of ATPG patterns is calculated (the 12th line of Fig.6). The numbers of ATPG patterns of blocks must not exceed T_{max} so that T_{max} is nearly equal to the number of ATPG patterns of an LSI. Thus, this algorithm takes notice that the numbers of ATPG patterns of partial scan design blocks must not exceed T_{max} (from 13th line to the 16th line of Fig.6). By inserting test points for B_{tpi}, the number of ATPG patterns of an LSI can be reduced. By applying the partial scan design method to blocks except B_{tpi}, the number of scan FFs on an LSI can be reduced. Thus, the shortening of the maximum scan path length and the reduction of the number of ATPG patterns of B_{tpi} reduce TL of the formula (1).

4. EXPERIMENTAL RESULTS

In this section, the experimental results of the three DFT strategies are described by applying them to the practical LSIs. Platform of experiments is as follows.

CPU: Ultra SPARC II,

Frequency: 450MHz,

and SPECint@19.7.

4-1. Experimental Circuits

The characteristic of the LSIs is shown in Table1. LSI, #GATE, #PI, #PO, #PIO and #FF denote the circuit names, the numbers of

gates, the numbers of primary inputs, the numbers of primary outputs, the numbers of bi-directional external pins and the numbers of FFs, respectively.

4-2. Experimental Results of DFT Strategy 1

We applied DFT strategy 1 to #1, #2 and #3. Table2, Table3 and Table4 show the characteristic and the results of the full scan ATPG of the blocks included in #1, #2 and #3, respectively. We did not show small blocks that the numbers of FFs are less than 100. BLOCK, #SFF, FE and #TP mean the names of blocks, the numbers of scan FFs, the fault efficiencies, and the numbers of ATPG patterns, respectively. In Table2, the number of ATPG pattern of B15 was the maximum. Thus, B15 was selected as a test point insertion block. Similarly, B28 was selected in #2, and B33 was selected in #3.

Table 5 shows the results of the full scan ATPG for test point insertion blocks. #TPI, FE, #TP, BPA and APA mean the numbers of test points, the fault efficiencies, the numbers of ATPG patterns, the maximums of value assignment probabilities of inputs of the blocks before test point insertions, and the maximums of value assignment probabilities of inputs of the blocks after test point insertions. One test point consists of a scan FF and a 2-input-multiplexer. Test points were inserted into fanout stems whose value assignment probabilities were 60% or more and whose levels were multiples of n until the maximums of value assignment probabilities of inputs of the blocks were reduced by 70% or less. First, 16 was set into n, Second, 8 was set into n, and finally 4 was set into n. The numbers of test points were 1 to 6.2% of the total number of FFs on LSIs, and the test point insertions could reduce the maximums of the value assignment probabilities of inputs of the blocks by 46 to 68%. It reduced the number of ATPG patterns by 44 to 80%.

Table6 shows the comparison between the results of ATPG for full scan design circuits including the test points and the original full scan design circuits. In Table6, DFT, #SP, MSL, TL, RR, CPU denotes DFT methods, the numbers of scan paths, the maximum scan path lengths, the test lengths of an ATE, the rate of the reduction of the test length, and ATPG times, respectively. Here, RR is defined as the following formula (2).

$$RR = \{ (TL \text{ of Full Scan}) - (TL \text{ of Full Scan with TPI}) \} / (TL \text{ of Full Scan}) \quad \ldots(2)$$

Table1. Characteristics of LSIs

LSI	#GATE	#PI	#PO	#PIO	#FF
#1	103127	48	12	19	6957
#2	433469	11	10	114	30930
#3	863834	8	97	67	52849

Table2. ATPG results for full scan design blocks in #1

BLOCK	#SFF	FE(%)	#TP
B11	134	100	71
B12	501	100	873
B13	671	100	248
B14	1550	100	49
B15	1720	100	1030
B16	2381	100	114

Table3. ATPG results for full scan design blocks in #2

BLOCK	#SFF	FE(%)	#TP
B21	738	99.82	242
B22	1226	99.75	504
B23	1226	99.97	213
B24	1316	99.98	984
B25	1710	99.94	212
B26	3266	99.99	760
B27	3744	99.93	362
B28	4569	99.93	2602
B29	5363	99.94	284
B210	7671	100	37

Table4. ATPG results for full scan design blocks in #3

BLOCK	#SFF	FE(%)	#TP
B31	12469	99.88	1493
B32	12469	99.88	1493
B33	12916	99.89	7192
B34	14478	99.89	1423

Table 5. ATPG results for full scan design blocks with test point insertions

BLOCK	#TPI	FE(%)	#TP	BPA(%)	APA(%)
B15	122	100	743	77.98	52.76
B28	1562	99.97	1646	71.63	45.52
B33	3231	100	2386	97.30	44.02

Table 6. ATPG results for full scan design LSIs with test point insertions

LSI	DFT	#SFF	#SP	MSL	FE(%)	#TP	TL(10^6)	RR(%)	CPU(s)
#1	Full Scan	6957	16	435	99.95	1164	0.508	0	1856
	Full Scan with TPI	7081	16	443	99.99	929	0.413	18.70	1825
#2	Full Scan	30930	31	998	99.62	2826	2.824	0	14599
	Full Scan with TPI	32483	31	1049	99.64	1942	2.040	27.76	14741
#3	Full Scan	52849	64	814	99.69	7142	5.822	0	70767
	Full Scan with TPI	56080	64	877	99.68	3022	2.654	54.41	62421

As shown in Table 6, DFT strategy 1 could shorten the test lengths by 46 to 82% as compared with those of the full scan design method. In Table5, the number of ATPG patterns of B15 was smaller than that of B12 shown in Table 2. Since the number of ATPG pattern of B12 is nearly equal to that of #1, the RR of #1 was lower than that of B15.

4-3. Experimental Results of DFT Strategy 2

Next, we applied DFT strategy 2 to #1 and #2. In #3, because the ratio of the number of scan FFs to all FFs was more than 90%, the experimental result would not be shown in this paper. In Table2, the number of ATPG patterns of B15 was the maximum, thus B15 was selected as a full scan design block. Similarly, B28 was selected in #2.

The partial scan ATPG is performed for blocks except the full scan design blocks. All partial scan design blocks satisfied the following two conditions.

(Condition 1) Fault efficiency of each block is more than 99.5%.

(Condition 2) The number of *ATPG patterns* for each block is less than that of B_{fs}.

Partial scan design LSIs can obtain the same fault efficiency as full scan design LSIs by satisfying Condition 1, and the number of ATPG patterns of B_{fs} will be nearly equal to that of an LSI by satisfying Conditions 2. When not satisfying either of two conditions, scan FFs were added in order to make the sequential depths of blocks shallow. Table 7 shows the result of ATPG for the partial scan design LSIs in comparison with those for full scan design LSIs. As shown in Table7, DFT strategy 2 can shorten the test lengths by 58 to 63% as compared with the those of the full scan design method.

4-4. Experimental Results of DFT Strategy 3

Next, we applied DFT strategy 3 to #1 and #2. In Table2, the number of ATPG patterns of B15 is the maximum, thus B15 was selected as a test point insertion block. Similarly, B28 was selected in #2.

After the test point insertions, the maximum numbers of ATPG patterns of blocks are set into T_{max}s. T_{max} of #1 was 873 (#TP of B12 shown in Table 2) and T_{max} of #2 was 1646 (#TP of B28 shown in Table 5). The numbers of ATPG patterns of B16(918) and B29(2227) that are the partial scan design blocks exceeded T_{max}s of #1 and #2, respectively. We added 62 scan FFs to B16 in order to make the sequential depth of B16 shallow from 29 to 15. In the same way, we added 331 scan FFs to B29 in order to make the sequential depth of B29 shallow from 5 to 3. #TP(499) of B16 became less than T_{max} (873) of #1 and #TP(1022) of B29 became less than T_{max} (1646) of #2.

Table8 shows the results of ATPG for the partial scan design LSIs with test point insertions in comparison with those for full scan design LSIs. As shown in Table 8, DFT strategy 3 can shorten the test length by 49 to 55% as compared with the case of the full scan design method.

Table 7. ATPG results for partial scan design LSIs

LSI	DFT	#SFF	#SR(%)	#SP	MSL	FE(%)	#TP	TL(10^6)	RR(%)	CPU(s)
#1	Full Scan	6957	100	16	435	99.95	1164	0.508	0	1856
	Partial Scan	3881	55.79	16	243	99.88	1192	0.291	42.72	3999
#2	Full Scan	30930	100	31	998	99.62	2826	2.824	0	14599
	Partial Scan	19346	62.55	31	625	99.36	2828	1.771	37.29	62189

Table 8. ATPG results for partial scan design LSIs with test points

LSI	DFT	#SFF	#SR(%)	#SP	MSL	FE(%)	#TP	TL(10^6)	RR(%)	CPU(s)
#1	Full Scan	6957	100	16	435	99.95	1164	0.508	0	1856
	Partial Scan with TPI	4067	57.44	16	255	99.92	1073	0.275	45.87	2045
#2	Full Scan	30930	100	31	998	99.62	2826	2.824	0	14599
	Partial Scan with TPI	21240	64.71	31	686	99.39	1998	1.373	51.37	62377

5. CONCLUSION

In this paper, we proposed three DFT strategies:

(1) DFT strategy 1: the full scan design method with test point insertions.

(2) DFT strategy 2 : the partial scan design method.

(3) DFT strategy 3 : the partial scan design method with test point insertions.

These strategies are based on the assumption that the maximum number of ATPG patterns of blocks is nearly equal to the ATPG patterns of an LSI. We compared the strategies and the full scan design method experimentally and we found following results.

(1) the test lengths were shortened by 46 to 82%. (DFT strategy 1)

(2) the test lengths were shortened by 58 to 63%. (DFT strategy 2)

(3) the test lengths were shortened by 49 to 55%. (DFT strategy 3)

Moreover, we proposed the value assignment probability, which expresses the compaction efficiency of test patterns as a cost function of the test point insertion in order to reduce the number of ATPG patterns.

Our future works are:

(1) developing an excellent algorithm for test point insertion to reduce the number of test points.

(2) developing a new DFT strategy which is took Built-In Self Test (BIST) [4] into consideration.

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