

KSim: A Stable and Efficient *RKC* Simulator for Capturing On-Chip Inductance Effect *

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Abstract— On-chip inductance extraction is difficult due to the global effect of inductance, and simulating the resulting dense partial inductance matrix is even more difficult. Furthermore, it is well known that simply discarding smallest terms to sparsify the inductance matrix can render the partial inductance matrix indefinite and result in an unstable circuit model. Recently a new circuit element, K , has been introduced to capture global effect of inductance by evaluating a corresponding sparse K matrix [1]. However, the reason that K has such local properties is not clear, and the positive semi-definiteness of the corresponding sparse K matrix is not proved. In this paper, we present the physical interpretation of K . Based on the physical interpretation, we explain why the faraway mutual K can be ignored (locality) and prove that after ignoring faraway mutual K , the resultant K matrix is positive definite (stability). Together with a *RKC* equivalent circuit model, the locality and stability enables us to simulate *RKC* circuit directly and efficiently for real circuits. A new circuit simulation tool, KSim, has been developed by incorporating the new circuit element K into Berkeley SPICE. The *RKC* simulation matches better with the full partial inductance matrix simulation with significant less computing time and memory usage, compared to other proposed methods, such as shift-truncate method [2, 3].

I. INTRODUCTION

Modeling of inductance effect of on-chip wiring is becoming increasingly important as clock speeds increase and less resistive lines are used to improve signal propagation speed.

To model inductance of general 3D interconnect for which the return paths are not known requires employing partial inductance elements. The partial inductance concept, which was developed by Rosa [4], was introduced to the circuit design field by Ruehli [5, 6]. Because partial inductances obey the same branch constitutive relations as closed-loop inductances, they can be conveniently applied in the context of modified nodal analysis and used internally in circuit simulators such as SPICE.

However, since the actual current and flux linkage loops are unknown, partial inductance is defined by the flux created by

an aggressor segment through the virtual loop which a victim segment forms at infinity. Therefore, instead of coupling among all of the loops, there is now coupling among all of the wire segments. This corresponds to an extremely large, dense, partial inductance matrix. Because it is difficult to invert (or factor) a large dense matrix in circuit simulation, it is often desirable to sparsify the partial inductance matrix.

One straight forward approach to make the inductance matrix sparse and, therefore, more tractable is simply to discard those mutual coupling terms of the partial inductance matrix which are below a certain threshold. This approach, however, does not guarantee the positive semi-definiteness of the resulting inductance matrix [3].

A couple of approaches were later proposed to generate sparse approximations with guaranteed stability, such as, the shift-truncate potential method [2, 3], and “return-limited loop inductance” concept [7]. However, the accuracy of both approaches are sensitive to the interconnects topology.

Recently, a new circuit element was introduced to represent inductance effect, while still preserve the C -like locality [1]. This new circuit element, K , is basically the inverse of partial inductance. It was proposed to capture on-chip inductance effect by directly extracting and simulating K , instead of partial inductance.

However, the physical meaning of K and the reason that K has C -like locality is not clear. Furthermore, the stability of the sparse system matrix constructed by ignoring far away mutual K has not been proved yet, which limits the application of K in real situation.

In this paper, we present the theoretical background of this new circuit element K . We provide the physical meaning of K and explain why K has local property like capacitance. We also prove that the sparse system matrix constructed by ignoring faraway mutual K is positive definite. That is to say, the subsequent *RKC* equivalent circuit is guaranteed to be stable. Finally, we develop a simulator, KSim, to directly simulate *RKC* equivalent circuit by integrating the transient model of K with Berkeley SPICE.

We compare the full partial inductance matrix method and the K -based method, together with the truncation only and shift-truncate techniques, in terms of circuit simulation results on practical examples. The K -based method shows great advantages over the truncation only and shift-truncate techniques

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in terms of accuracy and efficiency.

II. PHYSICAL MEANING OF NEW CIRCUIT ELEMENT K

The original definition of $[K]$ is the inverse of partial inductance matrix $[L]$ [1].

$$[K] = [L]^{-1} \quad (1)$$

In magneto-statics, the element of L matrix has the following formulation [5],

$$L_{ij} = \frac{\mu_0}{4\pi a_i a_j} \left[\int_{a_i} \int_{a_j} \int_{l_i} \int_{l_j} \frac{d\mathbf{l}_i \cdot d\mathbf{l}_j}{r_{ij}} da_i da_j \right] \quad (2)$$

where a_i and a_j are cross sections of segment i and j , respectively, and r_{ij} is the geometric distance between two points in segment i and j .

The partial inductance matrix for a set of n conductors is a $n \times n$ real symmetric matrix. The corresponding linear system is given by

$$\begin{bmatrix} L_{11} & L_{12} & \cdots \\ L_{21} & L_{22} & \cdots \\ \vdots & \vdots & L_{nn} \end{bmatrix} \begin{bmatrix} I_1 \\ \vdots \\ I_n \end{bmatrix} = \begin{bmatrix} \sum_{i=1}^n \left(\frac{1}{a_1} \int \mathbf{A}_{1i} \cdot d\mathbf{l}_1 da_1 \right) \\ \vdots \\ \sum_{i=1}^n \left(\frac{1}{a_n} \int \mathbf{A}_{ni} \cdot d\mathbf{l}_n da_n \right) \end{bmatrix} \quad (3)$$

where A_{1i} is the magnetic vector potential along segment 1 due to the current I_i in segment i .

Therefore, K satisfies the following linear equations,

$$\begin{bmatrix} K_{11} & K_{12} & \cdots \\ K_{21} & K_{22} & \cdots \\ \vdots & \vdots & K_{nn} \end{bmatrix} \begin{bmatrix} \sum_{i=1}^n \left(\frac{1}{a_1} \int \mathbf{A}_{1i} \cdot d\mathbf{l}_1 da_1 \right) \\ \vdots \\ \sum_{i=1}^n \left(\frac{1}{a_n} \int \mathbf{A}_{ni} \cdot d\mathbf{l}_n da_n \right) \end{bmatrix} = \begin{bmatrix} I_1 \\ \vdots \\ I_n \end{bmatrix} \quad (4)$$

From Eq. (4), it is observed that K is best understood in terms of normalized current induced by the magnetic vector potential drop along a set of conductor segments. However, unlike the extraction of partial inductance, in which we can directly calculate L_{ij} using analytical formula, K does not have such simple formulation. The calculation of each element in K matrix involves solving linear systems.

If we set the magnetic vector potential drop along conductor segment j to be 1, and the magnetic vector potential drops along all other conductor segments to be 0, then we can solve the current induced in each conductor segment, given the relationship between the magnetic vector potential drop and current,

$$A_{ij} = \frac{\mu_0}{4\pi a_j} \left[\int_{a_j} \int_{l_j} \frac{\mathbf{I}_j}{r_{ij}} d\mathbf{l}_j da_j \right] \quad (5)$$

From Eq. (4), we can see that the current induced in each conductor segment in this case is equal to each element in the column j of the K matrix. Therefore, we can redefine the element of K matrix as: *the element K_{ij} is the current flowing through the i^{th} conductor when the magnetic vector potential drop along all conductors, except the j^{th} , are set to zero, and the magnetic vector potential drop along the j^{th} conductor is raised to unit potential.*

This definition illustrates both the physical meaning of K matrix and how it can be calculated. That is, iteratively assigning the magnetic vector potential drop along conductor segment i , ($i = 1, 2, \dots, n$), to be 1, while the magnetic vector potential drops along all other conductor segments to be 0, we can obtain each column i of the K matrix through calculating the induced current in each conductor segments. In fact, this scheme resembles the capacitance calculation in electrostatics.

In next section, we will further introduce the C -like properties of K matrix, such as locality and positive definiteness.

III. LOCALITY AND STABILITY OF K MATRIX

In fact, the definition and physical explanation of K matrix is so similar to that of capacitance matrix, where the magnetic vector potential drop along a conductor segment resembles voltage drop, and the current in the conductor segment resembles the charge on the surface of the conductor. We can expect that K matrix has C -like properties. The proof for stability of K matrix also resembles the proof for capacitance matrix stated in [8].

Because orthogonal conductors do not couple magnetically, the resulting partial inductance matrix and K matrix are block diagonal matrices. Therefore, in following proof we only need to consider a set of parallel conductors. The proof can also be easily extended to structures with lean conductors, which is omitted here due to space limitation.

A. Locality

Although the calculation of K matrix involves solving linear systems, it is possible to learn a great deal about the K matrix and its elements by appealing to simple physical principles. Through the application of Green's Theorem it can be shown that the K matrix is symmetric:

$$K_{ij} \equiv K_{ji} \quad (6)$$

Next, suppose that the magnetic vector potential drop along the i^{th} conductor is assigned some positive value, and the magnetic vector potential drop along all of the other conductors are kept zero. In order for the magnetic vector potential drop along the i^{th} conductor to be positive, it must carry a current at the same direction as the magnetic vector potential drop. Thus it must be true that

$$K_{ii} > 0 \quad (7)$$

Moreover, in order for the magnetic vector potential drop along the other conductors to remain at zero, they must carry

currents at the opposite direction as the magnetic vector potential drop along the i^{th} conductor. Hence,

$$K_{ij} < 0, \quad i \neq j \quad (8)$$

One may doubt how can current flow in opposite directions in different segments of a same conductor, when a long conductor broken into several segments is under consideration. In this case, we can assume that there are infinite thin gaps between any two neighbor segments, which will not alter the partial inductance matrix or K matrix, while leave the current direction in each segment undetermined.

Therefore, if we assign some positive value to the magnetic vector potential drop along one aggressor conductor, and keep the magnetic vector potential drop along all other neighbor conductors as zero, as we stated above, the current induced on the neighbors are at the opposite direction as the current induced on the aggressor conductor. Same applies to the magnetic field generated by the currents. Therefore, the magnetic field generated by each neighbor cancels part of the field induced on the aggressor line, and shields the field induced on the aggressor line to go further, shown in Fig. 1. That is the physical explanation of the locality of K matrix.

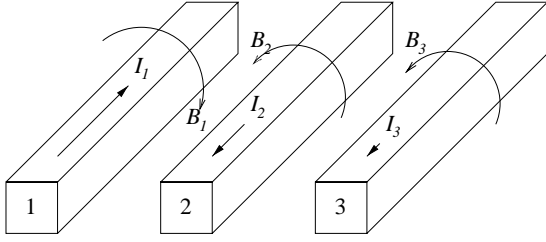


Fig. 1. Layout Example with Three Parallel Buses

Since K has C -like locality, we only need to consider a small number of neighbors in K -based method when capturing inductance effect of on-chip interconnect. The K -based method can be summarized as follows.

- Calculate the partial inductance matrix, L , of a small structure which is enclosed in a small window.
- Calculate the small K matrix by inverting the corresponding L matrix.
- Compose the big K_{all} matrix by the column in each small K matrix, which is corresponding to the aggressor, like the general techniques used in capacitance extraction.
- Simulate the subsequent RKC equivalent circuit.

Therefore, for a large system, this approach will generate a very sparse K matrix in later circuit simulation. As the next step, we need to prove the stability of this sparse system matrix.

B. Stability

Consider the situation in which the magnetic vector potential drop on all n conductors are raised to unit (positive) potential at the same direction. Then the flux, Φ , through the loop composed by any pair of conductors is zero. According to original definition of loop inductance, we have

$$\Phi = L_{loop}I \quad (9)$$

where I is the current flow through this loop. We can see that the current that flow through the loop composed by any pair of conductors is also zero, since L_{loop} is not zero. That is to say, no current induced in one conductor returns through any other conductor in this case. Thus, all the currents induced from the magnetic vector potential drop have to return from the infinity (or, in reality, return from other ports or terminals). Therefore we can conclude that the current induced in each conductor has same direction as the potential drop. From Eq. (4) with $\sum_{j=1}^n \left(\frac{1}{a_i} \int \mathbf{A}_{ij} \cdot d\mathbf{l}_i da_i \right) = 1$, for $i = 1, 2, \dots, n$, we get

$$I_i = \sum_{j=1}^n K_{ij} > 0 \quad i = 1, 2, \dots, n \quad (10)$$

Since $K_{ii} > 0$, and $K_{ij} < 0$ for $i \neq j$, it follows from Eq. (10) that

$$K_{ii} > \sum_{j=1, j \neq i}^n |K_{ij}| \quad (11)$$

which is the property known as strict diagonal dominance.

According to Gersgorin Circle Theorem, each eigenvalue of a square matrix, $A = (a_{ij})$, of order n is in at least one of the disks in complex plane

$$\{z : |z - a_{ii}| \leq R_i\}, \quad R_i = \sum_{j=1, j \neq i}^n |a_{ij}|, \quad i = 1, 2, \dots, n \quad (12)$$

That is to say, all the eigenvalues are in the set of disks, which is centered at the diagonal element, a_{ii} , with the radius of the summation of the absolute value of off-diagonal elements in row i , $i = 1, 2, \dots, n$. If A is strict diagonal dominant,

$$R_i = \sum_{j=1, j \neq i}^n |a_{ij}| < |a_{ii}|, \quad i = 1, 2, \dots, n \quad (13)$$

and $|a_{ii}| > 0$, we can know that all the disks of A matrix lie in the right-hand side of the complex plane, so do the eigenvalues. Therefore, *A matrix is positive definite if A is strict diagonal dominant and all the diagonal elements are positive.*

The property of strict diagonal dominance holds in K extraction for whatever number of conductors and whatever the window size is. Therefore, each small K matrix is strict diagonal dominant. Using K -based method, the sparse K_{all} matrix for the whole system is still strict diagonal dominant, since each column of K_{all} matrix is composed by the corresponding column of the small K matrix and some fill-in zeros. Together with the property of Eq. (7), thus, we can guarantee the positive definiteness or stability of the sparse K_{all} matrix.

IV. EQUIVALENT CIRCUIT MODEL OF K FOR TRANSIENT ANALYSIS

Since the sparse K matrix produced by K -based method is guaranteed the stability, we can now take advantage of K with confidence. Since K is a newly defined circuit element, the conventional SPICE does not support it. To best utilize the sparsity of K system matrix, however, we have to simulate K matrix directly, instead of its inverted version L matrix which is known to be dense. Therefore, in this section, we discuss the equivalent circuit model of K for transient analysis.

Since K is the inverse of L , consequently, the branch equation for this new element K is

$$KV = \frac{dI}{dt} \quad (14)$$

which is again the inverse linear system of L .

For transient circuit analysis, if we apply the backward Euler method, it is assumed that the time derivative of current, $\frac{dI}{dt}$, is constant over the time interval $[kh, (k+1)h]$, and it is given by

$$\frac{dI}{dt} = \frac{I^{k+1} - I^k}{h} \quad (15)$$

where h is the chosen step size, I^k is known, while I^{k+1} is to be calculated.

For the circuit example shown in Fig. 2, the circuit differential equations are written as

$$\begin{cases} K_{11}V_1 + K_{12}V_2 = dI_1/dt \\ K_{21}V_1 + K_{22}V_2 = dI_2/dt \end{cases} \quad (16)$$

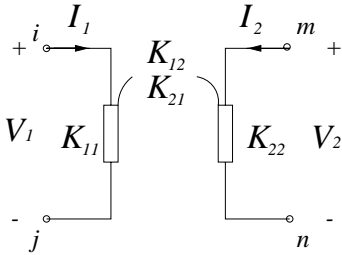


Fig. 2. Circuit Example with mutual K

Using the backward Euler method, *i.e.*, substitute Eq. (15) into Eq. (16), we can obtain

$$\begin{cases} I_1^{k+1} = K_{11}hV_1^{k+1} + K_{12}hV_2^{k+1} + I_1^k \\ I_2^{k+1} = K_{21}hV_1^{k+1} + K_{22}hV_2^{k+1} + I_2^k \end{cases} \quad (17)$$

Therefore, the transient equivalent model of K is composed of one resistor, one voltage control current source, and one independent current source in parallel, shown in Fig 3.

We also derive the equivalent circuit model of K according to the Trapezoidal method. It is also composed of one resistor, one voltage control current source, and one independent

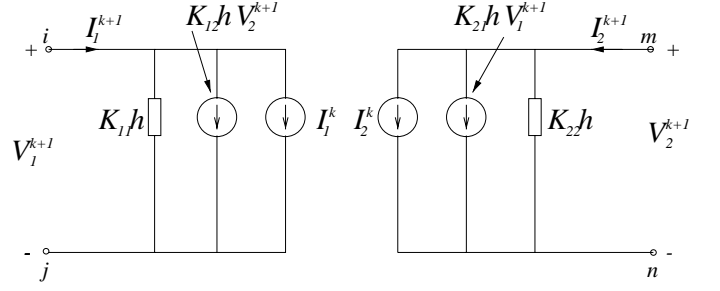


Fig. 3. Equivalent Circuit Model for Circuit Example in Fig. 2 for Transient Analysis

current source in parallel. The resistor and the voltage control current source in this Trapezoidal method are of half value of those in Euler method, respectively. The independent current source has the expression of $0.5 * K_{i1}hV_1^k + 0.5 * K_{i2}hV_2^k + I_i^k$, $i = 1, 2$, for the two branches, respectively.

We add K as a new device in Berkeley SPICE according to its transient model in both Euler method and Trapezoidal method, and switch between these two methods according to the convergence speed automatically. We call this modified SPICE as KSim, since it can directly simulate RKC circuit model.

V. EXPERIMENT RESULTS

Consider the layout example with three parallel buses, shown in Fig. 1. The length of each bus is $20 \mu\text{m}$, the cross section is $2 \times 2 \mu\text{m}$, and the spacing between the buses is $5 \mu\text{m}$.

We calculate the partial inductance matrix, L , using FastHenry [9],

$$[L] = \begin{bmatrix} 11.4 & 4.26 & 2.54 \\ 4.26 & 11.4 & 4.26 \\ 2.54 & 4.26 & 11.4 \end{bmatrix} \text{ pH}, \quad (18)$$

and then inverted L to get K matrix.

$$[K] = \begin{bmatrix} 103 & -34.7 & -9.93 \\ -34.7 & 114 & -34.7 \\ -9.93 & -34.7 & 103 \end{bmatrix} \times 10^9 H^{-1} \quad (19)$$

If we remove the center conductor 2, and recalculate the corresponding L and K matrix,

$$[L] = \begin{bmatrix} 11.4 & 2.54 \\ 2.54 & 11.4 \end{bmatrix} \text{ pH}, \quad (20)$$

$$[K] = \begin{bmatrix} 92.2 & -20.5 \\ -20.5 & 92.2 \end{bmatrix} \times 10^9 H^{-1}. \quad (21)$$

It's observed that the removal of conductor 2 has no effect on the mutual partial inductance between conductor 1 and 3, while the mutual K between conductor 1 and 3 is increased by

$\frac{20.5-9.93}{9.93}$ or 106%. This example demonstrates the shielding effect of conductor 2 for the mutual K between conductor 1 and 3.

To compare the efficiency and accuracy of K -based method and other sparsification approaches, we chose a periodic signal bus structure similar to that presented in Fig. 7(b) of He's paper [3]. The circuit is depicted in Fig. 4. We deliberately chose this circuit topology because all the signal lines share one return path. It was shown to be difficult to capture the inductance effect with far away current return path in He's paper [3], since the inductive coupling between more periods has to be taken into account in partial inductance sparsification. To magnify the distance to the current return path, we pick bigger dimensions than "real" on-chip interconnects in this example. The length of all 30 wires is 40 cm, the cross-section is 2x2 mm, and the spacing between the wires is 1 cm. Partial inductances and K were derived assuming each conductor was broken into ten equal segments in order to create a large yet illustrative system matrix. In fact, K -based method has neither limitations on the dimension of interconnects, nor assumptions on current return path. Therefore, K -based method is suitable for both on-chip and package applications.

To make the inductive effects dominate, R_s and R_t were set to 1 and 10 ohms, and a slow rise time (10ns) was considered so that capacitive coupling could be ignored for this example. These numbers are referenced from another sparsification approach, shift-truncate method [2].

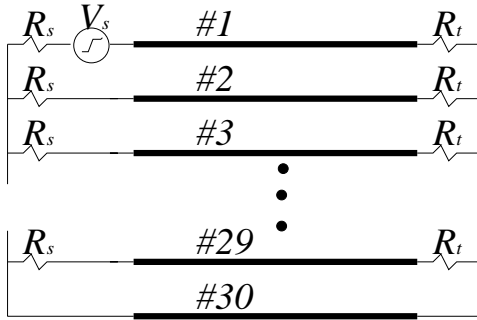


Fig. 4. Circuit Example Similar to Fig. 7 from He's paper[3]

The circuit shown in Fig. 4 was analyzed using four different methods as follows.

- Use full partial inductance matrix.
- Use the shift-truncate method. Since the segment length is 4 cm, to capture enough forwarding magnetic coupling, we had to set the radius of the current return shell to be at least 8.1 cm. Therefore, on the same conductor, two neighbor segments of each side of the aggressor segment were considered to have mutual partial inductance respect to the aggressor segment. In this case, 11,184 of the total 90,000 matrix terms were set to zero (about 87.6% sparse). Here, we can see that the shift-truncate method does not work well for long wires.

- Use the truncation only method. To achieve the same sparsity, 87.6%, as the shift-truncate method, the sparse matrix was formed by discarding all mutual inductances less than 1.9753 nH.
- Use K -based method. Our K matrix was constructed by setting the window size of both segments and different conductors to be 5. That is to say, on the same conductor, two neighbor segments of each side of the aggressor segment were considered to have mutual K respect to the aggressor segment, and two neighbor conductors of each side of the aggressor conductor were considered to have mutual K respect to the aggressor conductor. In this case, 83,664 of the total 90,000 matrix terms were set to zero (about 93% sparse).

To view the inductance effect clearly, we chose the current flow through the R_t which is directly connected to the #2 conductor. The positive current direction is specified as from left to right. The simulation results are depicted in Fig. 5.

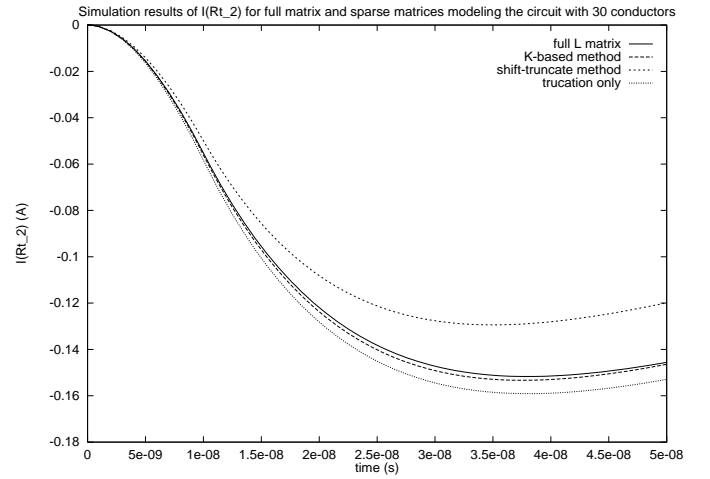


Fig. 5. Simulation results of $I(Rt_2)$ for full matrix and sparse matrices modeling the circuit with 30 conductors

From Fig. 5, we can see that the results of the K -based method matches very well with that of full L matrix simulation, while the results of both shift-truncate method and truncation only method deviate a lot from the full L matrix simulation result. Here, we need to point out that the sparsity of the K matrix is even larger than the partial inductance matrices produced in both shift-truncate method and truncation only method, while still has better agreement in simulation result. Moreover, the difference in the shift-truncate method is even larger than that in truncation only method, which again exposed the shortcoming of the shift-truncate method for handling long wires. Besides, the far away current return path is another reason accounting for the inaccuracy of the shift-truncate method.

From the sparsity of the K matrix, one can imagine the speed up of the circuit simulation using K matrix. The CPU

time and memory usage of the transient simulation using different methods is stored in Table I. Here, note that the generation of K matrix only involves the inversion of very small matrices, 25×25 in this example, the inversion cost can be ignored compared to the inversion (or factorization) of the big K or L matrix in circuit simulation.

TABLE I
CPU TIME AND MEMORY USAGE IN CIRCUIT SIMULATION

Method	CPU time(s)	memory(MB)
full L matrix	743.76	20.13
shift-truncate	144.96	6.00
truncation only	157.36	6.14
K -based method	17.31	3.19

From Table I, we observe that the K -based method can speed up 40 times, and only consume 16% of memory, compared to the original method using full L matrix. Here, although the system matrix generated by the truncation only method is of same sparsity of that generated by the shift-truncate method, the truncation only method need more computer resource than the shift-truncate method. This is because the system matrix generated by the truncation only method is worse-conditioned, if not unstable, than that generated by the shift-truncate method.

VI. CONCLUSIONS

On-chip inductance effect is difficult to capture because the current return path is unknown prior to extraction. Recently a new circuit element, K , has been introduced to capture on-chip inductance effect efficiently without knowing the current return path [1]. In this paper, we provide physical interpretation of K to answer why K has local property, that is, the faraway mutual K can be ignored, and to prove why the RKC simulation is stable, that is the K matrix after ignoring faraway mutual K is positive definite. We have developed a new simulation tool, KSim, by incorporating the circuit element K into Berkeley SPICE. The experimental results indicate that our RKC simulation not only more accurate, but also more efficient, both in terms of time and memory, than other sparsification techniques, such as truncation only method and shift-truncate method [2, 3].

REFERENCES

[1] A. Devgan, H. Ji, and W. Dai, "How to efficiently capture on-chip inductance effect: Introducing a new circuit element K ," in *Proc. IEEE International Conference on Computer Aided Design*, pp. 150–155, Nov. 2000.

[2] B. Krauter and L. Pileggi, "Generating sparse partial inductance matrixes with guaranteed stability," in *Proc. IEEE International Conference on Computer Aided Design*, pp. 45–52, Nov. 1995.

[3] Z. He, M. Celik, and L. Pileggi, "SPIE: Sparse partial inductance extraction," in *Proc. 34-th Design Automation Conference*, pp. 137–140, June 1997.

[4] E. B. Rosa, "The self and mutual inductance of linear conductors," in *Bulletin of the National Bureau of Standards*, pp. 301–344, 1908.

[5] A. E. Ruehli, "Inductance calculations in a complex integrated circuit environment," *IBM Journal of Research and Development*, pp. 470–481, Sept. 1972.

[6] A. E. Ruehli, "Equivalent circuit models for three dimensional multiconductor systems," *IEEE Trans. on MTT*, pp. 216–220, Mar. 1974.

[7] K. L. Shepard and Z. Tian, "Return-limited inductances: A practical approach to on-chip inductance extraction," in *Proc. IEEE Custom Integrated Circuits Conference*, pp. 453–456, 1999.

[8] D. D. Ling and A. E. Ruehli, *Circuit Analysis, Simulation and Design—Advances in CAD for VLSI*. Netherlands: Elsevier Science Publishers B.V., 1987.

[9] M. Kamon, M. J. Tsuk, and J. K. White, "FASTHENRY: A multipole-accelerated 3-D inductance extraction program," *IEEE Trans. on MTT*, pp. 216–220, Sept. 1994.