An On-Chip 96.5% Current Efficiency CMOS Linear Regulator

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Abstract - A proposed linear regulator uses a Flexible Control technique of Output Current (FCOC) to achieve 96.5% efficiency. The FCOC technique realizes to drive a flexible output current according to the output current variation and stable output voltage supply. The linear regulator fabricated by 1.2μm CMOS process occupies 0.423mm^2. The fabricated linear regulator achieves 96.5% current efficiency and less than 6.81mVpp output voltage fluctuation at an output current frequency from 1.8Hz to 100 MHz.

I. Introduction

An on-chip linear regulator with high current efficiency, high packing density and easy implementation to LSIs is needed for single-supply voltage and low-power operation of LSIs. To obtain high-efficiency, DC/DC converters using a fixed Pulse-Width Modulation (PWM) and Divided Switches with Current Control (DSCC) have been reported [1][2]. However, these reported converters cannot realize a high packing density on board and easy implementation to LSIs. Because these reported converters need additional off-chip implementations of inductance, capacitance and pn-diode on board. These additional off-chip implementations require much sacrifice area on board. These are the most important points for practical use. In order to overcome these drawbacks, the specifications for the linear regulator are:

(1) Easy implementation to LSIs,
(2) High current efficiency over 90%
(at Iout=5.7mA, from 5.0V to 3.0V),
(3) Low output noise below 150mVpp.

For (1) to (3), Flexible Control technique of Output Current (FCOC technique) can realize easy implementation to LSIs and high current efficiency. The current efficiency is defined as the ratio of output current (Iout) to the total current of linear regulator (Ivdd), that is (Iout/Ivdd), where Ivdd is the current flowing from Vdd. Moreover, previous reported linear regulators are only applicable to the one with a light load in order to realize a stable output voltage supply and low power operation at the same time. Our proposed linear regulator overcomes the issue by FCOC technique. Therefore, proposed linear regulator is applicable to the one with a more heavy output current in comparison with reported linear regulators. We proposed FCOC technique from above viewpoints and showed a good performance by using circuit simulation [3]-[5]"unpublished"[6]. However, FCOC technique was verified only with circuit simulation. In this paper, we fabricate the linear regulator with FCOC technique using 1.2μm CMOS technology and verify the performance of this linear regulator experimentally. As a result, the on-chip linear regulator using FCOC technique can achieve current efficiency over 96.5%, output noise less than 150mVpp.

II. Flexible Control technique of Output Current (FCOC technique)

The schematic of the proposed linear regulator is shown in Fig. 1. In order to keep the constant output voltage, a linear regulator should perfectly drive the output current which has the same value of the output current. The FCOC technique dynamically drives the output current in seven different stages according to a variation of the output current as shown in Fig. 2. Moreover, the FCOC technique achieves little consumption current even at flowing large output currents. As a result, the on-chip linear regulator using FCOC technique achieves high current efficiency.

An FCOC circuit is shown at Block (A) including three Aj's (j=1,2,3) circuits in Fig. 1. The operation principle of

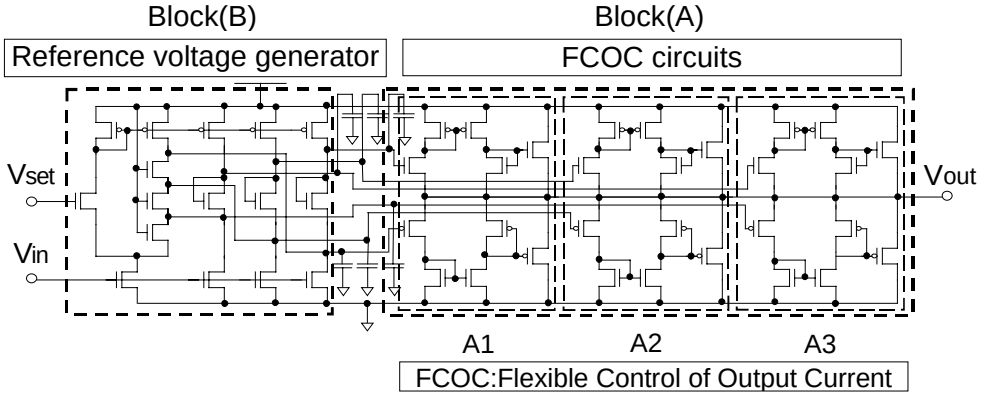

Fig. 1 (a) The schematic of on-chip linear regulator.

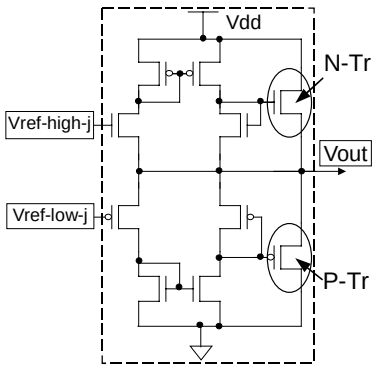

Fig. 1 (b) Aj circuit in FCOC circuits.

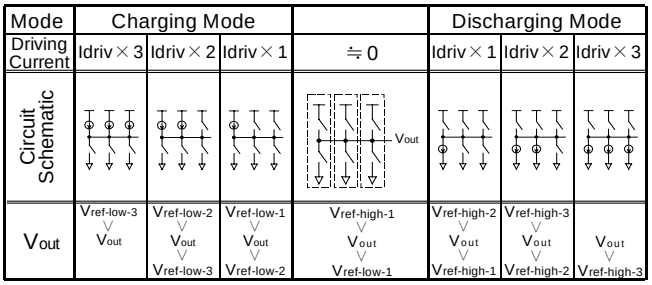

Fig. 2 Operation principle of FCOC technique.

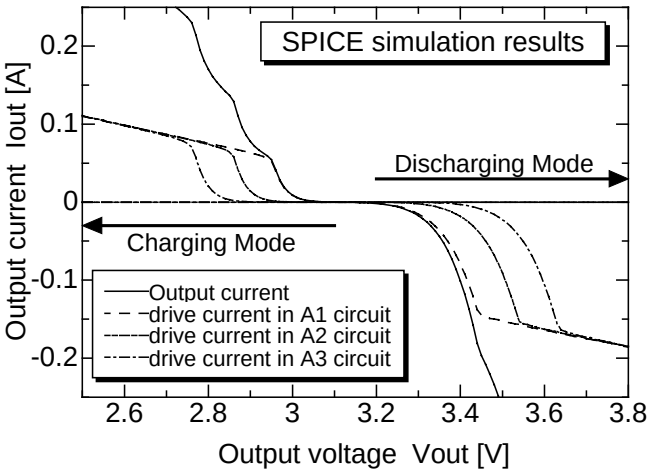

Fig. 3 The SPICE results of output current and driving current in Aj circuit of on-chip linear regulator.

FCOC circuit is shown in Fig. 2. Each Aj circuit consists of an NMOS driver transistor (N-Tr), a PMOS driver transistor (P-Tr) and a current mirror amplifier circuit. Two reference voltages (Vref-high-j, Vref-low-j), which are generated by the reference voltage generator of Block (B), are supplied into the current mirror amplifier circuit in each Aj circuit. Each Vref-high-j is a higher reference voltage for each Aj, and each Vref-low-j is a lower reference voltage for each Aj. When the output voltage is smaller than Vref-low-j, only NMOS driver transistor in the Aj turns on, and PMOS driver transistor in the Aj turns off. On the other hand, when the output voltage is larger than Vref-high-j, only PMOS driver transistor in the Aj turns on, and NMOS driver transistor in the Aj turns off. As a result, the number of charging or discharging current paths at the output node of the linear regulator can be automatically changed according to a variation of the output current. Therefore, the proposed circuit realizes to drive a flexible output current according to the output current variation as shown in Fig. 2. Moreover, little pass-through current flows. Therefore, the consumption current is very small in comparison with the output current.

In Block (A), each transistor in Aj circuit is designed as follows. The total gate size, that is sum over all driver transistors of each Aj, is optimized for an output current of 30mA and an output current-frequency of 100MHz. The gate size of the each driver transistor is determined by the minimum that can supply the 7mA target maximum current within the saturation region of the transistor. The output

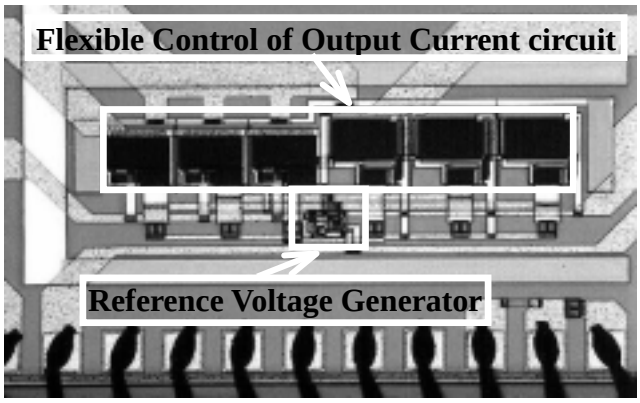

Fig. 4 The chip micrograph : 1.211× 0.35mm^2 die.

current is quickly changed by quick response of the current mirror circuit. The output current Iout is given by Iout=|Ivdd|-|Ivss|, where Ivdd and Ivss are currents flowing from Vdd and Vss, respectively. Each transistor in Block (B) is designed as follows. (1) The six reference voltages, which differ to each other by ±0.1V, are generated from the setting voltage (Vset). (2) The voltage fluctuations of all six reference voltages are suppressed to less than ±17mVpp for a supply voltage ranging from 4.5 V to 5.5 V. The input voltage (Vin) for the reference voltage generator is supplied by an external power source. Vin is set to 1.0V.

As shown in Fig. 3, output current and each driving current of Aj(j=1,2,3) as shown in Fig. 1 are simulated at Vdd=5V and Vset=3V. When the output voltage (Vout) is between 2.9V and 3.0V, only A1 circuit drives the output current with charging the output node. When Vout is between 2.8V and 2.9V, both A1 and A2 drive the output current. When Vout is lower than 2.8V, all A1, A2 and A3 drive the output current. The driving current flows from the power source to the output node of linear regulator. On the other hand, when Vout is between 3.2V and 3.3V, only A1 drives the output current with discharging the output node. When Vout is between 3.3V and 3.4V, both A1 and A2 drive the output current. When Vout is higher than 3.4V, all A1, A2 and A3 drive the output current. This driving current flows from the output node of linear regulator to the ground. Moreover, when Vout is between 3.0V and 3.2V, all A1, A2 and A3 drive no output current to the output node with little consumption current.

III. Fabrication of the Linear Regulator Using FCOC technique

The proposed on-chip linear regulator is fabricated by the 1.2μm CMOS double metal and single polysilicon process. Fig. 4 shows the photomicrograph of the fabricated proposed linear regulator. The number of transistors is 46 and the die size is 0.423mm^2.

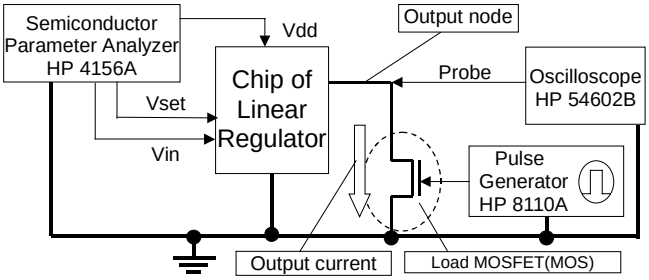

Fig. 5 Measurement setup.

IV. Experimental Results and Discussion

(a) Measurement method

The measurement of this chip is performed as shown in Fig. 5. Since this linear regulator needs the external power supply voltage (Vdd, Vss, Vin and Vset) and the driving current, a semiconductor parameter analyzer (HP4156A) and a pulse generator (HP8110A) are used respectively. The driving current of this chip is controlled by the MOSFET, whose gate voltage is changed by the pulse generator. The output node is connected to the sampling oscilloscope (HP54602B), which has 2GSa/s sampling rate, because the parasitic capacitance for monitor must be small. Therefore, the power consumption current and the output voltage of the linear regulator are monitored at the same time.

(b) Experimental Results and Discussion

Fig. 6 shows the measured dc characteristics of fabricated linear regulator using FCOC technique. X-axis is supply voltage (Vdd), and Y-axis is the output voltage (Vout). This measurement condition is that setting voltage (Vset), as is shown in Fig. 1 is 3.0V.

The reference voltage generator (Block B) suppresses the fluctuation of reference voltages to ±17mVpp against the supply voltage at Vdd=5.0V±0.5V. Therefore, by the six stable reference voltages from Block (B), the linear regulator can supply an output voltage of 2.978V±128mV at Vdd=5.0V±0.5V (also Vdd=4.8V±0.7V). Moreover, at the output voltage range of 5.0V±0.3V, the linear regulator can supply 2.9005V±50mV. The stable output voltage of the linear regulator is realized.

Fig. 7 shows the measurement method of the frequency characteristics of fabricated linear regulator. The gate voltage (Vg) of the MOSFET (MOS) in Fig. 7 used as the load of linear regulator is supplied with a saw tooth waveform by the pulse generator. Therefore, the output current is dynamically changed. By flowing the output current, the output voltage is measured with oscilloscope. By this method, the dependence of the output voltage fluctuation on the output current frequency can be experimentally analyzed.

Fig. 8 shows the characteristic of an output voltage fluctuation for a frequency of an output current that is not zero. In practical use, even if no transistor is active, LSI consumes some leakage current, e.g., pn junction leakage currents, subthreshold leakage currents, and so on. Therefore, output current does not become zero. Under the condition

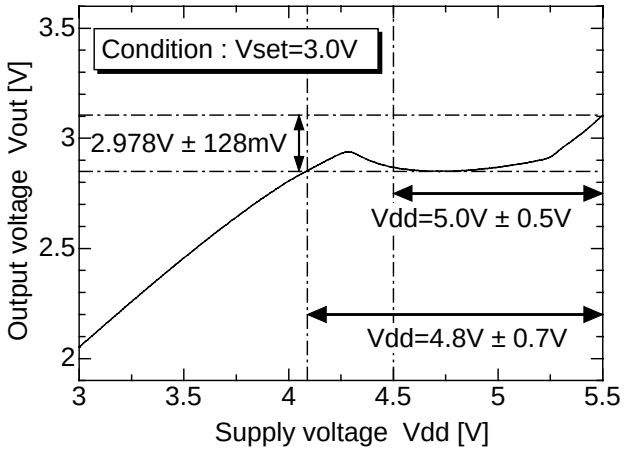

Fig. 6 Measurement dc characteristic of proposed linear regulator with FCOC technique.

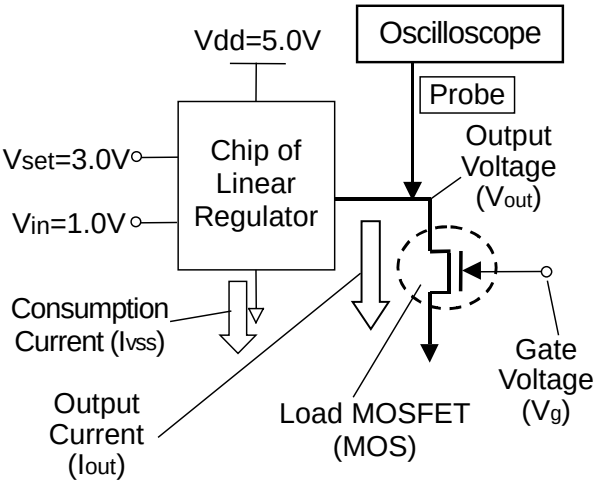

Fig. 7 Measurement method to evaluate frequency characteristic.

that an output current flows, we evaluate the output voltage fluctuation as shown in Fig. 8. Fig. 8(a) shows a measurement output current Iout at a frequency of output current f(Iout)=1.8Hz, which is the drain current of the MOSFET (MOS) in Fig. 7. The maximum current (Iout(max)) is 13.8uA at each output current frequency (f(Iout)) ranging from 1.8Hz to 100MHz. Fig. 8(b) shows a measured output voltage waveform of the fabricated linear regulator at a frequency of output current f(Iout)=1.8Hz. The proposed linear regulator can supply stable output voltage at a frequency of output current f(Iout)=1.8Hz as shown in Fig. 8(b). Fig. 8(c) shows the stability of the output voltage for the output current frequency (f(Iout)) of the fabricated linear regulator. X-axis is the output current frequency (f(Iout)) and Y-axis is the output voltage (Vout). The output voltage, which is the averaged value of the measured waveform, is plotted at each output current frequency (f(Iout)) ranging from 1.8Hz to 100MHz. The maximum output current is 13.8uA at each output current frequency (f(Iout)) ranging from 1.8Hz to 100MHz. Measurement conditions are as follows. Supply voltage (Vdd) equals 5.0V and setting voltage (Vset) as shown in Fig. 1 equals 3.0V.

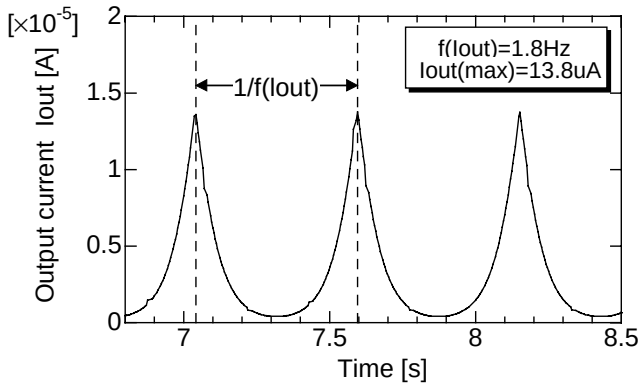

Fig. 8(a) Measured output current waveform at f(Iout)=1.8Hz.

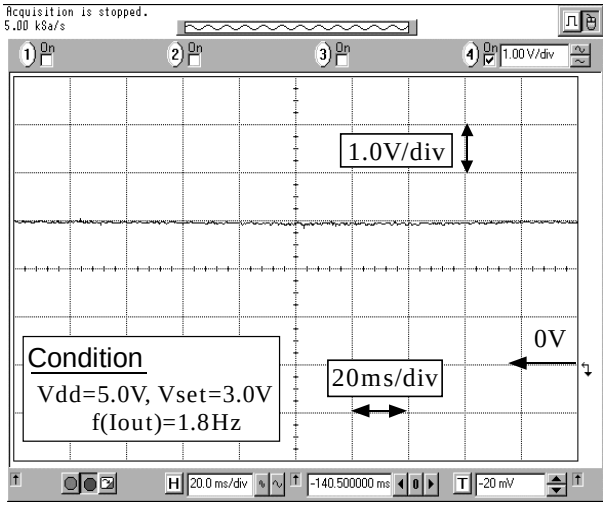

Fig. 8(b) Measured output voltage waveform at f(Iout)=1.8Hz.

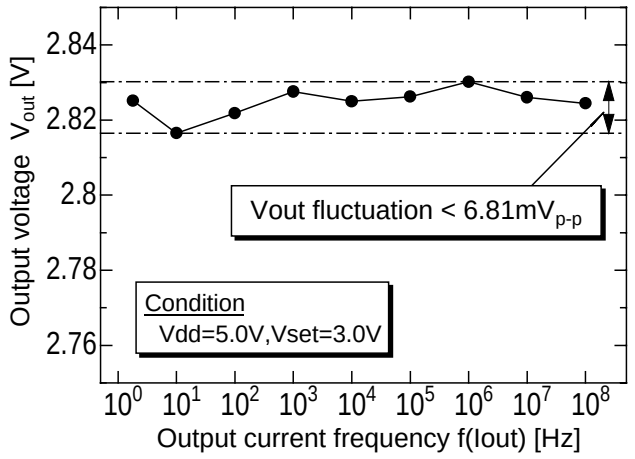

Fig. 8(c) Measured output voltage vs. output current frequency.

The linear regulator can supply an output voltage from 2.8302V to 2.8165V at a frequency of output current (f(Iout)) ranging from 1.8Hz to 100MHz. The linear regulator which is fabricated using 1.2µm technology achieves a fluctuation of output voltage less than 6.81mVpp at a frequency of output current (f(Iout)) ranging from 1.8Hz to 100 MHz. Moreover, the 1.2µm linear regulator achieves

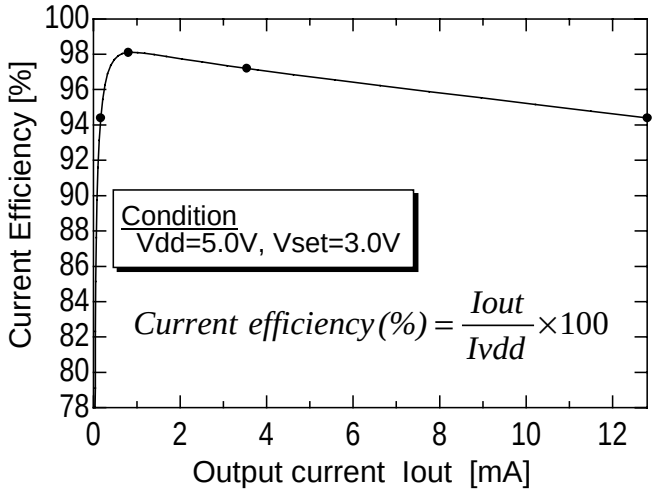

Fig. 9 Measured current efficiency of linear regulator with FCOC technique.

a fluctuation of output voltage less than 150mVpp at an output current ranging from 0 to 5.7mA. From circuit simulation results (HSPICE), it is estimated that the linear regulator using FCOC technique, which has designed using 0.13µm technology, achieves an output voltage fluctuation less than 30mVpp at output current ranging from 0 to 900mA.

Fig. 9 shows the measured current efficiency of fabricated linear regulator. X-axis is the output current (Iout) and Y-axis is the current efficiency of fabricated linear regulator. Measurement conditions are as follows. Supply voltage (Vdd) equals 5.0V and setting voltage (Vset) as shown in Fig. 1 equals 3.0V. This current efficiency is defined as the ratio of output current (Iout) to the total current of linear regulator (Ivdd). As the current efficiency increases, the power dissipation of the linear regulator decreases. Therefore, the enhanced current efficiency can achieve a linear regulator with reduced power consumption. The proposed on-chip linear regulator using FCOC technique achieves 96.5% current efficiency at an output current of 5.7mA and 90% current efficiency at an output current of 27.35mA. The concept of FCOC technique is that no current flows from Vdd to ground in FCOC circuit at any output voltage. However, actually Ivdd consists of Iout, Iself, Isub and Isub-hot. Iout is the output current of fabricated linear regulator. Iself is the current of Block (B). Isub is a pn leakage current from an N+ diffusion layer to substrate. Isub-hot is a hot carrier current to substrate from drain edge. Therefore, the measured current efficiency, Iout/Ivdd, is defined as Iout/(Iout+Iself+Isub+Isub-hot). Isub is proportional to the area of N+ diffusion layer. The on-chip CMOS linear regulator has a large size driver transistor in order to drive a large stable output current. In our proposed circuit there are three NMOS driver transistors whose gate width is 2000µm. The sum of NMOS transistor gate widths is more than 6000µm. Therefore, the area of N+ diffusion layer is very large and Isub is not negligible. Moreover, the

TABLE I
Chip performance summary.

Die size	0.423mm^2 (1.211x0.349mm^2)
Technology	1.2um CMOS 2AL 1PS
Number of Transistors	46
Current Efficiency	96.5% @ Iout=5.7mA, from 5V to 3V 90% @ Iout=27.35mA, from 5V to 3V
Output voltage range	0.61V - 3.69V
Output voltage fluctuation	2.850V - 3.106V @ Vdd=4.1V - 5.5V 2.850V - 2.951V @ Vdd=4.7V - 5.3V
Output voltage noise	<6.81mV$_{p-p}$ @f(Iout)=1.8Hz - 100MHz
Output current range	<5.7mA(DC) @Vout_fluctuation<150mV$_{p-p}$

pn junction is heated up as Iout increases as a result Isub increases, too. Moreover, usually hot carriers are generated at the drain edge area and generated hot holes flow to substrate. Therefore, hot hole carrier current Isub-hot flows to substrate. Isub-hot increases as Iout increases. From above all, the Isub and Isub-hot increase as Iout increases. In Fig. 9, the measured current efficiency decreases because Isub and Isub-hot increase according to the increase of Iout.

Table 1 summarizes the chip performance.

V. Conclusion

This paper proposed an on-chip 96.5% current efficiency CMOS linear regulator using a Flexible Control Technique of Output Current. By the use of the Flexible Control technique of Output Current (FCOC), the proposed circuit realizes to drive a flexible output current according to the output current variation. The FCOC technique dynamically drives the output current in seven different stages according to a variation of the output current. Moreover, the FCOC technique can achieve little consumption current even at flowing large output currents. Therefore, the proposed linear regulator can supply stable output voltage using FCOC technique at any place on chip. The linear regulator is fabricated by double metal 1.2µm CMOS technology. The number of transistors is 46 and the die size is 0.423mm2. The fabricated linear regulator achieves a fluctuation of output voltage less than 6.81mVpp at a frequency of output current (f(Iout)) ranging from 1.8Hz to 100 MHz. Moreover, the 1.2µm linear regulator achieves a fluctuation of output voltage less than 150mVpp at an output current ranging from 0 to 5.7mA. From circuit simulation results (HSPICE), it is estimated the linear regulator using FCOC technique, which has designed using 0.13µm technology, achieves an output voltage fluctuation less than 30mVpp at output current ranging from 0 to 900mA. The fabricated linear regulator using FCOC technique can achieve 96.5% current efficiency.

Acknowledgments

The authors thank VDEC as follows; "The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by Nippon Motorola LTD., Dai Nippon Printing Corporation, and KYOCERA Corporation."

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