A Smart Position Sensor for 3-D Measurement

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Abstract— A smart position sensor for 3-D measurement has been developed. The sensor is designed for detecting positions of laser spots projected on target objects quickly. The sensor has a 256×256 pixel array, a set of address decoders for variable block access and a variable block logical-OR circuit on an 8.9mm×8.9mm die. The sensor is designed and fabricated in 0.6μm CMOS 3-metal 2-poly-Si process. The measured accuracy of 3-D measurement is 0.4%. The speed of 3-D measurement is up to 10000points/s.

I. Introduction

The 3-D measurement is one of important techniques in the field of computer vision. In 3-D measurement using projection of spot lights, the information needed for acquiring 3-D positions is positions of the spot lights projected on the sensor plane. Lateral effect position sensitive photodetectors(LEP) are often used for position sensing. The LEP has problems in accuracy, linearity and effect of background illumination. Position sensing can also be achieved using imaging arrays such as CCDs. Higher resolution is needed to achieve higher accuracy using imaging arrays. However, the number of cycles needed to scan the entire image increases proportionally with the number of pixels using raster scan.

Some smart sensors to solve the problems were previously developed. Brajovic [1] developed a smart sensor for position detection using a 2-D winner-take-all circuit. The pixel with the highest intensity of incident light is determined by the 2-D winner-take-all circuit. Mäkynen [2] developed a binary image sensor for position sensing with adaptive threshold controlled by the intensity of background illumination. We developed a binary image sensor for position sensing using quad-tree scan [3]. We can reduce the number of cycles needed to scan the entire image using quad-tree scan [4].

II. Methods

A. 3-D measurement

The 3-D measurement method used in our 3-D measurement system is based on triangulation. Fig. 1 shows the model of the 3-D measurement method used in the system. The 3-D position of a target object can be calculated by the position of the laser spot on the acquired image($P_1(x, y, d)$ in Fig. 1). The 3-D position is represented by the following three equations.

$$X = xDtan\alpha_2/(xtan\alpha_2 + d) \quad (1)$$
$$Y = yDtan\alpha_2/(xtan\alpha_2 + d) \quad (2)$$
$$Z = dDtan\alpha_2/(xtan\alpha_2 + d) \quad (3)$$

Here, the value of α_2, d and D are known.

B. Quad-tree scan

The information needed for 3-D measurement is the position of the laser spot projected on the sensor plane. Fig. 2 shows the concept of quad-tree scan. The numbers written on nodes or pixels in Fig. 2 indicate the sequence of quad-tree scan. The number of cycles needed to scan the entire image can be reduced using quad-tree scan [4].

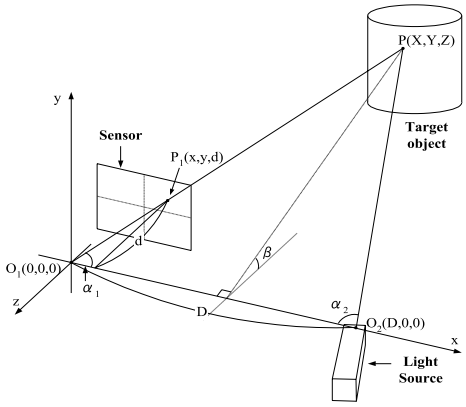


Fig. 1. Model of 3-D measurement method

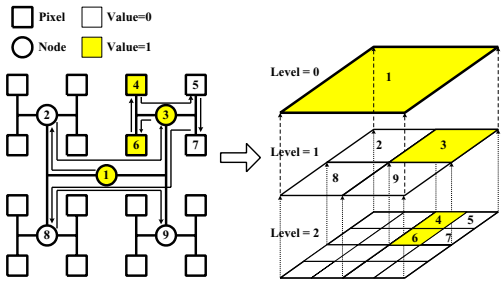


Fig. 2. Concept of quad-tree scan

III. Circuit realization

Fig. 3(a) shows a schematic of a pixel. A pixel is composed of a photo detector, a 1-bit D-latch and an output circuit. A photo detector is composed of a photo diode and a reset transistor. After integration of photo-current, the D-latch converts the output voltage of the photo detector to a binary value. The output circuit is a part of a dynamic logical-OR circuit.

The logical-OR of pixel values in a rectangular region is needed to realize the quad-tree scan. Fig. 3(b) shows a schematic of a variable block logical-OR circuit. The variable block logical-OR circuit is composed of a row logical-OR circuit and column logical-OR circuits. A column logical-OR circuit is composed of a transistor for pre-charge and pull-down transistors included in all pixels as output circuits. A column logical-OR circuit calculates the logical-OR of pixel values in a column. The row logical-OR circuit calculates the logical-OR of output values of selected column logical-OR circuits.

Fig. 3(c) shows a block diagram of a variable block address decoder. The variable block address decoder is composed of two standard address decoders and an address se-

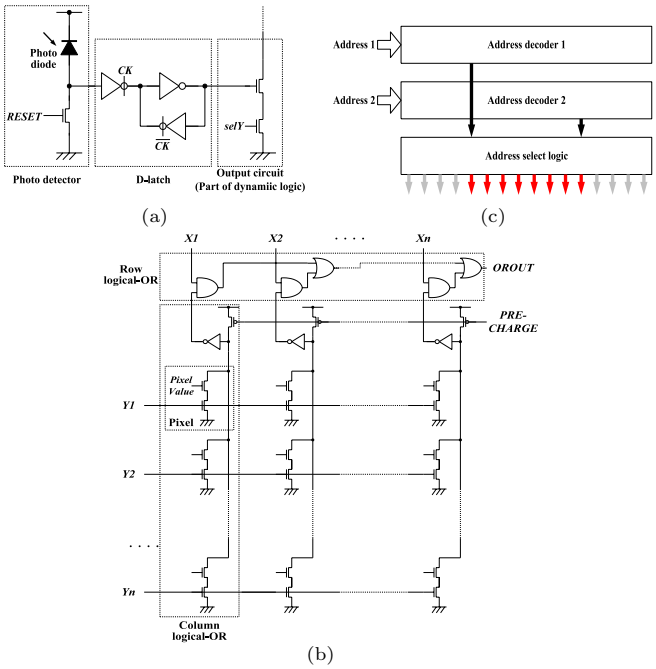


Fig. 3. Schematics and a block diagram of sensor circuits (a) schematic of a pixel (b) block diagram of a variable block address decoder (c) schematic of a variable block logical-OR circuit

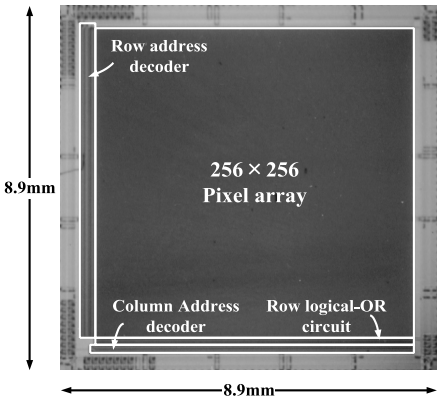


Fig. 4. Micrograph of the chip

lector. The variable block address decoder activates multiple address lines of the variable block logical-OR circuit between two addresses selected by the two standard address decoders simultaneously. The address select logic is composed of simple logic circuits.

Fig. 4 shows a micrograph of the fabricated chip. The sensor is fabricated using a 0.6μ CMOS 3-metal 2-poly-Si process.[1] Table. 1 shows a summary of the sensor.

IV. Experimental results

Fig. 5 shows a block diagram of a 3-D measurement system. The 3-D measurement system is composed of a position sensor, a laser with mirrors and a PC with an ADC/DAC board and a digital parallel I/O board. The PC acquires image data, controls the sensor and the mirrors and calculates the centroid of the laser spot.

[1]The VLSI chip in this study has been fabricated in the chip fabrication progrm of VLSI Design and Education Center(VDEC), the University of Tokyo with the collaboration by Rohm Corporation and Toppan Printing Corporation.

TABLE I
Summary of the image sensor

Process	0.6μm CMOS 3-metal 2-poly-Si
Chip size	8.9mm×8.9mm
Num. of pixels	256×256 pixels
Pixel size	28.1μm×28.1μm
Photo diode size	24.5μm×7.1μm
Fill-factor	22.1%
Number of FETs in a pixel	13 Transistors

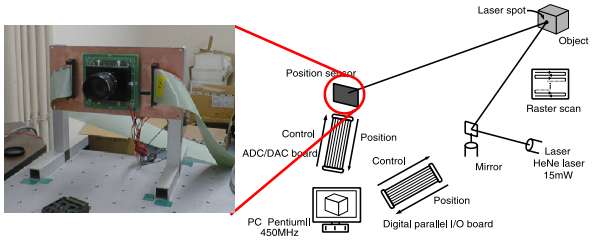
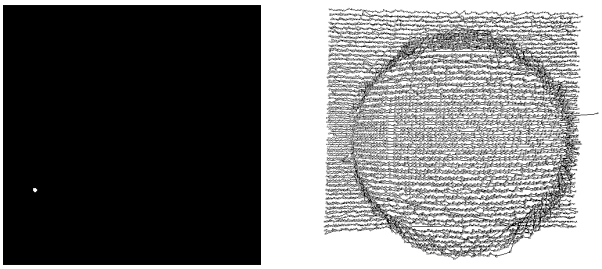


Fig. 5. Block diagmram of the experimental setup



(a) (b)

Fig. 6. Experimental results (a) acquired image of spot light (b) measurement result of sphere-shaped object

Fig. 6(a) shows an acquired image of a laser spot. The integration time of photo-current is 100μs. The number of activated pixels is 1-8. The number of cycles needed for quad-tree scan is 33-90. Fig. 6(b) shows a result of 3-D measurement. Here, 100×100 points of a sphere-shaped object are measured. The accuracy of 3-D measurement is measured by measuring 3-D positions of 8×8 points in a 20cm×20cm area on a flat panel. The measured accuracy of 3-D position is 0.4%. The speed of 3-D measurement is 2500points/s using a 2MHz digital I/O board. By the results of circuit simulation and measurement, the sensor can work up to the speed of 10000points/s.

V. Conclusions

A smart position sensor for 3-D measurement is developed. The sensor is designed for detecting the position of the laser spot quickly using quad-tree scan. The sensor has 256×256 pixels, a set of variable block address decoders and a variable block logical-OR circuit on the same chip. The sensor is fabricated in 0.6μm CMOS 3-metal 2-poly-Si process. The accuracy of 3-D measurement using developed system is 0.4%. The speed of 3-D measurement is up to 10000points/s.

References

[1] V. Brajovic and T. Kanade, "Computational Sensor for Visual Tracking with Attention," JSSC, Vol. 33, pp.1199–1207, 1998.

[2] A. Makynen, et.al., "A binary photodetector array for position sensing," Sensors and Actuators A, Vol. 65, pp.45–53, 1998.

[3] T. Nezuka, et.al., "A position detection sensor for 3-D measurement," Proc. of ESSCIRC, pp.412–415, Sep. 2000.

[4] J. Akita, K. Asada, "An Image Scanning Method with Selective Activation of Tree Structure," IEICE Trans. on Electronics, E80-C, No.7, pp.956–961, Jul. 1997.